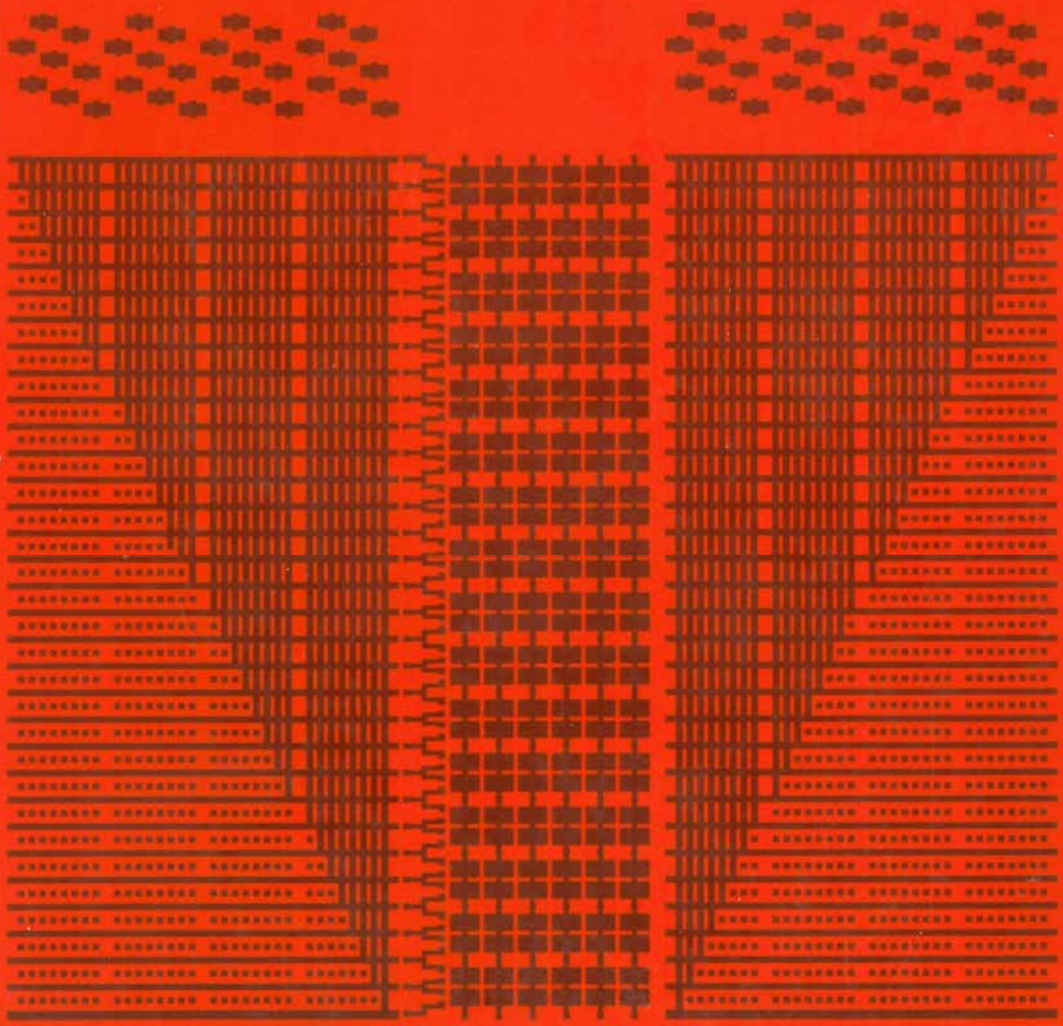
PROFESSIONAL SEMICONDUCTOR

DATABOOK 3

SGS ATES

LINEAR, MOS & COS/MOS
INTEGRATED CIRCUITS
1974/75



PROFESSIONAL SEMICONDUCTOR

DATABOOK 3

SGS ATES

LINEAR, MOS & COS/MOS INTEGRATED CIRCUITS 1974/75

INTRODUCTION

This databook contains data sheets on the SGS-ATES range of linear, MOS and COS/MOS integrated circuits intended for professional applications.
The information on each product has been specially presented in order that the performance of the product can be readily evaluated within any required equipment design.
Particular attention has been given to the measurement of the characteristics of all integrated circuits to ensure that they conform to the Company's Semiconductor Users' Reliability Evaluation programme (SURE).
The SURE programme has been carefully devised so as to be compatible with any national or international quality assurance programme. It is continuous (performed on all production batches), repetitive (performed under fixed conditions) and comprehensive (represents as many military and industrial specifications as possible).
It is emphasised that all products are produced from the same high grade silicon material and by the same manufacturing processes, the only difference in their classification being in the number and severity of tests applied and the degree of information supplied on each test.

OTHER SGS-ATES DATABOOKS

The SGS-ATES range of products includes discrete devices, linear and digital integrated circuits for both consumer and professional applications. Data sheets on these devices can be found in the following databooks:

SGS-ATES Professional Semiconductor Databook 1 (Small signal transistors, special assemblies)

SGS-ATES Professional Semiconductor Databook 2 (Bipolar digital integrated circuits)

SGS-ATES Consumer Semiconductor Databook (Integrated circuits, small signal transistors)

SGS-ATES Power Semiconductor Databook (Power transistors)

SGS-ATES GROUP OF COMPANIES

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ALPHA-NUMERICAL INDEX

LINEAR INTEGRATED CIRCUITS

MOS INTEGRATED CIRCUITS

COS/MOS INTEGRATED CIRCUITS

GENERAL ALPHA-NUMERICAL INDEX

E. = Extended temperature range
I. = Intermediate temperature range
S. = Standard temperature range

LINEAR INTEGRATED CIRCUITS

LINEAR INTEGRATED CIRCUITS

E. = Extended temperature range
I. = Intermediate temperature range
S. = Standard temperature range

Voltage regulator

STANDARD TEMPERATURE RANGE, 0°C ÷ 70°C

- OUTPUT CURRENT > 600 mA
- TIGHT TOLERANCE FOR OUTPUT VOLTAGE
- LOAD REGULATION LESS THAN 1%
- RIPPLE REJECTION 62 dB TYPICAL
- OVERLOAD AND SHORT CIRCUIT PROTECTION

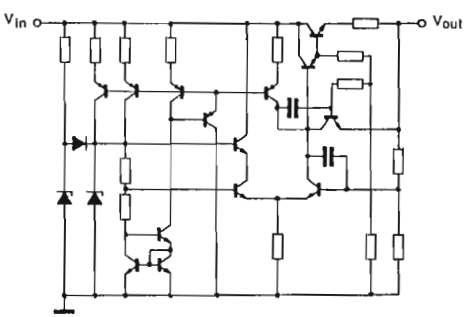
The L 005 T1 is a monolithic 5V voltage regulator which can supply more than 600 mA.
The device features high temperature stability, internal overload and short circuit protection, low output impedance and excellent transient response.
The L 005 T1 is intended for use as voltage supply for digital circuits and for any other industrial application.

ABSOLUTE MAXIMUM RATINGS

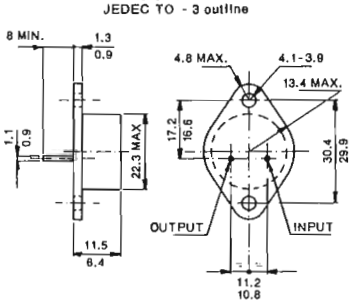
Input Voltage	20V
Power Dissipation (free air, $T_A = 25°C$)	3.25W
Power Dissipation (with infinite heat sink, $T_C = 25°C$)	12.75W
Storage Temperature Range	−55°C ÷ 150° C
Operating Temperature Range	0° C to + 70°C

ORDERING NUMBER
L005 T1

SCHEMATIC DIAGRAM



PHYSICAL DIMENSIONS
In accordance with
JEDEC TO - 3 outline



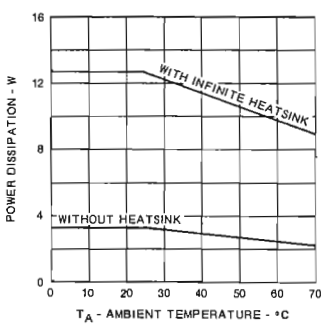
Notes:
All dimensions in mm.
Leads 1 and 2 electrically isolated from case.
Case is third electrical connection (ground).
Leads are gold-plated nickel-alloy.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

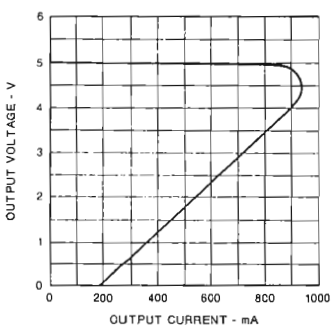
PARAMETER	CONDITIONS	Min.	Typ.	Max.	Unit
Output Voltage	V_{in} = 7.5V ÷ 20V, C_L = 10 μF, I_L = 10 mA	4.75	5.0	5.25	V
Load Regulation	V_{in} = 12V, I_L = 0 ÷ 600 mA		0.3	1	% Vout
Regulated Output Current	V_{in} = 12V, $\frac{\Delta Vout}{Vout} \leq 1\%$	600	850		mA
Maximum Output Current	V_{in} = 12V		930	1200	mA
Output Resistance	V_{in} = 12V, I_L = 0.6A		15		mΩ
Line Regulation	V_{in} = 7.5V ÷ 12V, C_L = 10 μF, I_L = 10 mA		0.1	0.5	% Vout
Ripple Rejection	V_{in} = 10V, ΔV_{in} = 4V_{pp}, f = 100 Hz	46	62		dB
Output Noise Voltage	V_{in} = 12V, I_L = 10 mA, C_L = 20 μF BW = 10 Hz ÷ 100 KHz		0.07		mV
Standby Current	V_{in} = 20V, I_L = 0		9		mA
Temperature Coefficient	V_{in} = 12V, I_L = 10 mA, C_L = 10 μF T_A = 0°C ÷ 60°C		0.003		%/°C
Short Circuit Current	V_{in} = 12V, V_{out} = 0		190	250	mA

TYPICAL ELECTRICAL CHARACTERISTICS

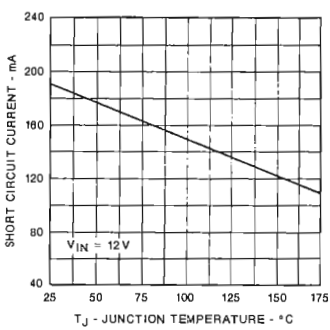
MAX ALLOWABLE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



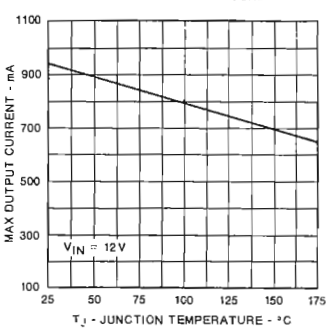
OUTPUT VOLTAGE VERSUS OUTPUT CURRENT



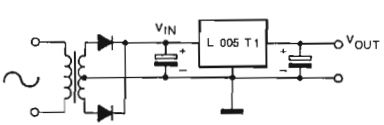
SHORT CIRCUIT CURRENT VERSUS JUNCTION TEMPERATURE



MAX OUTPUT CURRENT VERSUS JUNCTION TEMPERATURE



TYPICAL APPLICATION CIRCUIT



Balanced modulator

STANDARD TEMPERATURE RANGE -20° C TO 85° C

- SINGLE OR DUAL SUPPLY OPERATION
- LOW POWER CONSUMPTION
- LOW CARRIER LEAKAGE
- LOW DISTORTION
- LOW NOISE

The L 025 T9 is a linear integrated circuit intended for use as channel modulator and demodulator in FDM telephone equipment and as analogue AC multiplier in industrial and professional applications.
It features low quiescent power consumption, low distortion and intermodulation. The circuit requires a minimum number of external components.

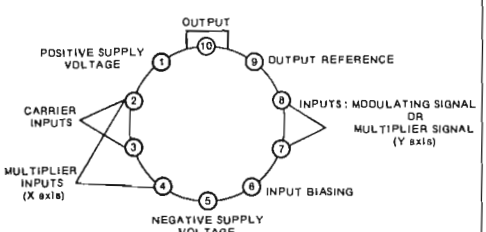
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	30 V
Differential Input Voltage	± 5 V
Power Dissipation (T_A = 70° C) (1)	300 mW
Storage Temperature	-55° C to 150° C
Operating Temperature	-20° C to 85° C

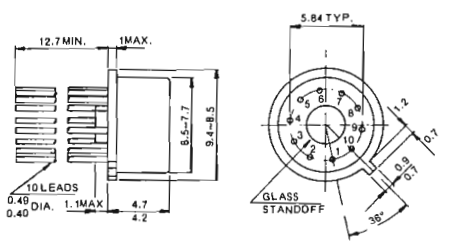
ORDERING NUMBER
L 025 T9

(1) Derate linearly at 3.75 mW/° C for ambient temperature above 70° C

CONNECTION DIAGRAM
(top view)



PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-100 outline



Note: all dimensions in mm.

ELECTRICAL CHARACTERISTICS:

WORKING CONDITIONS FOR THE CIRCUIT SHOWN IN FIG. 2
(unless otherwise specified)

Supply Voltage	V_{CC} = -20V
Carrier Frequency	f_c = 130 KHz
Modulating Signal Frequency	f_m = 25 KHz
Output Signal Level $[f_c \pm f_m = (130 \pm 25)KHz]$	V_o = -15dBv
Input Carrier Signal Level	V_c = -13dBv
Load Resistance	R_L = 600Ω
Ambient Temperature	T_A = 25°C

PARAMETER	CONDITIONS	Min.	Typ.	Max.	UNIT
Operating Supply Voltage Range		12		30	V
Supply Current	V_{CC} = ± 10V		2	2.5	mA
Input Bias Current: $\frac{I_2 + I_3}{2}$	V_{CC} = ± 10V		0.7	2	μA
$\frac{I_2 + I_4}{2}$	V_{CC} = ± 10V		0.7	2	μA
$\frac{I_7 + I_8}{2}$	V_{CC} = ± 10V		1.4	4	μA
Input Offset Current: $I_2 - I_3$	V_{CC} = ± 10V		50		nA
$I_2 - I_4$	V_{CC} = ± 10V		70		nA
$I_7 - I_8$	V_{CC} = ± 10V		100		nA
Input Common Mode Voltage:	V_{CC} = ± 10V				
Pos.			4.5		V
Neg.			-8		V
DC Output Voltage (pin 10)		-3.2	-3.8	-4.6	V
Differential Output Voltage (pins 9; 10)			25	100	mV
Input Biasing Reference Voltage (pin 6)			-7.5		V
Input Resistance: pins 2 and 3			30		KΩ
pins 2 and 4			300		KΩ
pins 7 and 8			150		KΩ
Output Resistance	f = 1 KHz		3	10	Ω
Output Voltage Swing		1	1.3		Vpp
Common Mode Rejection Ratio:					
CM Signal: pins 2 and 3	{ CM signal (2-3) (V=700mV rms; f_1 = 10 KHz) { Diff. signal (7-8) (V=350mV rms; f_2 = 40KHz)		98		dB
CM Signal: pins 2 and 4	{ CM signal (2-4) (V=700mV rms; f_1 = 10 KHz) { Diff. signal (7-8) (V=350mV rms; f_2 = 40KHz)		86		dB
CM Signal: pins 7 and 8	{ CM signal (7-8) (V=350mV rms; f_1 = 10KHz) { Diff. signal (2-3) (V=175mV rms; f_2 = 40KHz)		80		dB
Supply Voltage Rejection Ratio:	V_{CC} = ± 10V f = 1 KHz				
Pos.			33		dB
Neg.			80		dB
Scale Factor K	V_{CC} = ± 10V		3.2		V^{-1}
Conversion Gain G_c		4.5	5	5.5	dB
Carrier Leakage	$V_{modulating}$ = 0		-35	-50	dBv
Modulating Signal Leakage $\frac{V_{fm}}{V_{(fc \pm fm)}}$			-35	-50	dBmo
2nd Harmonic Modulating Signal Leakage $\frac{V_{(2fm)}}{V_{(fc \pm fm)}}$				-75	dBmo
2nd Harmonic Distortion $\frac{V_{(fc \pm 2fm)}}{V_{(fc \pm fm)}}$			-60	-75	dBmo
2nd Harmonic Distortion $\frac{V_{2(fc \pm fm)}}{V_{(fc \pm fm)}}$			-55	-80	dBmo
3rd Harmonic Distortion $\frac{V_{(fc \pm 3fm)}}{V_{(fc \pm fm)}}$			-60	-79	dBmo
Low Frequency Thermal Noise	$V_{modulating}$ = 0 f = 1KHz BW = 100 Hz	-115	-125		dBv
High Frequency Thermal Noise	$V_{modulating}$ = 0 f = 30KHz BW = 100 Hz		-127		dBv
Conversion Gain Change	T_A = 10°C to 50°C		±0.1		dB

ELECTRICAL DIAGRAM

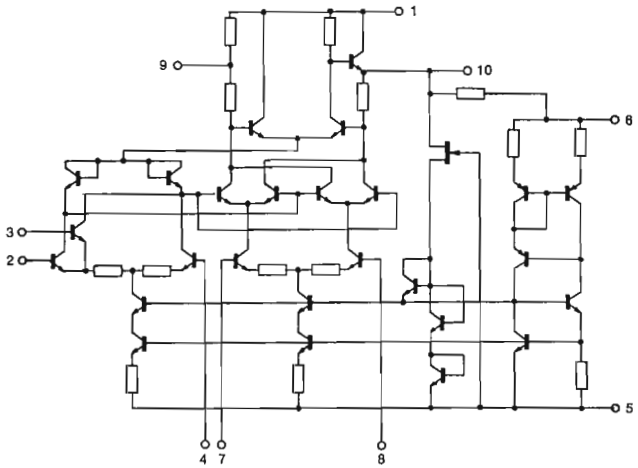


FIG. 1

TYPICAL APPLICATION OF MODULATOR WITH ONE SUPPLY VOLTAGE

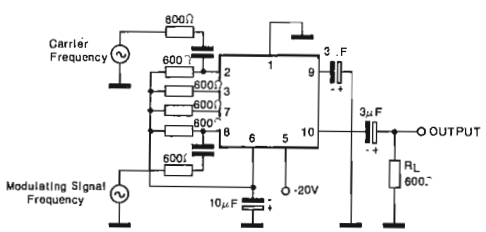


FIG. 2

DEFINITION OF UNITS:

dBm: power gain ($10 \lg \frac{P_2}{P_1}$) is expressed in dBm when P_1 is 1mW, therefore 0 dBm = 1mW.

dBmo: the power is expressed in dBmo when referred to an established power level in the circuit, generally the output signal level.

e.g. if the output level is -15 dBm and this level is chosen as reference, then we say 0 dBmo = -15 dBm; if another signal, i.e. the distortion measured at the same point of the circuit is -90 dBm, we can say that the distortion is -75 dBmo.

dBv: $20 \text{ Log} \frac{V_2}{V_1}$ when V_1 = 775 mVrms

DEFINITION OF TERMS:

Common mode rejection ratio: $CMRR = 20 \lg \frac{V_{CM}G}{V_{out}}$

with G = Conversion gain with specified circuit conditions
V_{CM} = Common mode signal level
V_{out} = Output signal level at frequency = $f_2 \pm f_1$

Scale factor: $K = \frac{V_{out}}{V_x V_y}$

with V_x = voltage input 2 - 4
V_y = voltage input 7 - 8

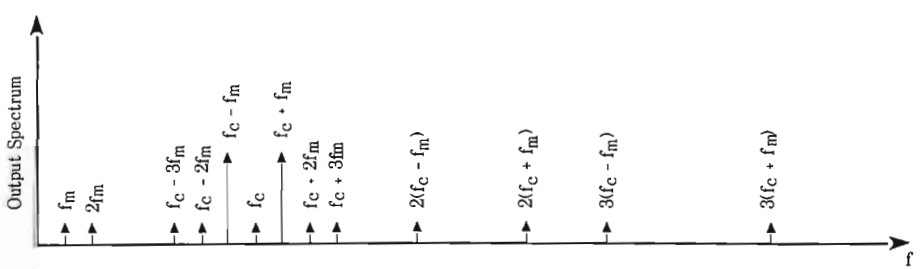
Conversion gain: $G_c = 20 \log \frac{V_{out\ (f_c \pm f_m)}}{V_{in\ (f_m)}}$

Carrier leakage: is defined as the output voltage at carrier frequency with only the carrier applied to the input (modulating voltage = 0)

Modulating signal leakage: is defined as the output voltage, at modulating frequency, referred to fundamental carrier sidebands

$M.S.L. = 20 \log \frac{V_{out\ (f_m)}}{V_{out\ (f_c \pm f_m)}}$

OUTPUT SPECTRUM VS. FREQUENCY



f_c = carrier fundamental (leakage)

f_m = mod. sig. (leakage)

nf_m = harmonic modulating signal (leakage)

$f_c \pm f_m$ = fundamental carrier sidebands

$f_c \pm nf_m$ = fundamental carrier sideband harmonics

$n(f_c \pm f_m)$ = carrier harmonic sidebands

Voltage regulator

STANDARD TEMPERATURE RANGE, 0°C ÷ 70°C

- OUTPUT CURRENT > 500 mA
- TIGHT TOLERANCE FOR OUTPUT VOLTAGE
- LOAD REGULATION LESS THAN 1%
- RIPPLE REJECTION 61 dB TYP.
- OVERLOAD AND SHORT CIRCUIT PROTECTION

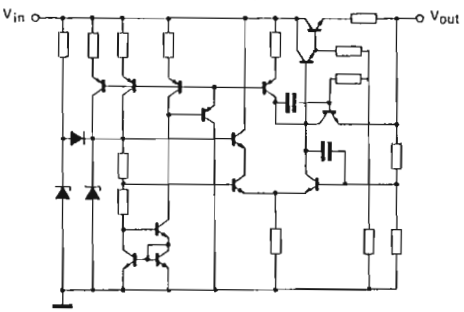
ORDERING NUMBER
L036 T1

The L 036 T1 is a monolithic 12V voltage regulator which can supply more than 500 mA.
The device features high temperature stability, internal overload and short circuit protection, low output impedance and excellent transient response.
The L 036 T1 is intended for use as voltage supply for digital circuit with high noise immunity, linear integrated circuits and for any other industrial application.

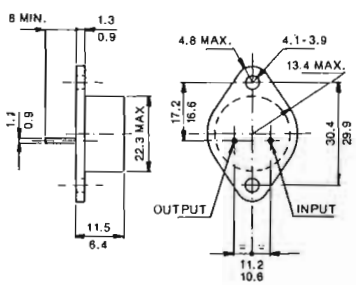
ABSOLUTE MAXIMUM RATINGS

Input Voltage	27V
Power Dissipation (free air, T_A =25°C)	3.25W
Power Dissipation (with infinite heat sink, T_C =25°C)	12.75W
Storage Temperature Range	−55°C - 150°C
Operating Temperature Range	0°C to + 70°C

SCHEMATIC DIAGRAM



PHYSICAL DIMENSIONS
In accordance with
JEDEC TO - 3 outline



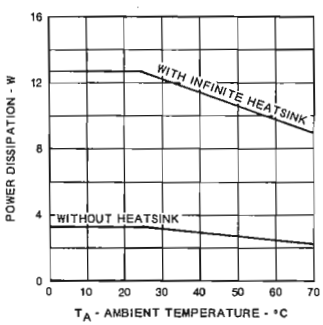
Notes:
All dimensions in mm.
Leads 1 and 2 electrically isolated from case.
Case is third electrical connection (ground).
Leads are gold-plated nickel-alloy.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

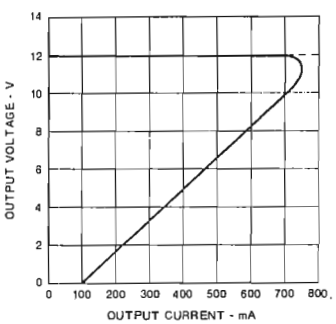
PARAMETER	CONDITIONS	Min.	Typ.	Max.	Unit
Output Voltage	V_{in} = 14.5 ÷ 27V, I_L = 10 mA, C_L = 10 μF	11.4	12	12.6	V
Load Regulation	V_{in} = 21V, I_L = 0 ÷ 500 mA		0.3	1	% Vout
Regulated Output Current	V_{in} = 21V, $\frac{\Delta Vout}{Vout} \leq 1\%$	500	720		mA
Maximum Output Current	V_{in} = 21V		750	1000	mA
Output Resistance	V_{in} = 21V, I_L = 500 mA		20		mΩ
Line Regulation	V_{in} = 14.5 ÷ 21V, C_L = 10 μF, I_L = 10 mA		0.1	0.5	%
Ripple Rejection	V_{in} = 19V, ΔV_{in} = 4 V_{pp}, f = 100 Hz, I_L = 10 mA	46	60		dB
Output Noise Voltage	V_{in} = 21V, I_L = 10 mA, C_L = 20 μF, BW = 10Hz ÷ 100 KHz		0.15		mV
Standby Current	V_{in} = 27V, I_L = 0		10		mA
Temperature Coefficient	V_{in} = 21V, I_L = 10 mA, T_A = 0°C ÷ 60°C		003		%/°C
Short Circuit Current	V_{in} = 21V, V_{out} = 0		100	200	mA

TYPICAL ELECTRICAL CHARACTERISTICS

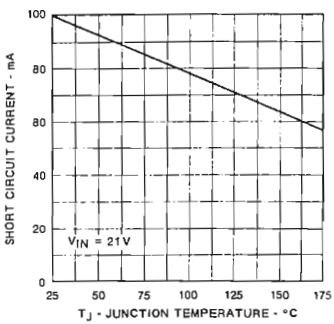
MAX ALLOWABLE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



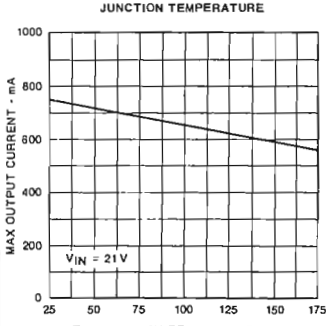
OUTPUT VOLTAGE VERSUS OUTPUT CURRENT



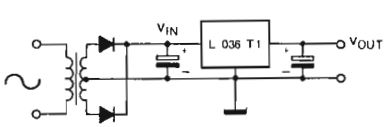
SHORT CIRCUIT CURRENT VERSUS JUNCTION TEMPERATURE



MAX OUTPUT CURRENT VERSUS JUNCTION TEMPERATURE



TYPICAL APPLICATION CIRCUIT



Voltage regulator

STANDARD TEMPERATURE RANGE, 0°C ÷ 70°C

- OUTPUT CURRENT > 450 mA
- TIGHT TOLERANCE FOR OUTPUT VOLTAGE
- LOAD REGULATION LESS THAN 1%
- RIPPLE REJECTION 56 dB
- OVERLOAD AND SHORT CIRCUIT PROTECTION

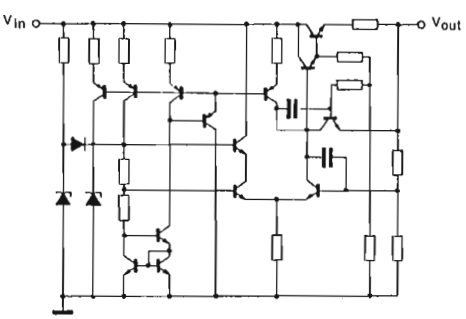
The L 037 T1 is a monolithic 15 V voltage regulator which can supply more than 450 mA.
The device features high temperature stability, internal overload and short circuit protection, low output impedance and excellent transient response.
The L 037 T1 is intended for use as voltage supply for linear integrated circuits, for digital circuits with high noise immunity and for any other industrial application.

ABSOLUTE MAXIMUM RATINGS

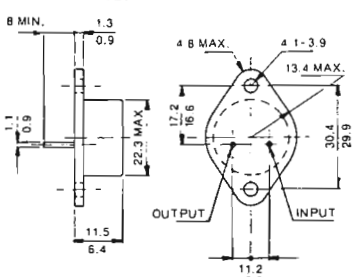
Input Voltage	27V
Power Dissipation (free air, $T_A = 25°C$)	3.25W
Power Dissipation (with infinite heat sink, $T_C = 25°C$)	12.75W
Storage Temperature Range	−55°C - 150°C
Operating Temperature Range	0°C to + 70°C

ORDERING NUMBER
L037 T1

SCHEMATIC DIAGRAM



PHYSICAL DIMENSIONS
in accordance with
JEDEC TO - 3 outline



Notes
All dimensions in mm.
Leads 1 and 2 electrically isolated from case.
Case is third electrical connection (ground).
Leads are gold-plated nickel-alloy.

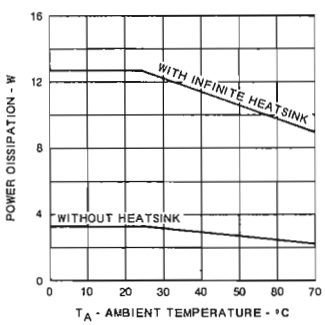
STANDARD TEMPERATURE RANGE

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

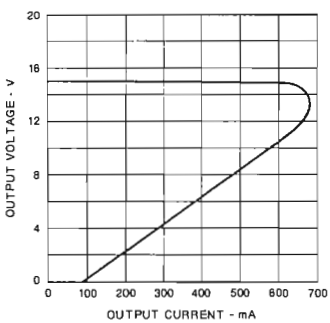
PARAMETER	CONDITIONS	Min.	Typ.	Max.	Unit
Output Voltage	V_{in}=17.5V÷27V, I_L=10 mA, C_L=10 μF	14.25	15	15.75	V
Load Regulation	V_{in}=24V, I_L=0÷450 mA		0.3	1	%Vout
Regulated Output Current	V_{in}=24V, $\frac{\Delta Vout}{Vout} \leq 1\%$	450	600		mA
Maximum Output Current	V_{in}=24V		680	900	mA
Output Resistance	V_{in}=24V, I_L=450 mA		27		mΩ
Line Regulation	V_{in}=17.5V÷24V, I_L=10 mA, C_L=10 μF		0.16	0.5	%
Ripple Rejection	V_{in}=22V, ΔV_{in}=4 Vpp, f = 100 Hz, I_L = 10 mA	46	56		dB
Output Noise Voltage	V_{in}=24V, I_L=10mA, C_L=20μF, BW=10Hz÷100KHz		0.18		mV
Standby Current	V_{in}=27V, I_L=0		10		mA
Temperature Coefficient	V_{in}=24V, I_L=10 mA, C_L=10μF, T_A=0÷60°C		0.003		%/°C
Short Circuit Current	V_{in}=24V		85	160	mA

TYPICAL ELECTRICAL CHARACTERISTICS

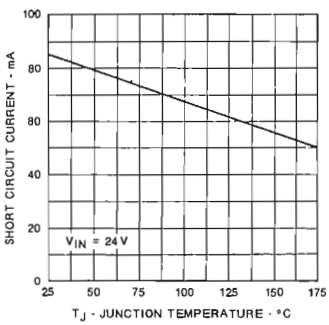
MAX ALLOWABLE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



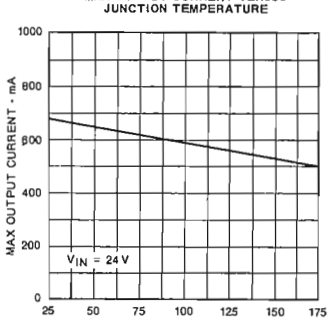
OUTPUT VOLTAGE VERSUS OUTPUT CURRENT



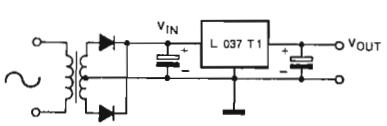
SHORT CIRCUIT CURRENT VERSUS JUNCTION TEMPERATURE



MAX OUTPUT CURRENT VERSUS JUNCTION TEMPERATURE



TYPICAL APPLICATION CIRCUIT



Channel amplifier

STANDARD TEMPERATURE RANGE, –20°C to +85°C

- LOW QUIESCENT POWER CONSUMPTION
- LOW DISTORTION
- HIGH GAIN
- SHORT CIRCUIT PROTECTION

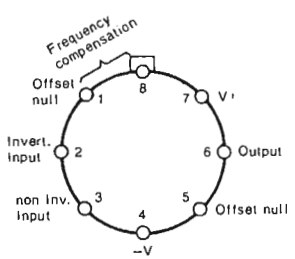
The L 045 T9 is a linear integrated circuit intended for use as channel amplifier in FDM and PCM telephone equipments.
It features low quiescent power consumption, low distortion, high gain.
The L 045 T9 is short circuit protected and shows an offset voltage null capability.

ABSOLUTE MAXIMUM RATINGS (1)

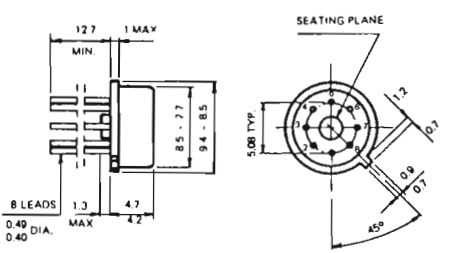
Supply Voltage	36V
Differential Input Voltage	±30V
Input Voltage	±12V
Power Dissipation (T_A = 70°C, see note 2)	500mW
Storage Temperature	–65°C ÷ 150°C
Operating Temperature	–20°C ÷ 85°C
Output short circuit duration	indefinite

Notes on the following page.

CONNECTION DIAGRAM
(top view)



PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-99 outline



Notes: All dimensions in mm.

ORDERING NUMBER
L045 T9

ELECTRICAL CHARACTERISTICS (note 3)

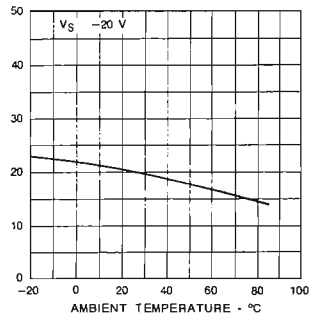
PARAMETER	CONDITIONS	Min.	Typ.	Max.	Unit
Input Offset Voltage	$R_S = 10\ K\Omega$		±1.5	±10	mV
Input Bias Current			100	750	nA
Input Resistance	open loop		2		MΩ
Output Resistance	open loop		75		Ω
Voltage Gain	$R_L = 2\ K\Omega$	83	100		dB
Total Harmonic Distortion	$P_{out} = -5dBm$ $G = 40dB$ $R_L eq. = 470\Omega$ $f = 1KHz$		1.5	3	‰
Total Harmonic Distortion	$P_{out} = 8dBm$ $G = 40dB$ $R_L eq. = 470\Omega$ $f = 1KHz$		1.5	3	‰
Quiescent Power Dissipation	$P_{out} = 0$		20	30	mW
Max Output Power	$R_L eq. = 470\Omega$ $THD \leq 1\%$ $G = 40dB$	14	16		dBm
Noise Power Referred to Input	$R_S \leq 1.5K\Omega$ $G = 40dB$ $f = 1KHz$ $BW = 100Hz$			-120.5	dBm
Supply Voltage Rejection Ratio Referred to Output	$f = 1KHz$ $G = 40dB$	30	36		dB
The Following Specifications apply for $-20°C \leq T_A \leq +85°C$:					
Input Offset Voltage	$R_S = 10\ K\Omega$			±15	mV
Input Bias Current				1.5	μA
Voltage Gain	$R_L = 2\ K\Omega$	78			dB

NOTES:

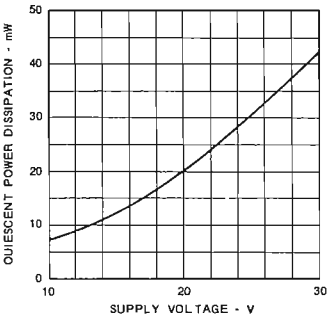
(1) $T_A = 25°C$ unless otherwise noted.
(2) Derate linearly at 6.25 mW/°C for ambient temperature above 70° C.
(3) $T_A = 25°C$, $V_S = -20V$, $V_R = -10V$ unless otherwise noted, for V_R see "Typical channel amplifier circuit".

TYPICAL ELECTRICAL CHARACTERISTICS (25° C free air temperature unless otherwise noted)

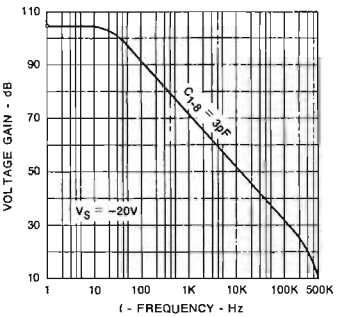
QUIESCENT POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



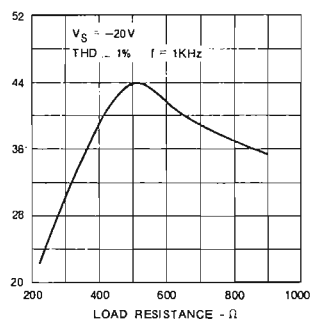
QUIESCENT POWER DISSIPATION VERSUS SUPPLY VOLTAGE



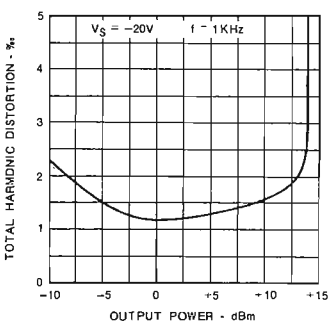
OPEN LOOP GAIN VERSUS FREQUENCY



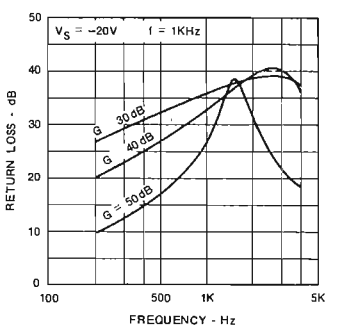
MAXIMUM OUTPUT POWER VERSUS LOAD RESISTANCE



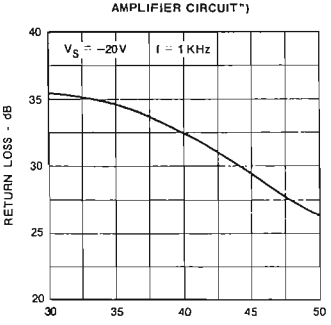
TOTAL HARMONIC DISTORTION VERSUS OUTPUT POWER



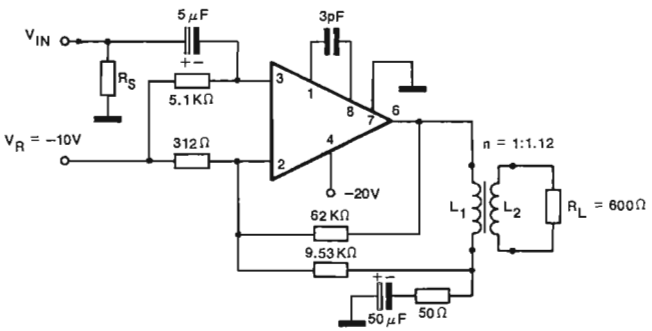
RETURN LOSS VERSUS FREQUENCY (RELATIVE TO "TYPICAL CHANNEL AMPLIFIER CIRCUIT")



RETURN LOSS VERSUS VOLTAGE GAIN (RELATIVE TO "TYPICAL CHANNEL AMPLIFIER CIRCUIT")



TYPICAL CHANNEL AMPLIFIER CIRCUIT



L_1 = 120 mH. Series resistance of: L_1 = 20 Ω
L_2 = 20 Ω

High speed operational amplifier

STANDARD TEMPERATURE RANGE,
0°C to 70°C

- HIGH SLEW RATE : 100V/ μS
- FAST SETTLING TIME : 300 ns
- WIDE BANDWIDTH : 65 MHz
- WIDE OPERATING SUPPLY RANGE
- WIDE INPUT VOLTAGE RANGES

The L 115 is a high speed, high gain, monolithic operational amplifier constructed on a single chip using the planar epitaxial process. It is intended for use in a wide range of applications where fast signal acquisition or wide bandwidth is required. The L 115 features fast settling time, high slew rate, low offsets, and high output swing for large signal applications. In addition, the device displays excellent temperature stability and will operate over a wide range of supply voltages. The L 115 is ideally suited for use in A to D and D to A converters, active filters, deflection amplifiers, video amplifiers, phase locked loops, multiplexed analogue gates, precision comparators, sample and holds, and general feedback applications requiring wide (including DC) bandwidth operation.

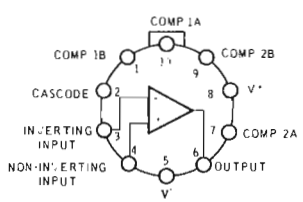
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	± 18 V
Internal Power Dissipation (note 1)	500 mW
Differential Input Voltage	± 6.5V
Input Voltage (note 2)	± 15V
Storage Temperature Range	-55°C to 150°C
Operating Temperature Range	0°C to 70°C
Lead Temperature (Soldering, 60 secs)	300°C

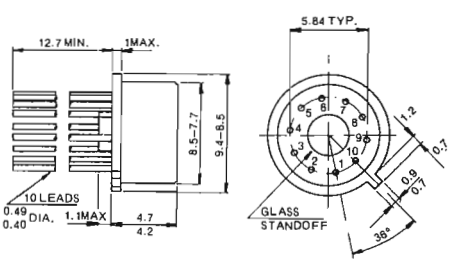
ORDERING NUMBER
L 115 T1

Notes on the following page.

CONNECTION DIAGRAM
(top view)



PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-100 outline



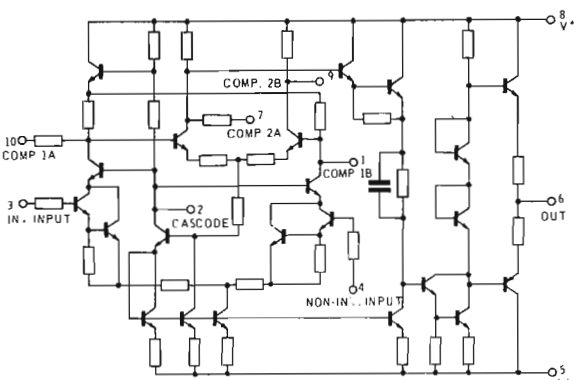
Note . all dimensions in mm.

STANDARD TEMPERATURE RANGE

ELECTRICAL CHARACTERISTICS (V_{CC} = ± 15V, T_A =25°C unless otherwise noted)

PARAMETER	CONDITIONS	Min.	Typ.	Max.	UNIT
Input Offset Voltage	$R_S \leq$ 10 kΩ		± 2	± 7.5	mV
Input Offset Current			± 70	± 250	nA
Input Bias Current			0.4	1.5	µA
Input Resistance			1		MΩ
Input Voltage Range		± 10	± 12		V
Common Mode Rejection Ratio	$R_S \leq$ 10 kΩ	74	92		dB
Supply Voltage Rejection Ratio	$R_S \leq$ 10 kΩ		45	400	µV / V
Large Signal Voltage Gain	$R_L \geq$ 2kΩ V_{OUT}= ± 10V	10,000	30,000		
Output Resistance			75		Ω
Supply Current			5.5	10	mA
Power Consumption			165	300	mW
Acquisition Time (Unity Gain)	V_{OUT} = + 5V		800		ns
Settling Time (Unity Gain)			300		ns
Transient Response (Unity Gain)	V_{IN} = 400 mV				
Rise Time			30	75	ns
Overshoot			25	50	%
Slew Rate	A_V = 100		70		V/ µs
	A_V = 10		38		V/ µs
	A_V = 1 (non-inverting)	10	18		V/ µs
	A_V = 1 (inverting)		100		V/ µs
The following apply for 0°C ≤ T_A ≤ + 70°C :					
Input Offset Voltage	$R_S \leq$ 10 kΩ			± 10	mV
Input Offset Current	T_A = + 70°C			± 250	nA
	T_A = 0°C			± 750	nA
Input Bias Current	T_A = + 70°C			1.5	µA
	T_A = 0°C			7.5	µA
Large Signal Voltage Gain	$R_L \geq$ 2 kΩ V_{OUT} = ± 10V	8,000			
Output Voltage Swing	$R_L \geq$ 2 kΩ	± 10	± 13		V

EQUIVALENT CIRCUIT

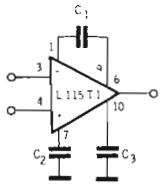


NOTES :

1) Rating applies for ambient temperatures to +70°C.
2) For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

COMPENSATION COMPONENTS VALUES

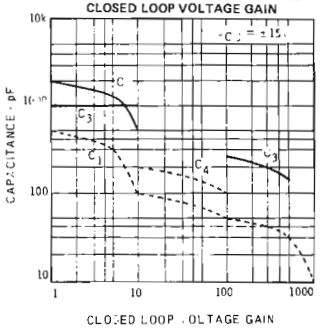
FREQUENCY COMPENSATION CIRCUIT



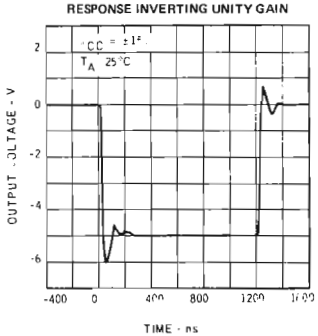
CLOSED LOOP GAIN	C_1	C_2	C_3
1000	10 pF		
100	50 pF		250 pF
10*	100 pF	500 pF	1000 pF
1	500 pF	2000 pF	1000 pF

* For Gain 10, compensation may be simplified by removing C_2, C_3 and adding a 200 pF capacitor (C_4) between Pin 7 and 10.

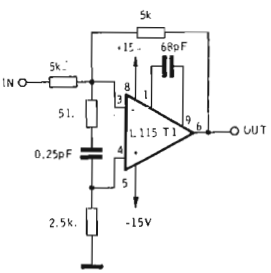
SUGGESTED VALUES OF COMPENSATION CAPACITORS AS A FUNCTION OF THE CLOSED LOOP VOLTAGE GAIN



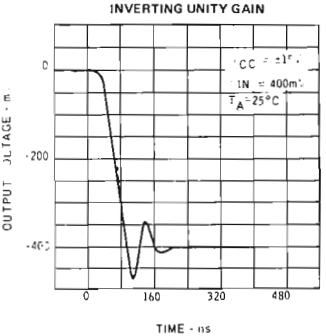
LARGE SIGNAL PULSE RESPONSE INVERTING UNITY GAIN



INVERTING UNITY GAIN HIGH SLEW RATE CIRCUIT

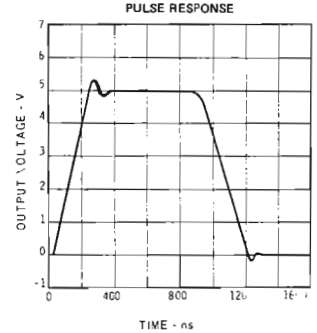


SMALL SIGNAL PULSE RESPONSE INVERTING UNITY GAIN

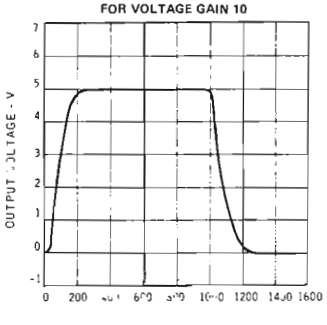


TYPICAL ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = ±15V unless otherwise noted)

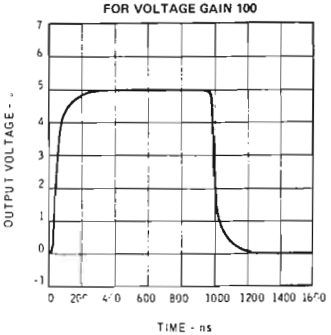
UNITY GAIN LARGE SIGNAL PULSE RESPONSE



LARGE SIGNAL PULSE RESPONSE FOR VOLTAGE GAIN 10

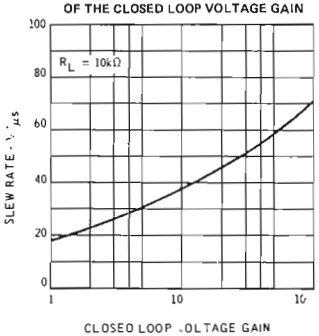


LARGE SIGNAL PULSE RESPONSE FOR VOLTAGE GAIN 100

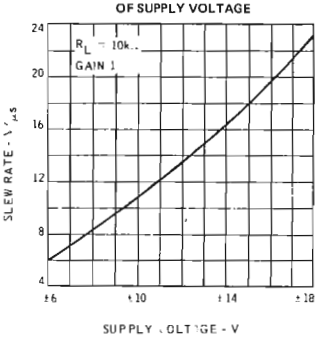


TYPICAL ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = ±15V unless otherwise noted)

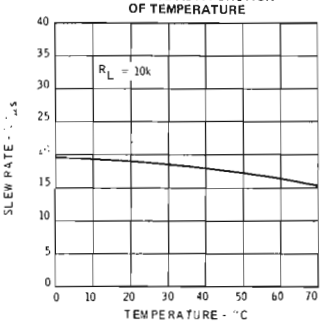
SLEW RATE AS A FUNCTION OF THE CLOSED LOOP VOLTAGE GAIN



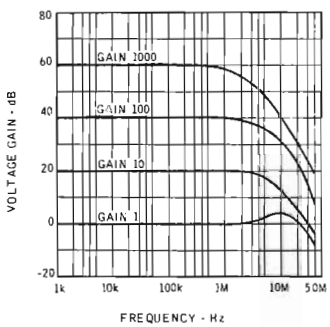
SLEW RATE AS A FUNCTION OF SUPPLY VOLTAGE



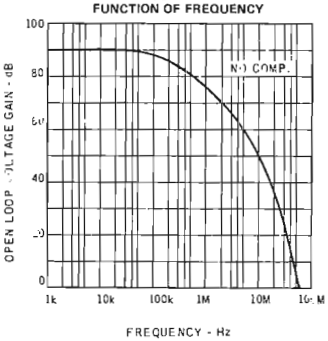
SLEW RATE AS A FUNCTION OF TEMPERATURE



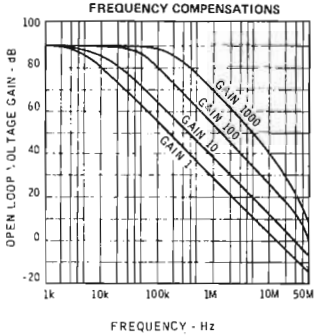
CLOSED LOOP FREQUENCY RESPONSE FOR VARIOUS GAIN CONFIGURATIONS



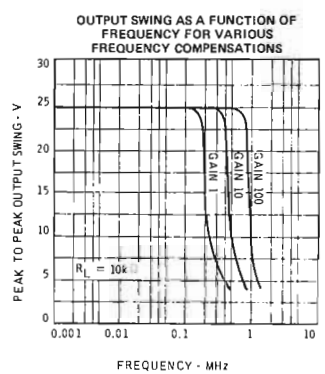
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



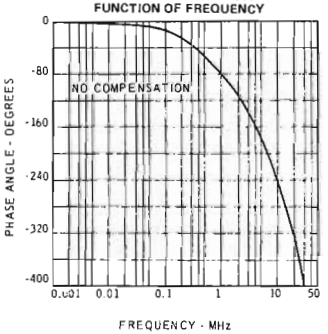
OPEN LOOP RESPONSE WITH COMPENSATION NECESSARY FOR VARIOUS FREQUENCY COMPENSATIONS



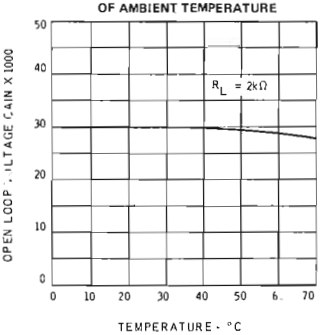
OUTPUT SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS FREQUENCY COMPENSATIONS



OPEN LOOP PHASE AS A FUNCTION OF FREQUENCY

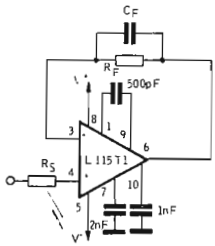


OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE

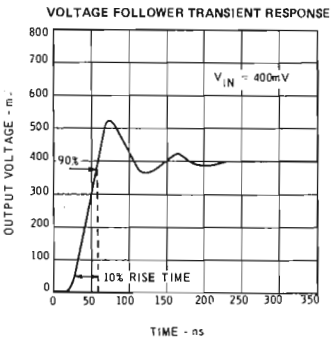


TYPICAL ELECTRICAL CHARACTERISTICS (T_A = 25°C; V_{CC} = ±15V unless otherwise noted)

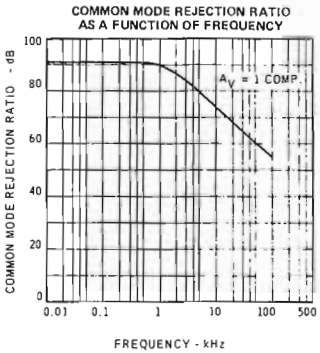
VOLTAGE FOLLOWER



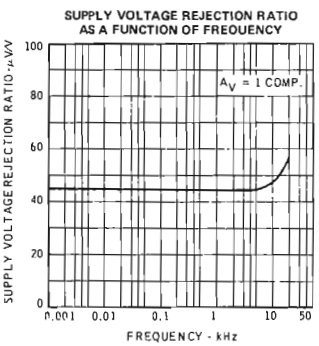
VOLTAGE FOLLOWER TRANSIENT RESPONSE



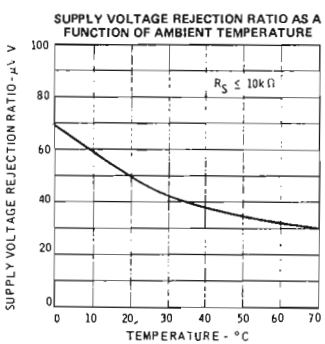
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



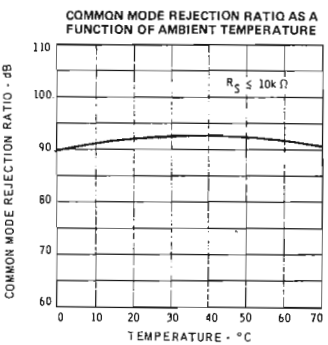
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF FREQUENCY



SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE

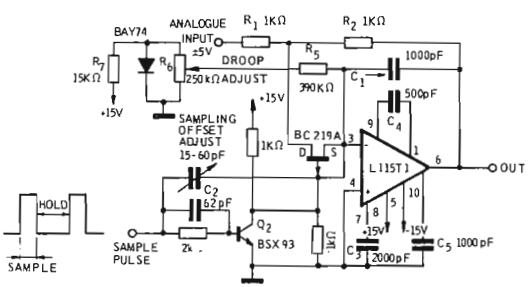


COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



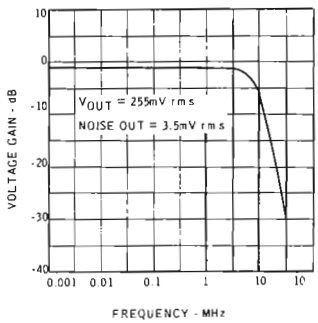
TYPICAL APPLICATIONS

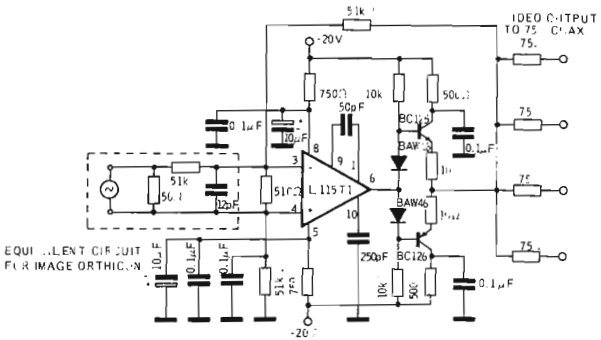
HIGH SPEED SAMPLE AND HOLD



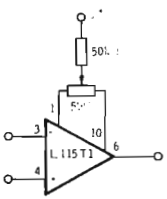
TYPICAL APPLICATIONS (contd)

WIDE BAND VIDEO AMPLIFIER WITH
75Ω COAX CABLE DRIVE CAPABILITY

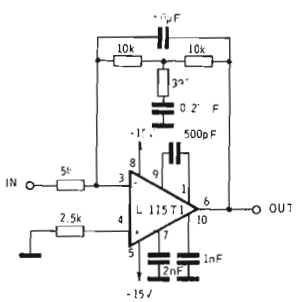


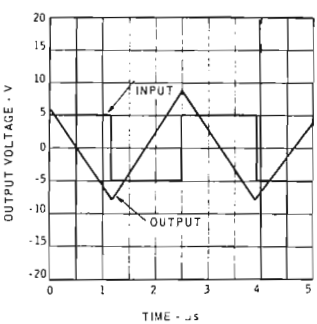


VOLTAGE OFFSET
NULL CIRCUIT



HIGH SPEED INTEGRATOR





DEFINITION OF TERMS

INPUT OFFSET VOLTAGE – That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT – The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE – The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT – The average of the two input currents.

INPUT VOLTAGE RANGE – The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO – The ratio of the input voltage range to the maximum change in input offset voltage over this range.

SUPPLY VOLTAGE REJECTION RATIO – The ratio of the change in input offset voltage to the change in supply voltage producing it.

LARGE-SIGNAL VOLTAGE GAIN – The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING – The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE – The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small-signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

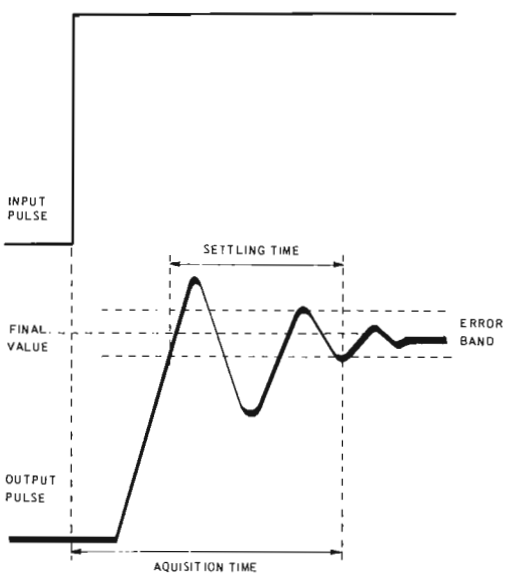
POWER CONSUMPTION – The DC power required to operate the amplifier with the output at zero and with no load current.

TRANSIENT RESPONSE – The closed-loop step-function response of the amplifier under small-signal conditions.

ACQUISITION TIME – The time from change of input until last time output exceeds specified percent of final value.

SLEW RATE – The maximum rate of change of output under large-signal conditions.

SETTLING TIME – The time from output first reaching final value until last time output exceeds specified percent of final value.



HELPFUL HINTS

LAYOUT – The layout should besuch that stray capacitance is minimal.

SUPPLIES – The supplies should be adequately bypassed. Use of 0.1 μF high quality ceramic capacitors is recommended.

RINGING – Excessive ringing (long acquisition time) may occur with large capacitive loads. This may be reduced by isolating the capacitive load with a resistance of 100 Ω.Large source resistances may also give rise to the same problem and this may be decreased by the addition of a capacitance across the feedback resistance. A value of around 50 pF for unity gain configuration and around 3 pF for gain 10 should be adequate.

LATCH UP – This may occur when the amplifier is used as a voltage follower. The inclusion of a diode between pins 6 and 2 with the cathode towards pin 2 is the recommended preventive.

LINEAR INTEGRATED CIRCUIT

L 120

PRELIMINARY DATA

TRIAC/SCR PHASE CONTROL

The L120 is a silicon monolithic integrated circuit in 16-lead dual in-line plastic package. It incorporates the following functions :

- AC supply 50/60 Hz
- zero-voltage and zero-current detection
- ramp generation
- inhibition of casual firing pulses
- stabilization of the internal positive DC supply
- high gain operational amplifier
- output short-circuit protection

The L120 is intended for use as a phase controller in industrial and consumer applications.

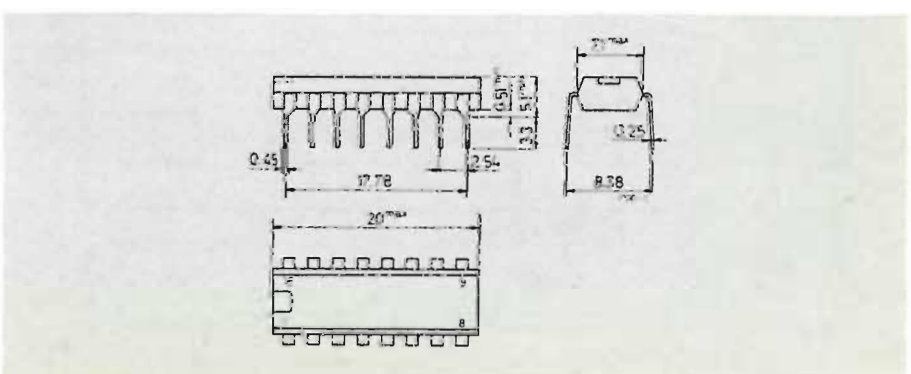
ABSOLUTE MAXIMUM RATINGS

I_9	AC supply current	60	mA
V_{8-12}	Positive AC clamp voltage	15	V
V_{10-12}	Negative AC clamp voltage	15	V
V_{1-2}	Differential input voltage	± 7	V
V_{3-5}	Differential input voltage	± 8	V
P_{tot}	Total power dissipation at $T_{amb} \leqslant 70°C$	450	mW
T_{stg}	Storage temperature	-55 to 150	°C
T_{op}	Operating temperature	0 to 70	°C

ORDERING NUMBER : L 120 B1.

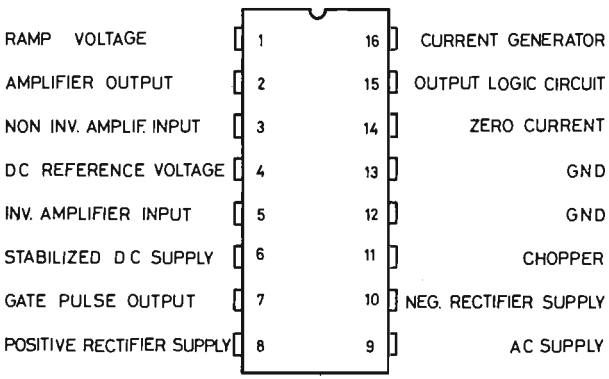
MECHANICAL DATA

Dimensions in mm



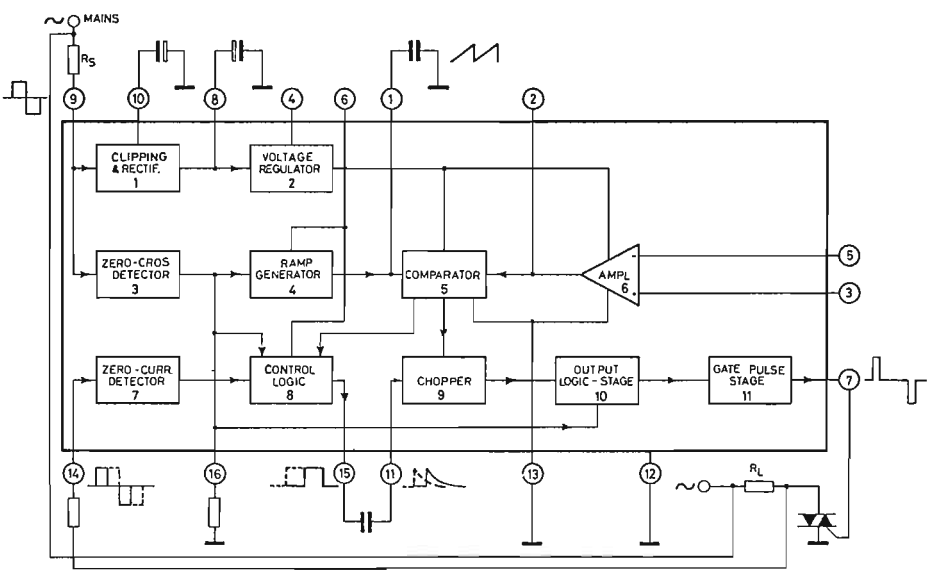
L 120

CONNECTION DIAGRAM (top view)



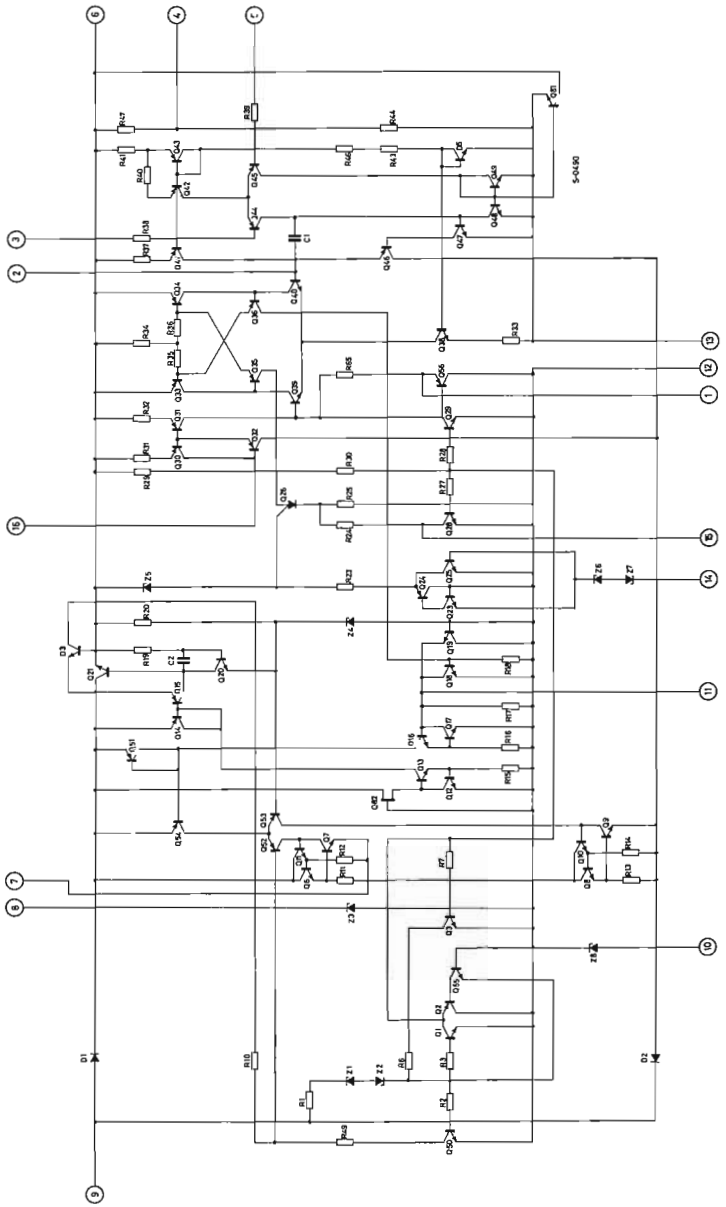
S-0404

BLOCK DIAGRAM

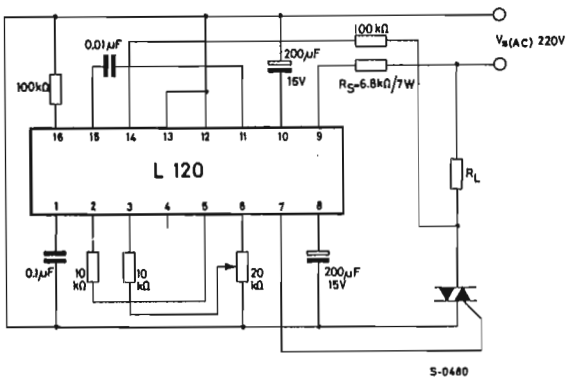


S-0510/1

SIMPLIFIED SCHEMATIC DIAGRAM



TEST CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}amb}$ Thermal resistance junction-ambient	max	175	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, refer to the test circuit unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{8\text{-}12}$ Positive clamp voltage	$V_{s\ (AC)}$ = 220V R_S =6.8kΩ		12	15	V
$V_{10\text{-}12}$ Negative clamp voltage			12	15	V
$V_{9\text{-}12}$ Sync input threshold			±12		V
$V_{14\text{-}12}$ Zero current threshold	$V_{s\ (AC)}$ =220V R_S=6.8kΩ R_{14} = 100kΩ		±9	±10	V
$V_{1\text{-}12}$ Ramp discharge level	$V_{s\ (AC)}$ =220 V R_S=6.8kΩ			1	V
$V_{1\text{-}12}$ Ramp maximum level		7			V

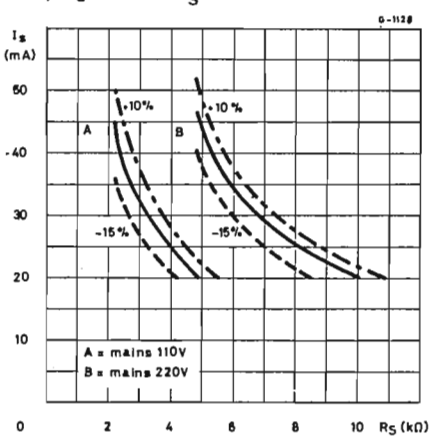
ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{1-2}	Comparator differential trigger level	$V_{6-13} = 8V$		70	100	mV
V_{1-13}, V_{2-13}	Comparator input voltage range		0		7	V
G_v	Amplifier large signal voltage gain (open loop)	V_2 (peak to peak) = 6V $V_{6-13} = 8V$ $R_{2-13} = 10k\Omega$	60	70		dB
→ ΔV_{2-13}	Amplifier output voltage swing	$V_{6-13} = 8V$ $R_{2-13} = 20k\Omega$	5.5			V
V_{3-13}, V_{5-13}	Input offset voltage	$V_{6-13} = 8V$ $R_{3-13} = R_{5-13} = 50\Omega$		3	6	mV
I_b	Input bias current	$V_{6-13} = 8V$		0.1	1	μA
V_{3-5}	Amplifier differential input voltage				±7	V
V_{3-13}, V_{5-13}	Amplifier input voltage range		0		8	V
CMRR	Common mode rejection ratio	$V_{6-13} = 8V$ $R_{3-13} = R_{5-13} \leqslant 1k\Omega$		60		dB
V_{6-13}	Regulator output voltage	$V_{s\,(AC)} = 220V$ $R_S = 6.8k\Omega$	7.5		8.7	V
I_6	Regulator output current	$V_{s\,(AC)} = 220V$ $R_S = 6.8k\Omega$ $C_8 = 250\mu F$			3	mA
$\frac{\Delta V_6}{V_6}$	Load regulation	$V_{s\,(AC)} = 220V$ $I_6 = 0$ to 2mA $R_S = 6.8k\Omega$ $C_8 = 250\mu F$		0.5	1	%
$\frac{\Delta V_6}{\Delta V_8}$	Line regulation	$V_8 = 12$ to 14V $I_6 = 0$		46		dB
SVR	Supply voltage rejection	$V_8 = 12V$ $f_{ripple} = 50$ Hz V_{ripple} (peak to peak) = 4V		46		dB

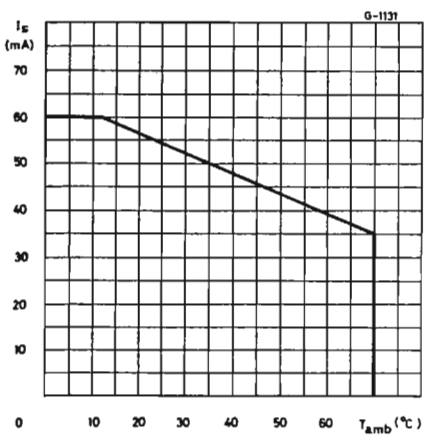
ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min. Typ. Max.	Unit
V_4	Reference voltage	$V_{s(AC)}$ =220V R_S= 6.8kΩ	1.5	V
→ V_{7-12}	Firing pulse amplitude	$V_{s(AC)}$=220V R_S= 6.8kΩ R_{7-12} = 1kΩ C_8 = 250μF positive negative	 5.5 -9.5	 V V
I_7	Maximum output current	$V_{s\ (AC)}$= 220V R_S=6.8kΩ R_{7-12} = 10Ω C_8=250μF	80	mA
t_{pw}	Output pulse width	$V_{s\ (AC)}$= 220V R_S=6.8kΩ	200	μs
t_r	Output pulse rise time	R_{7-12} = 50Ω C_8 =250μF C_{11-15} = 10 nF	200	ns

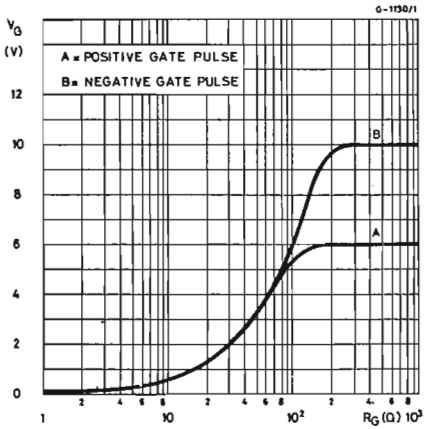
Typical average supply current vs.dropping resistor R_S



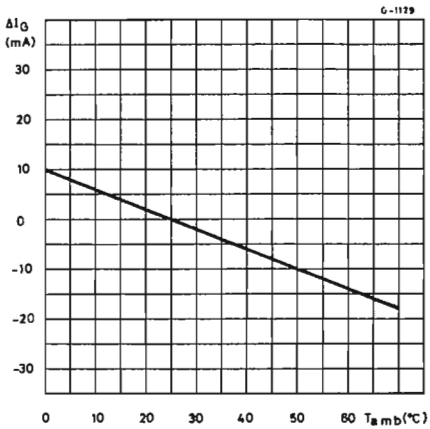
Maximum allowable average supply current vs.ambient temperature



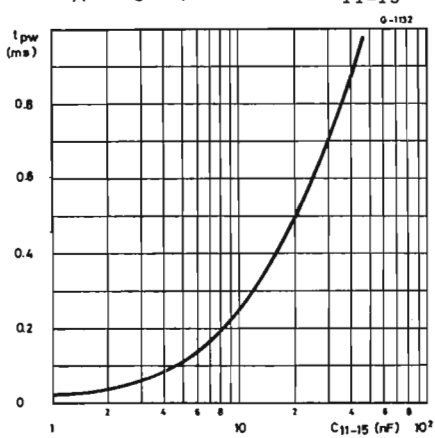
Typical gate pulse amplitude vs. gate resistance



Typical gate current variation vs. ambient temperature

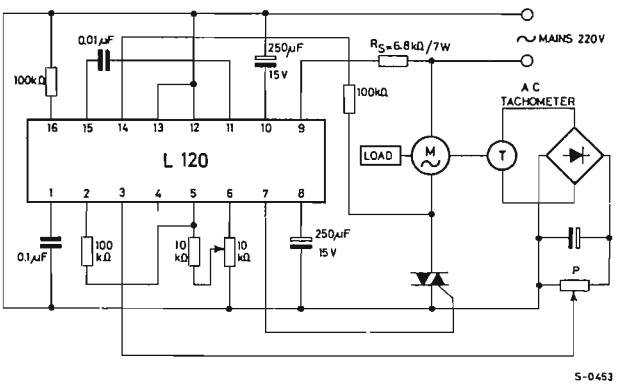


Typical gate pulse width vs. C_{11-15}

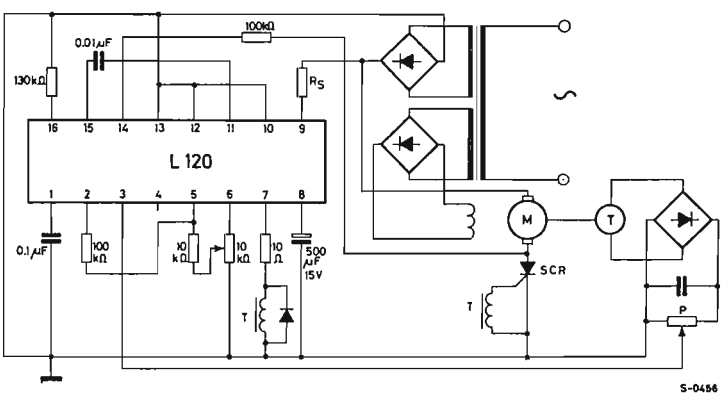


APPLICATION INFORMATION

Application circuit for AC motor speed regulators



Application circuit for DC motor speed regulators



LINEAR INTEGRATED CIRCUIT

L 121

PRELIMINARY DATA

TRIAC/SCR BURST CONTROL

The L121 is a silicon monolithic integrated circuit in 16-lead dual in-line plastic package. It incorporates the following functions :

- AC supply 50/60 Hz
- zero-voltage detection
- ramp generation
- inhibition of casual firing pulses
- stabilization of the internal positive DC supply
- high gain operational amplifier
- output short-circuit protection

The L121 is intended for use as a burst controller in industrial and consumer applications.

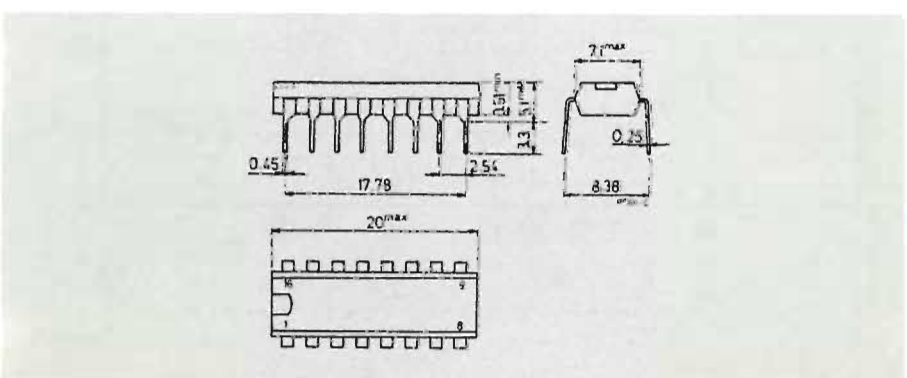
ABSOLUTE MAXIMUM RATINGS

I_9	AC supply current	60	mA
$V_{8\text{-}12}$	Positive AC clamp voltage	15	V
$V_{10\text{-}12}$	Negative AC clamp voltage	15	V
$V_{1\text{-}2}$	Differential input voltage	± 7	V
$V_{3\text{-}5}$	Differential input voltage	± 8	V
P_{tot}	Total power dissipation at $T_{amb} \leqslant 70°C$	450	mW
T_{stg}	Storage temperature	-55 to 150	°C
T_{op}	Operating temperature	0 to 70	°C

ORDERING NUMBER : L 121 B1

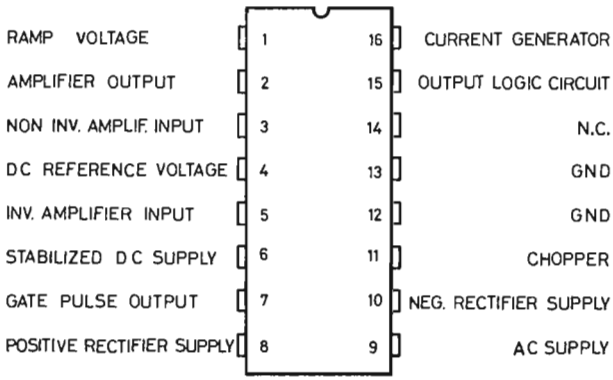
MECHANICAL DATA

Dimensions in mm.



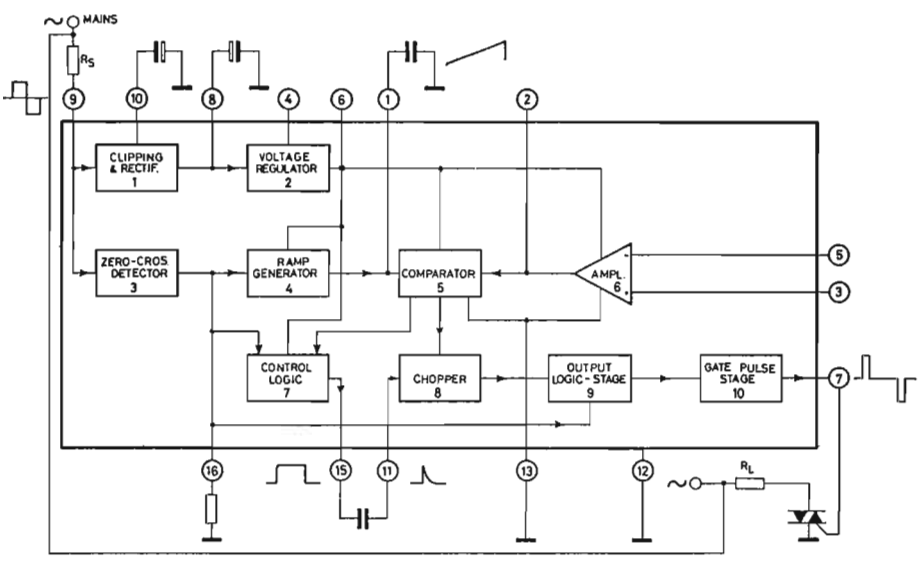
L 121

CONNECTION DIAGRAM (top view)



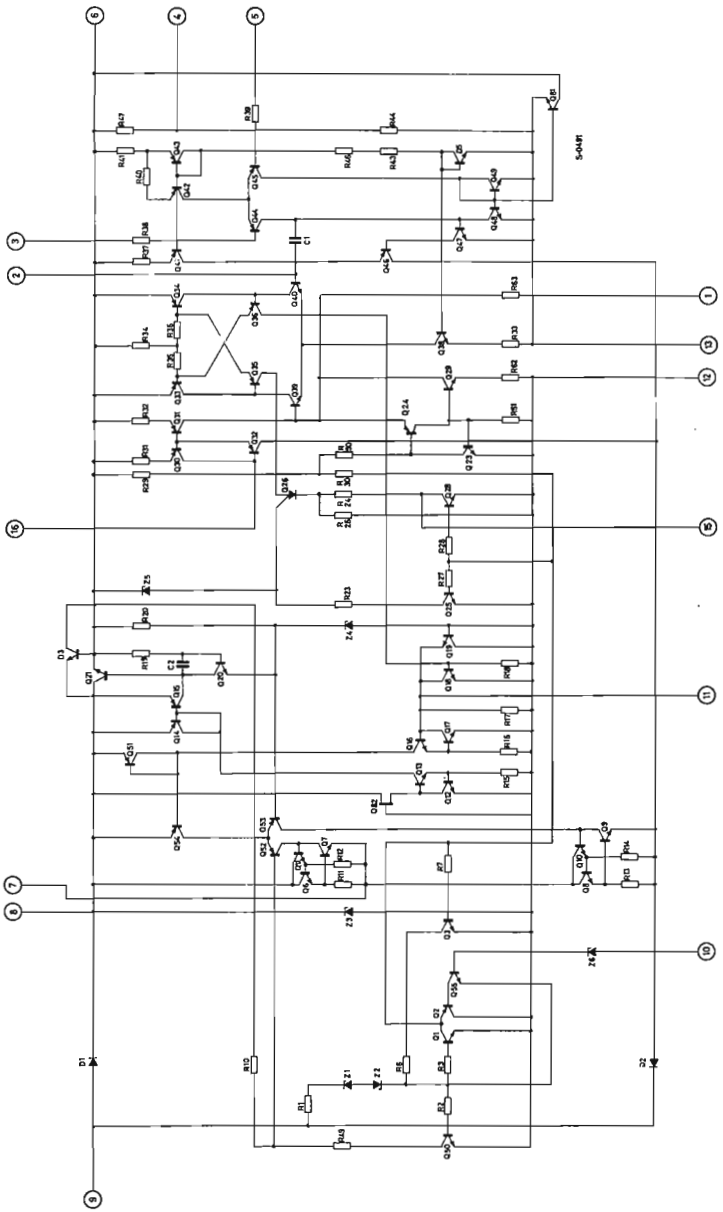
S-0481

BLOCK DIAGRAM



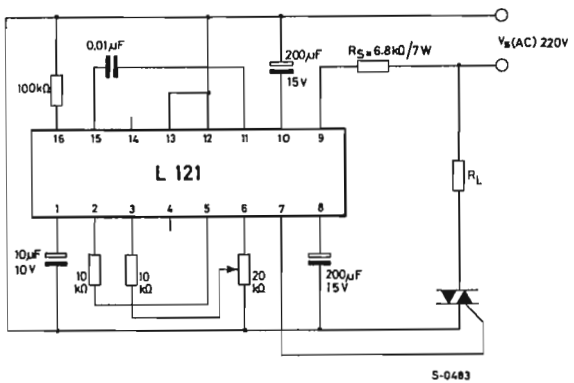
S-0511/1

SIMPLIFIED SCHEMATIC DIAGRAM



L 121

TEST CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}amb}$ Thermal resistance junction-ambient	max	175	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, refer to the test circuit unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{8\text{-}12}$ Positive clamp voltage	$V_{s\,(AC)}$ = 220V R_S = 6.8kΩ		12	15	V
$V_{10\text{-}12}$ Negative clamp voltage			12	15	V
$V_{9\text{-}12}$ Sync input threshold			±12		V
$V_{1\text{-}12}$ Ramp discharge level				1.2	V
$V_{1\text{-}12}$ Ramp maximum level		5			V

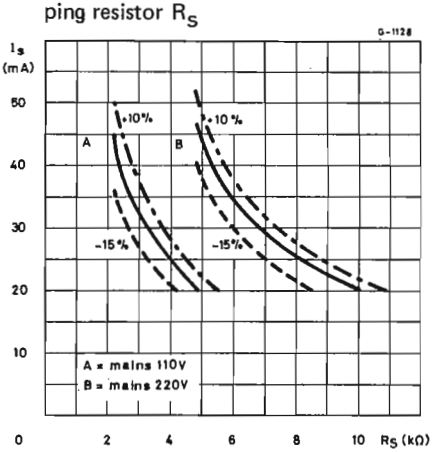
ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{1-2}	Comparator differential trigger level	$V_{6-13} = 8V$		70	100	mV
V_{1-13}, V_{2-13}	Comparator voltage range	$V_{6-13} = 8V$	0		7	V
G_v	Amplifier large signal voltage gain (open loop)	V_2 (peak to peak) = 6V $V_{6-13} = 8V$ $R_{2-13} = 10k\Omega$	60	70		dB
→ ΔV_{2-13}	Amplifier output voltage swing	$V_{6-13} = 8V$ $R_{2-13} = 20k\Omega$	5.5			V
V_{3-13}, V_{5-13}	Input offset voltage	$V_{6-13} = 8V$ $R_{3-13} = R_{5-13} = 50\Omega$		3	6	mV
I_b	Input bias current	$V_{6-13} = 8V$		0.1	1	μA
V_{3-5}	Amplifier differential input voltage				±7	V
V_{3-13}, V_{5-13}	Amplifier input voltage range		0		8	V
CMRR	Common mode rejection ratio	$V_{6-13} = 8V$ $R_{3-13} = R_{5-13} \leqslant 1k\Omega$		60		dB
V_{6-13}	Regulator output voltage	$V_{s\,(AC)} = 220V$ $R_S = 6.8k\Omega$	7.5		8.7	V
I_6	Regulator output current	$V_{s\,(AC)} = 220V$ $R_S = 6.8k\Omega$ $C_8 = 250\mu F$			3	mA
$\frac{\Delta V_6}{V_6}$	Load regulation	$V_{s\,(AC)} = 220V$ $I_6 = 0$ to 2mA $R_S = 6.8k\Omega$ $C_8 = 250\mu F$		0.5	1	%
$\frac{\Delta V_6}{\Delta V_8}$	Line regulation	$V_8 = 12$ to $14V$ $I_6 = 0$		46		dB
SVR	Supply voltage rejection	$V_8 = 12V$ $f_{ripple} = 50Hz$ V_{ripple} (peak to peak) = 4V		46		dB

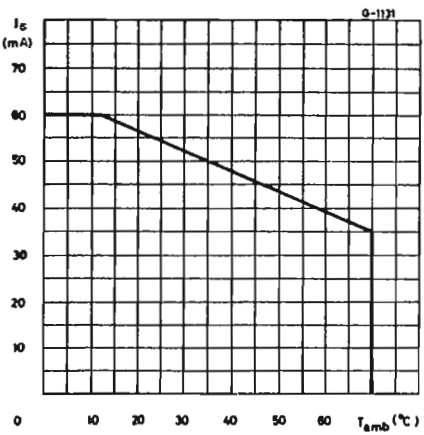
ELECTRICAL CHARACTERISTICS (continued)

	Parameter		Test conditions	Min.	Typ.	Max.	Unit
	V_4	Reference voltage	$V_{s(AC)}$ =220V R_S= 6.8kΩ		1.5		V
→	V_{7-12}	Firing pulse amplitude	$V_{s(AC)}$=220V R_S= 6.8kΩ R_{7-12} = 1kΩ C_8 = 250μF positive negative		 5.5 -9.5		 V V
	I_7	Maximum output current	$V_{s\ (AC)}$= 220V R_S=6.8kΩ R_{7-12} = 10Ω C_8=250μF	80			mA
	t_{pw}	Output pulse width	$V_{s\ (AC)}$= 220V R_S=6.8kΩ		200		μs
	t_r	Output pulse rise time	R_{7-12} = 50Ω C_8 =250μF C_{11-15} = 10 nF		200		ns
	I_F	Unijunction firing current	V_{6-12} = 8V		20		μA
	I_H	Unijunction holding current			200		μA
→	R_{16}	Resistor value to operate ramp oscillator			100		kΩ

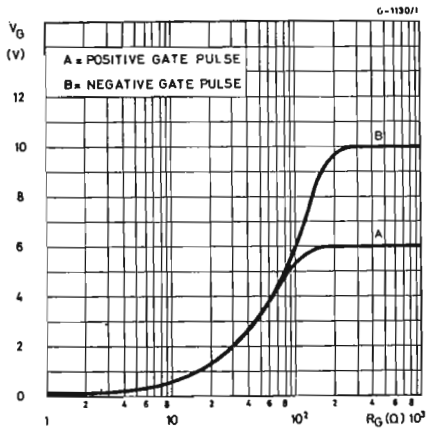
Typical average supply current vs.dropping resistor R_S



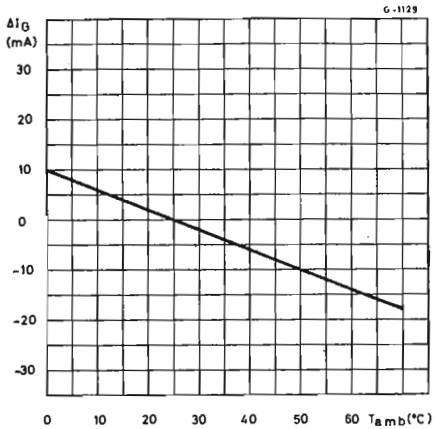
Maximum allowable average supply current vs.ambient temperature



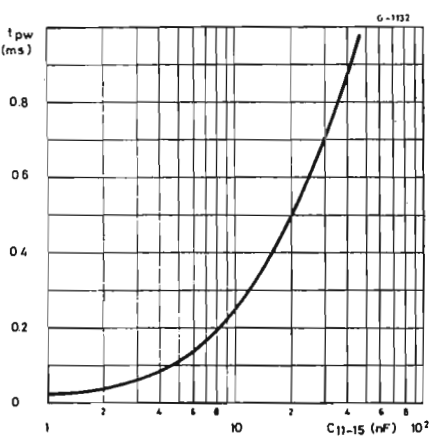
Typical gate pulse amplitude vs. gate resistance



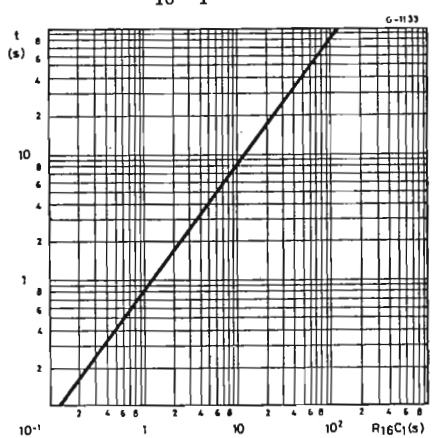
Typical gate current variation vs. ambient temperature



Typical gate pulse width vs. C_{11-15}

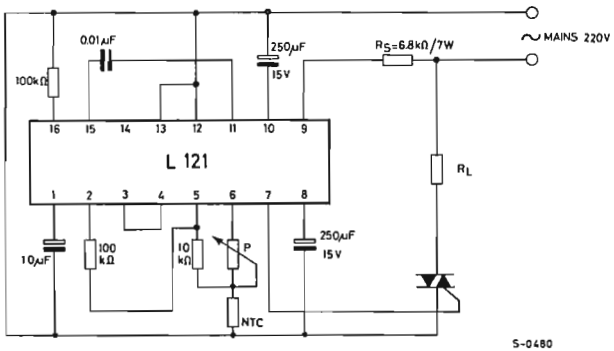


Typical ramp width vs. external time constant R_{16} C_1

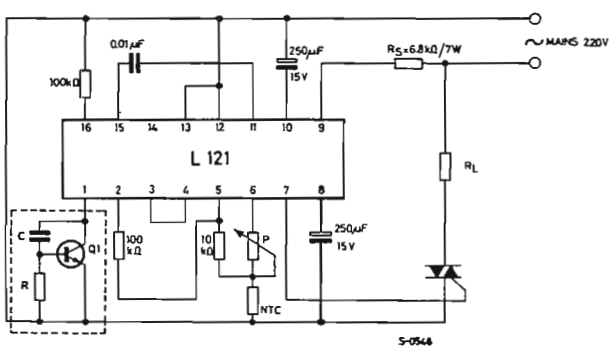


APPLICATION INFORMATION

Typical application circuit



Circuit diagram to increase time base with the use of low value capacitors.

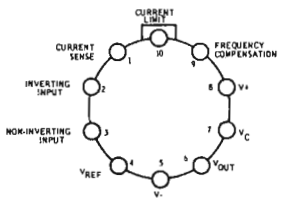


precision voltage regulator

EXTENDED TEMPERATURE RANGE -55°C to +125°C

- **Positive or negative supply operation**
- **Series, shunt, switching or floating operation**
- **.01% line and load regulation**
- **Output voltage adjustable from 2 to 37 volts**
- **Output current to 150 mA without external pass transistor**

CONNECTION DIAGRAM
Top view



NOTE : PIN 5 IS CONNECTED TO CASE

ORDERING NUMBER

L123T2

The L123 is a monolithic voltage regulator constructed on a single silicon chip using the Planar-epitaxial process. The device consists of a temperature compensated reference amplifier, error amplifier, power series pass transistor and current limit circuitry. Additional NPN or PNP pass elements may be used when output currents exceeding 150 mA are required. Provisions are made for adjustable current limiting and remote shutdown. In addition to the above, the device features low standby current drain, low temperature drift and high ripple rejection. The L123 is intended for use with positive or negative supplies as a series, shunt, switching or floating regulator. Applications include laboratory power supplies, isolation regulators for low level data amplifiers, logic card regulators, small instrument power supplies, airborne systems and other power supplies for digital and linear circuits.

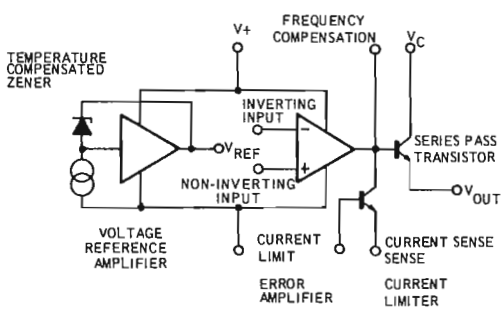
ABSOLUTE MAXIMUM RATINGS

(above which the useful life may be impaired)

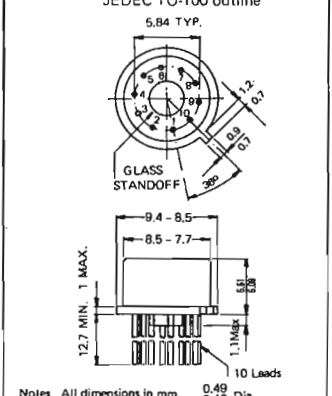
Pulse Voltage from V^+ to V^- (50 msec)	50V
Continuous Voltage from V^+ to V^-	40V
Input-Output Voltage Differential	40V
Maximum Output Current	150 mA
Current from V_{REF}	15 mA
Internal Power Dissipation (Note 1)	800 mW
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

NOTES : On the following page.

EQUIVALENT CIRCUIT



PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-100 outline



ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER (see definitions)	CONDITIONS	Min.	Typ.	Max.	UNITS
Line Regulation	V_{IN} = 12 V to V_{IN} = 15 V		0.01	0.1	% V_{OUT}
	V_{IN} = 12 V to V_{IN} = 40 V		0.02	0.2	% V_{OUT}
	-55°C ≤ T_A ≤ +125°C, V_{IN} = 12 V to V_{IN} = 15V			0.3	% V_{OUT}
Load Regulation	I_L = 1 mA to I_L = 50 mA		0.03	0.15	% V_{OUT}
	55°C ≤ T_A ≤ +125°C, I_L = 1 mA to I_L = 50 mA			0.6	% V_{OUT}
Ripple Rejection	f = 50 Hz to 10 kHz, C_{REF} = 0		74		dB
	f = 50 Hz to 10 kHz, C_{REF} = 5 μF		86		dB
Average Temperature Coefficient of Output Voltage	-55°C ≤ T_A ≤ +125°C		0.002	0.015	%/°C
Short Circuit Current Limit	R_{SC} = 10 Ω, V_{OUT} = 0		65		mA
Reference Voltage		6.95	7.15	7.35	V
Output Noise Voltage	BW = 100 Hz to 10 kHz, C_{REF} = 0		20		μV_{rms}
	BW = 100 Hz to 10 kHz, C_{REF} = 5 μF		2.5		μV_{rms}
Long Term Stability			0.1		% /1000 hrs
Standby Current Drain	I_L = 0, V_{IN} = 30V		2.3	3.5	mA
Input Voltage Range		9.5		40	V
Output Voltage Range		2		37	V
Input-Output Voltage Differential		3		38	V

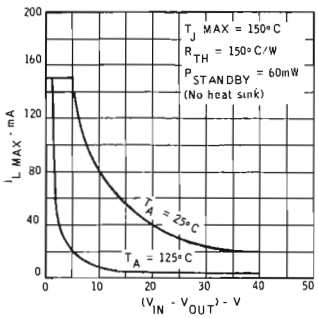
DEFINITION OF TERMS

LINE REGULATION – The percentage change in output voltage for a specified change in input voltage.
LOAD REGULATION – The percentage change in output voltage for a specified change in load current.
RIPPLE REJECTION – The ratio of the peak to peak input ripple voltage to the peak to peak output ripple voltage.
AVERAGE TEMPERATURE COEFFICIENT OF OUTPUT VOLTAGE – The percentage change in output voltage for a specified change in ambient temperature.
SHORT CIRCUIT CURRENT LIMIT – The output current of the regulator with the output shorted to the negative supply.
REFERENCE VOLTAGE- The output of the reference amplifier measured with respect to the negative supply.
OUTPUT NOISE VOLTAGE – The rms output noise voltage with constant load and no input ripple.
STANDBY CURRENT DRAIN – The supply current drawn by the regulator with no output load and no reference voltage load.
INPUT VOLTAGE RANGE – The range of supply voltage over which the regulator will operate.
OUTPUT VOLTAGE RANGE – The range of output voltage over which the regulator will operate.
INPUT-OUTPUT VOLTAGE DIFFERENTIAL – The range of voltage difference between the supply voltage and the regulated output voltage over which the regulator will operate.
SENSE VOLTAGE – The voltage between current sense and current limit terminals necessary to cause current limiting.
TRANSIENT RESPONSE – The closed-loop step function response of the regulator under small-signal conditions.

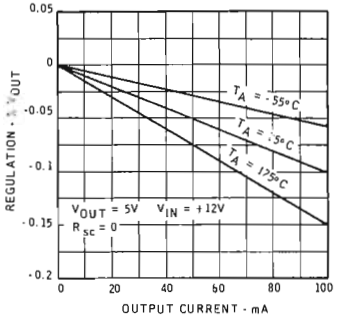
NOTES :
(1) Derate linearly at 6.4 mW/°C for operation at ambient temperatures above 25°C.
(2) Unless otherwise specified, T_A = 25°C, V_{IN} = V^+ = V_C = 12V, V^- = 0, V_{OUT} = 5V, I_L = 1 mA, R_{SC} = 0, C_1 = 100 pF C_{REF} = 0 and divider impedance as seen by error amplifier ≤ 10 KΩ connected as shown in Fig. 1.
(3) L_1 is 40 turns of # 20 enameled copper wire wound on Ferroxcube P36/22-3B7 pot core or equivalent with 0.009" air gap.
(4) Figures in parentheses may be used if R_1/R_2 divider is placed on opposite of error amp.
(5) Replace R_1/R_2 in figures with divider shown in figure 13.
(6) V^+ must be connected to a +3 V or greater supply.

ELECTRICAL CHARACTERISTICS (25° free air temperature unless otherwise noted)

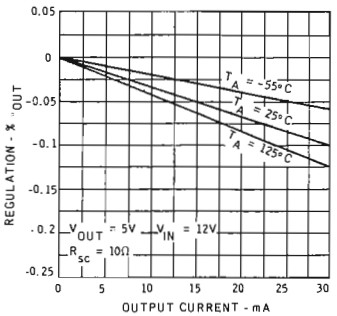
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



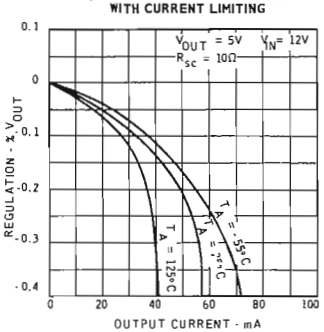
LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING



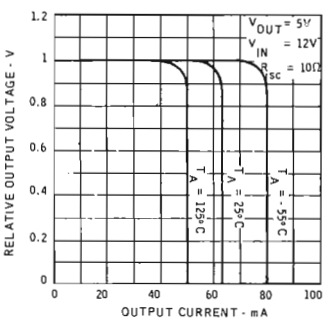
LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING



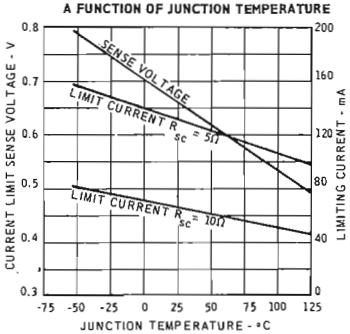
LCAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING



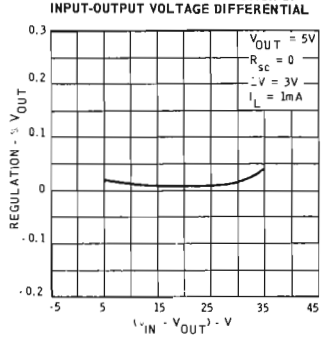
CURRENT LIMITING CHARACTERISTICS



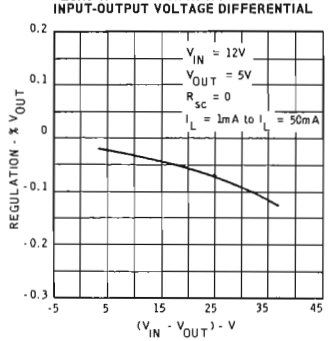
CURRENT LIMITING CHARACTERISTICS AS A FUNCTION OF JUNCTION TEMPERATURE



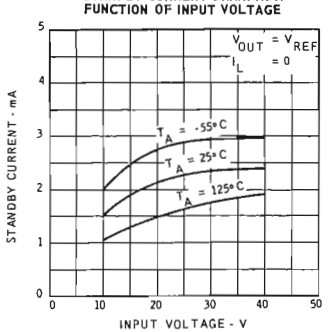
LINE REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



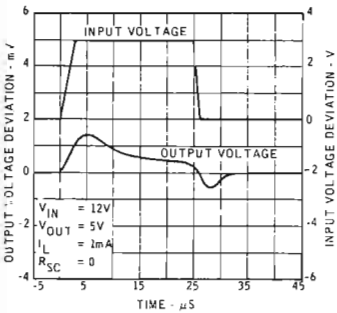
LOAD REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



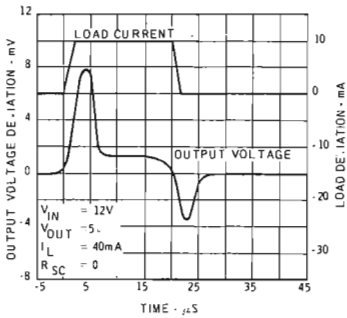
STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE



LINE TRANSIENT RESPONSE



LOAD TRANSIENT RESPONSE



OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY

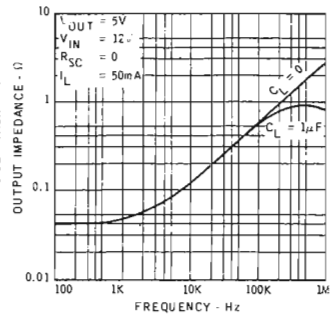


TABLE I

RESISTOR VALUES (kΩ) for standard output voltages

Positive Output Voltage	Applicable Figures	Fixed output ± 5%		Output adjustable ± 10% (Note 5)			Negative Output Voltage	Applicable Figures	Fixed output ± 5%		5% Output adjustable ± 10%		
	(Note 4)	R_1	R_2	R_1	P_1	R_2			R_1	R_2	R_1	P_1	R_2
+ 3	1, 5, 6, 9, 12 (4)	4.12	3.01	1.8	0.5	1.2	+100	7	3.57	102	2.2	10	91
+3.6	1, 5, 6, 9, 12 (4)	3.57	3.65	1.5	0.5	1.5	+250	7	3.57	255	2.2	10	240
+5	1, 5, 6, 9, 12 (4)	2.15	4.99	0.75	0.5	2.2	-6 (note 6)	3, (10)	3.57	2.43	1.2	0.5	0.75
+6	1, 5, 6, 9, 12 (4)	1.15	6.04	0.5	0.5	2.7	-9	3, 10	3.48	5.36	1.2	0.5	2
+9	2, 4, (5, 6, 12, 9)	1.87	7.15	0.75	1	2.7	-12	3, 10	3.57	8.45	1.2	0.5	3.3
+12	2, 4, (5, 6, 9, 12)	4.87	7.15	2	1	3	-15	3, 10	3.65	11.5	1.2	0.5	4.3
+15	2, 4, (5, 6, 9, 12)	7.87	7.15	3.3	1	3	-28	3, 10	3.57	24.3	1.2	0.5	10
+28	2, 4, (5, 6, 9, 12)	21	7.15	5.6	1	2	-45	8	3.57	41.2	2.2	10	33
+45	7	3.57	48.7	2.2	10	39	-100	8	3.57	97.6	2.2	10	91
+ 75	7	3.57	78.7	2.2	10	68	-250	8	3.57	249	2.2	10	240

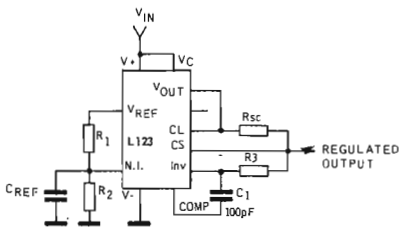
TABLE II

FORMULAE FOR INTERMEDIATE OUTPUT VOLTAGES

Outputs from +2 to +7 volts [Figures 1, 5, 6, 9, 12, (4)] $V_{OUT} = [V_{REF} \times \frac{R_2}{R_1 + R_2}]$	Outputs from +4 to +250 volts [Figure 7] $V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_2 - R_1}{R_1}]$; $R_3 = R_4$	Current Limiting $I_{LIMIT} = \frac{V_{SENSE}}{R_{sc}}$
Outputs from +7 to +37 volts [Figures 2, 4, (5, 6, 9, 12)] $V_{OUT} = [V_{REF} \times \frac{R_1 + R_2}{R_2}]$	Outputs from −6 to −250 volts [Figures 3, 8, 10] $V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_1 + R_2}{R_1}]$; $R_3 = R_4$	Foldback Current Limiting $I_{KNEE} = [\frac{V_{OUT} R_3}{R_{sc} R_4} + \frac{V_{SENSE}(R_3 + R_4)}{R_{sc} R_4}]$ $I_{SHORT\ CKT} = [\frac{V_{SENSE}}{R_{sc}} \times \frac{R_3 + R_4}{R_4}]$

BASIC LOW VOLTAGE REGULATOR FIG. 1

(V_{OUT} = 2 to 7 volts)



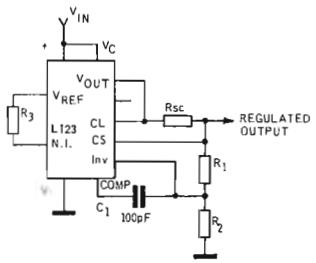
Note: $R3 = \frac{R1\,R2}{R1+R2}$ for minimum temperature drift.

TYPICAL PERFORMANCE

Regulated Output Voltage	5V
Line Regulation (ΔV_{IN} = 3V)	0.5 mV
Load Regulation (ΔI_L = 50mA)	1.5 mV

BASIC HIGH VOLTAGE REGULATOR FIG. 2

(V_{OUT} = 7 to 37 volts)



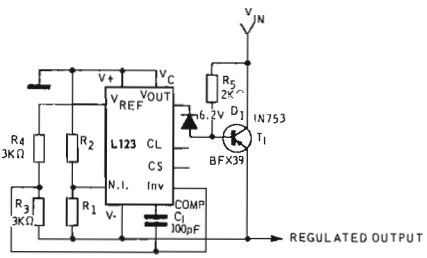
Note: $R3 = \frac{R1\,R2}{R1+R2}$ for minimum temperature drift

R3 may be eliminated for minimum component count.

TYPICAL PERFORMANCE

Regulated Output Voltage	15 V
Line Regulation (ΔV_{IN} = 3V)	1.5 mV
Load Regulation (ΔI_L = 50mA)	4.5 mV

NEGATIVE VOLTAGE REGULATOR FIG. 3

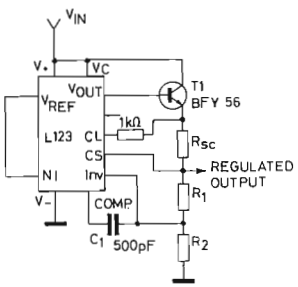


TYPICAL PERFORMANCE

Regulated Output Voltage	-15 V
Line Regulation (ΔV_{IN} = 3V)	1 mV
Load Regulation (ΔI_L = 100mA)	2 mV

POSITIVE VOLTAGE REGULATOR FIG. 4

(External NPN Pass Transistor)

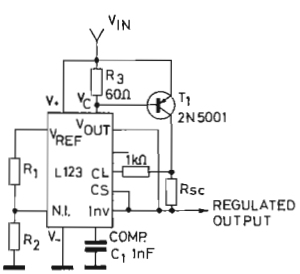


TYPICAL PERFORMANCE

Regulated Output Voltage	+ 15 V
Line Regulation (ΔV_{IN} = 3V)	1.5 mV
Load Regulation (ΔI_L = 1A)	15 mV

POSITIVE VOLTAGE REGULATOR FIG. 5

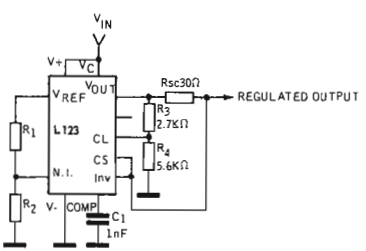
(External PNP Pass Transistor)



TYPICAL PERFORMANCE

Regulated Output Voltage	+ 5 V
Line Regulation (ΔV_{IN} = 3V)	0.5mV
Load Regulation (ΔI_L = 1A)	5mV

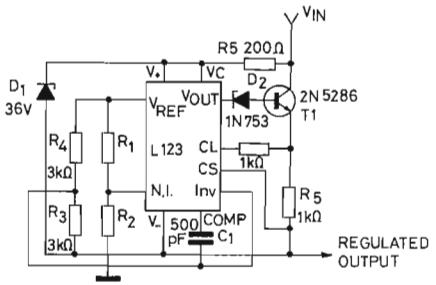
FOLDBACK CURRENT LIMITING FIG. 6



TYPICAL PERFORMANCE

Regulated Output Voltage	+ 5V
Line Regulation (ΔV_{IN} = 3V)	0.5mV
Load Regulation (ΔI_L = 10mA)	1mV
Current Limit Knee	20mA

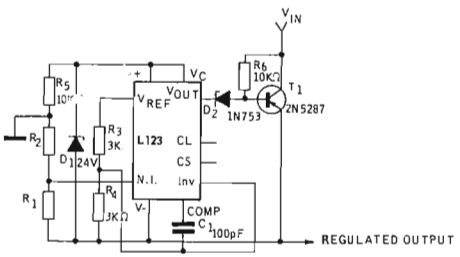
POSITIVE FLOATING REGULATOR FIG. 7



TYPICAL PERFORMANCE

Regulated Output Voltage	+ 50 V
Line Regulation (ΔV_{IN} = 20V)	15 mV
Load Regulation (I_L = 50mA)	20 mV

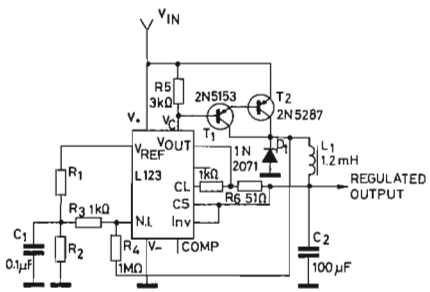
NEGATIVE FLOATING REGULATOR FIG. 8



TYPICAL PERFORMANCE

Regulated Output Voltage	-100V
Line Regulation (ΔV_{IN} = 20V)	20mV
Load Regulation (I_L = 100mA)	20mV

POSITIVE SWITCHING REGULATOR FIG. 9

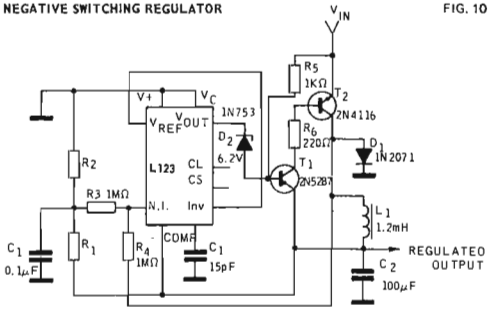


TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation (ΔV_{IN} = 30V)	10 mV
Load Regulation (I_L = 2A)	80 mV

NOTE 3

NEGATIVE SWITCHING REGULATOR FIG. 10

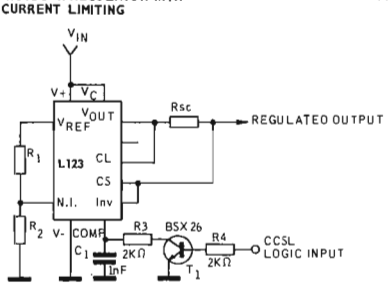


TYPICAL PERFORMANCE

Regulated Output Voltage	-15 V
Line Regulation (ΔV_{IN} = 20V)	8 mV
Load Regulation (I_L = 2A)	6 mV

NOTE 3

REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING FIG. 11

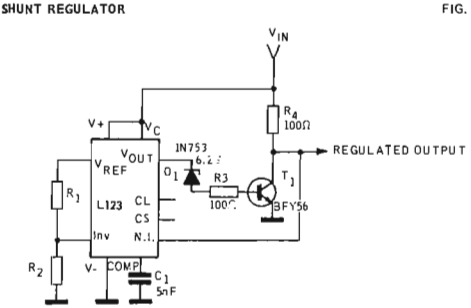


Note :
Current limit transistor may be used for shutdown if current limiting is not required.

TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation (ΔV_{IN} = 3V)	0.5 mV
Load Regulation (I_L = 50mA)	1.5 mV

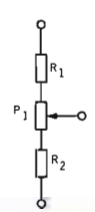
SHUNT REGULATOR FIG. 12



TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation (ΔV_{IN} = 10V)	0.5 mV
Load Regulation (ΔI_{IN} = 100mA)	1.5 mV

OUTPUT VOLTAGE ADJUST FIG. 1

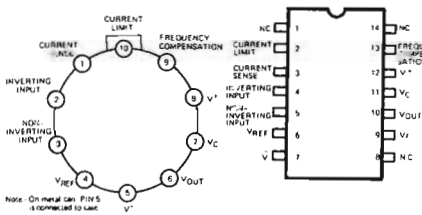


precision voltage regulator

STANDARD TEMPERATURE RANGE, 0°C ÷ 70°C

- Positive or negative supply operation
- Series, shunt, switching or floating operation
- .01 % line and load regulation
- Output voltage adjustable from 2 to 37 volts
- Output current to 150 mA without external pass transistor

CONNECTION DIAGRAM
TOP VIEW



The L 123 is a monolithic voltage regulator constructed on a single silicon chip using the Planar epitaxial process. The device consists of a temperature compensated reference amplifier, error amplifier, power series pass transistor and current limit circuitry. Additional NPN or PNP pass elements may be used when output currents exceeding 150 mA are required. Provisions are made for adjustable current limiting and remote shutdown. In addition to the above, the device features low standby current drain, low temperature drift and high ripple rejection. The L 123 is intended for use with positive or negative supplies as a series, shunt, switching or floating regulator. Applications include laboratory power supplies, isolation regulators for low level data amplifiers, logic card regulators, small instrument power supplies, airborne systems and in other power supplies for digital and linear circuits.

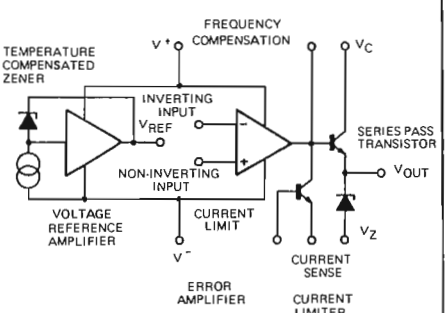
ABSOLUTE MAXIMUM RATINGS (1)

(T_A = 25° C unless otherwise noted)

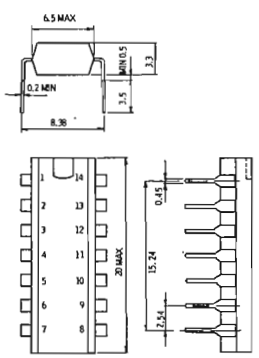
Voltage from V^+ to V^-	40 V
Input-Output Voltage Differential	40 V
Maximum Output Current	150 mA
Current from V_{REF}	25 mA
Internal Power Dissipation (1)	800 mW
Operating Temperature Range	0°C to + 70° C
Storage Temperature Range (Metal Can)	- 65° C to + 150° C
Storage Temperature Range (DIP)	- 55°C to + 125° C
Lead Temperature (Soldering, 60 sec.)	300° C

NOTE ON PAGE 2

EQUIVALENT CIRCUIT

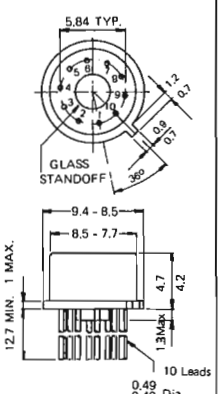


PHYSICAL DIMENSIONS
14-pin plastic DIP



Note : all dimensions in mm.

PHYSICAL DIMENSIONS
similar to
Jedec TO 100 outline



Notes All dimensions in mm.
Leads are gold-plated Kovar.

ORDERING NUMBER

L123 B1 (for TO 116 package)
L123 T1 (for TO 5 package)

ELECTRICAL CHARACTERISTICS (note 2)

PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Line Regulation	V = 12 V to V = 15 V		0.01	0.1	% V_{OUT}
	V_{IN}=12 V to V_{IN} = 40 V		0.1	0.5	% V_{OUT}
	0°C ≤ T_A ≤ 70°C, V_{IN}= 12V to V_{IN}= 15V			0.3	% V_{OUT}
Load Regulation	I_L = 1 mA to I_L = 50 mA		0.03	0.2	% V_{OUT}
	0°C ≤ T_A ≤ 70°C, I_L = 1 mA to I_L = 50 mA			0.6	% V_{OUT}
Ripple Rejection	f = 50 Hz to 10 kHz, C_{REF} = 0		74		dB
	f = 50 Hz to 10 kHz, C_{REF} = 5 μF		86		dB
Average Temperature Coefficient of Output Voltage	0°C ≤ T_A ≤ 70°C		0.003	0.015	%/°C
Short Circuit Current Limit	R_{SC} = 10Ω, V_{OUT} = 0		65		mA
Reference Voltage		6.80	7.15	7.50	V
Output Noise Voltage	BW = 100 Hz to 10 kHz, C_{REF} = 0		20		μV_{rms}
	BW = 100 Hz to 10 kHz, C_{REF} = 5 μF		2.5		μV_{rms}
Long Term Stability			0.1		%/1000 hrs
Standby Current Drain	I_L = 0, V_{IN} = 30 V		2.3	4	mA
Input Voltage Range		9.5		40	V
Output Voltage Range		2		37	V
Input-Output Voltage Differential		3		38	V

DEFINITION OF TERMS

LINE REGULATION - The percentage change in output voltage for a specified change in input voltage.

LOAD REGULATION- The percentage change in output voltage for a specified change in load current.

RIPPLE REJECTION - The ratio of the peak to peak input ripple voltage to the peak to peak output ripple voltage.

AVERAGE TEMPERATURE COEFFICIENT OF OUTPUT VOLTAGE - The percentage change in output voltage for a specified change in ambien temperature.

SHORT CIRCUIT CURRENT LIMIT - The output current of the regulator with the output shorted to the negative supply.

REFERENCE VOLTAGE - The output of the reference amplifier measured with respect to the negative supply.

OUTPUT NOISE VOLTAGE - The rms output noise voltage with constant load and no input ripple.

STANDBY CURRENT DRAIN - The supply current drawn by the regulator with no output load and no reference voltage load.

INPUT VOLTAGE RANGE - The range of supply voltage over which the regulator will operate.

OUTPUT VOLTAGE RANGE - The range of output voltage over which the regulator will operate.

INPUT-OUTPUT VOLTAGE DIFFERENTIAL - The range of voltage difference between the supply voltage and the regulated output voltage over which the regulator will operate.

SENSE VOLTAGE - The voltage between current sense and current limit terminals necessary to cause current limiting.

TRANSIENT RESPONSE - The closed-loop step function response of the regulator under small-signal conditions.

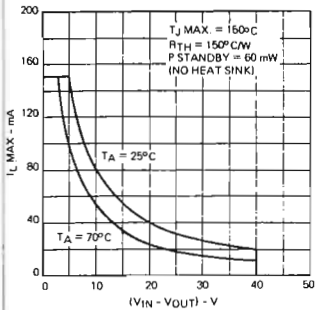
NOTES:

(1) Derate metal can package at 6.4 mW/°C and dual in-line package at 8 mW/°C for operation at ambient temperatures above 25°C.
(2) Unless otherwise specified, T_A = 25°C, V_{IN} = V+ = V_C = 12 V, V- = 0, V_{OUT} = 5 V, I_L = 1 mA, R_{SC} = 0, C_I = 100 pF and divider impedance as seen by the error amplifier ≤ 10 KΩ
(3) For metal can applications where V_Z is required, an external 6.2 zener should be connected in series with V_{OUT}.
(4) Figures in parentheses may be used if R_1/R_2 divider is placed on opposite of error amp.
(5) Replace R_1/R_2 in figures with divider shown in figure 13.
(6) V+ and V_C must be connected to a + 3 V or greater supply.
(7) L_1 is 40 turns of # 20 enameled copper wire wound on Ferroxcube P36/22-3B7 pot core or equivalent with 0,23 mm. air gap.

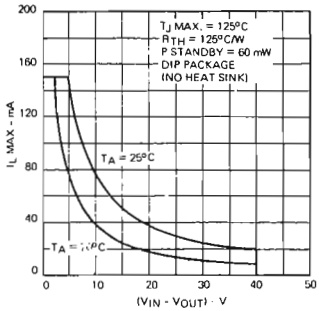
STANDARD TEMPERATURE RANGE

TYPICAL ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

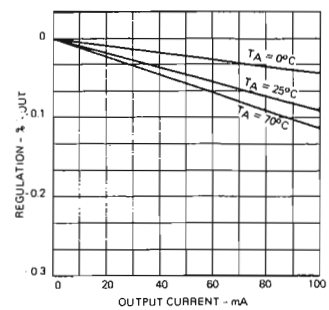
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



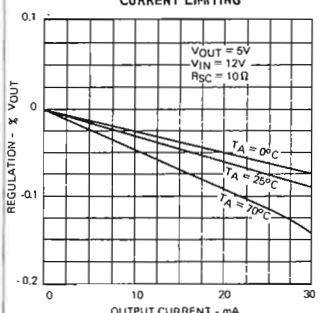
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT - OUTPUT VOLTAGE DIFFERENTIAL



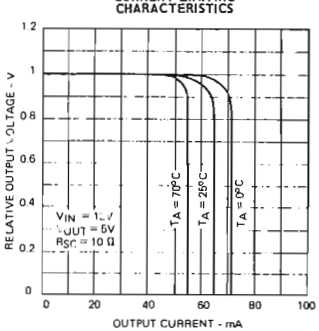
LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING



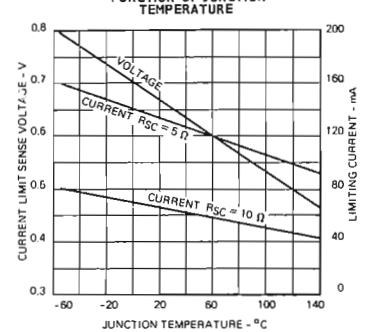
LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING



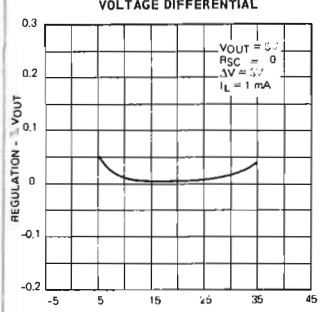
CURRENT LIMITING CHARACTERISTICS



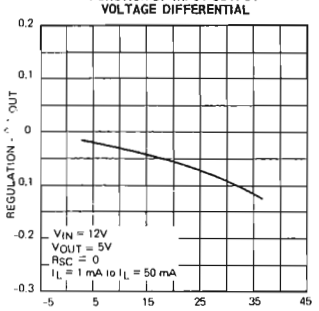
CURRENT LIMITING CHARACTERISTICS AS A FUNCTION OF JUNCTION TEMPERATURE



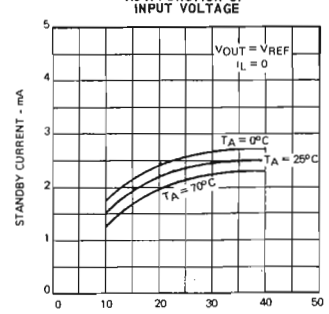
LINE REGULATION AS A FUNCTION OF INPUT - OUTPUT VOLTAGE DIFFERENTIAL



LOAD REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE



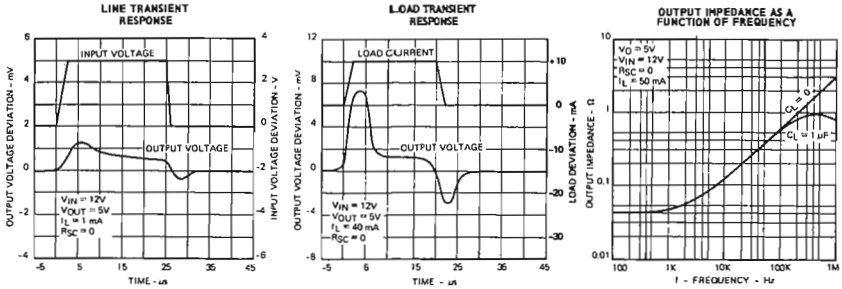


TABLE I
RESISTOR VALUES (KΩ) FOR STANDARD OUTPUT VOLTAGES

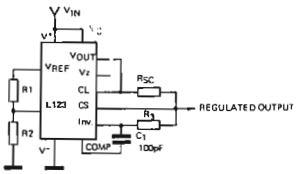
POSITIVE OUTPUT VOLTAGE	APPLICABLE FIGURES	FIXED OUTPUT ±5%		OUTPUT ADJUSTABLE ± 10%(Note 5)			NEGATIVE OUTPUT VOLTAGE	APPLICABLE FIGURES	FIXED OUTPUT ±5%		5% OUTPUT ADJUSTABLE ± 10%		
	(Note 4)	R_1	R_2	R_1	P_1	R_2			R_1	R_2	R_1	P_1	R_2
+ 3	1, 5, 6, 9 12 (4)	4.12	3.01	1.8	0.5	1.2	+ 100	7	3.57	102	2.2	10	91
+ 3.6	1, 5, 6, 9, 12 (4)	3.57	3.65	1.5	0.5	1.5	+ 250	7	3.57	255	2.2	10	240
+ 5	1, 5, 6, 9, 12 (4)	2.15	4.99	0.75	0.5	2.2	- 6 (note 6)	3, (10)	3.57	2.43	1.2	0.5	0.75
+ 6	1, 5, 6, 9, 12 (4)	1.15	6.04	0.6	0.5	2.7	- 9	3, 10	3.48	5.36	1.2	0.5	2
+ 9	2, 4, (5,6, 12, 9)	1.87	7.15	0.75	1	2.7	- 12	3, 10	3.57	8.45	1.2	0.5	3.3
+ 12	2, 4, (5,6, 9, 12)	4.87	7.15	2	1	3	- 15	3, 10	3.65	11.5	1.2	0.5	4.3
+ 15	2,4, (5, 6, 9, 12)	7.87	7.15	3.3	1	3	- 26	3, 10	3.57	24.3	1.2	0.5	10
+28	2, 4, (5, 6, 9, 12)	21	7.15	5.6	1	2	- 45	8	3.57	41.2	2.2	10	33
+45	7	3.57	48.7	2.2	10	39	- 100	8	3.57	97.6	2.2	10	91
+ 76	7	3.57	78.7	2.2	10	68	- 250	8	3.57	249	2.2	10	240

TABLE II
FORMULAE FOR INTERMEDIATE OUTPUT VOLTAGES

Outputs from +2 to +7 volts [Figures 1, 5, 6, 9, 12, (4)] $V_{OUT} = [V_{REF} \times \frac{R_2}{R_1 + R_2}]$	Outputs from +4 to +250 volts [Figure 7] $V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_2 - R_1}{R_1}]$; $R_3 = R_4$	Current Limiting $I_{LIMIT} = \frac{V_{SENSE}}{R_{sc}}$
Outputs from +7 to +37 volts [Figures 2, 4, (5, 6, 9, 12)] $V_{OUT} = [V_{REF} \times \frac{R_1 + R_2}{R_2}]$	Outputs from −6 to −250 volts [Figures 3, 8, 10] $V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_1 + R_2}{R_1}]$; $R_3 = R_4$	Foldback Current Limiting $I_{KNEE} = [\frac{V_{OUT} R_3}{R_{sc} R_4} + \frac{V_{SENSE}(R_3 + R_4)}{R_{sc} R_4}]$ $I_{SHORT\ CKT} = [\frac{V_{SENSE}}{R_{sc}} \times \frac{R_3 + R_4}{R_4}]$

BASIC LOW VOLTAGE REGULATOR FIG. 1

(V_{OUT} = 2 to 7 V)



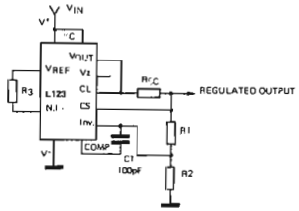
NOTE: $R3 = \frac{R1 \cdot R2}{R1+R2}$ for minimum temperature drift.
R3 may be eliminated for minimum component count.

TYPICAL PERFORMANCE

Regulated output Voltage	5 V
Line Regulation (ΔV_{IN} = 3 V)	0.5mV
Load Regulation (ΔI_L = 50 mA)	1.5mV

BASIC HIGH VOLTAGE REGULATOR FIG. 2

(V_{OUT} = 7 to 37 V)

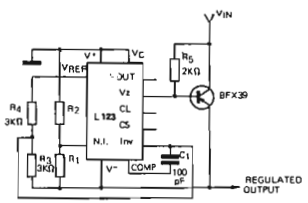


NOTE: $R3 = \frac{R1 \cdot R2}{R1+R2}$ for minimum temperature drift.
R3 may be eliminated for minimum component count.

TYPICAL PERFORMANCE

Regulated Output Voltage	15 V
Line Regulation (ΔV_{IN} = 3V)	1.5mV
Load Regulation (ΔI_L = 50mA)	4.5mV

NEGATIVE VOLTAGE REGULATOR FIG. 3



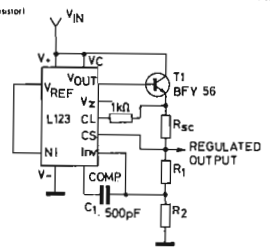
NOTE 3

TYPICAL PERFORMANCE

Regulated Output Voltage	-15 V
Line Regulation (ΔV_{IN} = 3V)	1mV
Load Regulation (ΔI_L = 100mA)	2mV

POSITIVE VOLTAGE REGULATOR FIG. 4

(External NPN Pass Transistor)

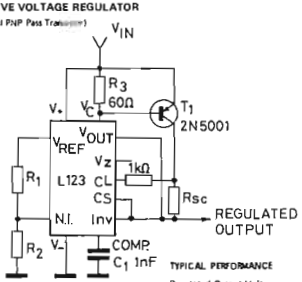


TYPICAL PERFORMANCE

Regulated Output Voltage	+15 V
Line Regulation (ΔV_{IN} = 3V)	1.5mV
Load Regulation (ΔI_L = 1A)	15mV

POSITIVE VOLTAGE REGULATOR FIG. 5

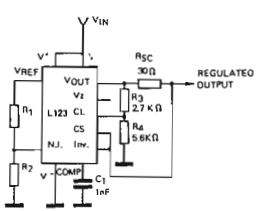
(External PNP Pass Transistor)



TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation (ΔV_{IN} = 3V)	0.5mV
Load Regulation (ΔI_L = 1A)	5mV

FOLDBACK CURRENT LIMITING FIG. 6

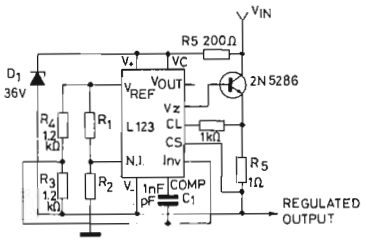


TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation (ΔV_{IN} = 3V)	0.5mV
Load Regulation (ΔI_L = 10mA)	1mV
Current Limit Knee	20mA

POSITIVE FLOATING REGULATOR

FIG. 7



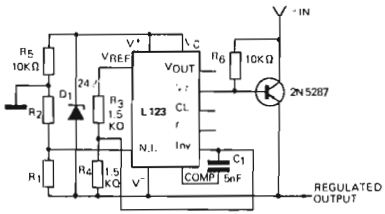
TYPICAL PERFORMANCE

Regulated Output Voltage	+ 100 V
Line Regulation (ΔV_{IN} = 20V)	15 mV
Load Regulation (ΔI_L = 50 mA)	20 mV

NOTE 3

NEGATIVE FLOATING REGULATOR

FIG. 8



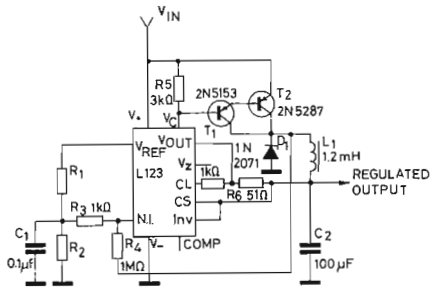
TYPICAL PERFORMANCE

Regulated Output Voltage	- 100 V
Line Regulation (ΔV_{IN} = 20V)	30 mV
Load Regulation (ΔI_L = 100 mA)	20 mV

NOTE 3

POSITIVE SWITCHING REGULATOR

FIG. 9



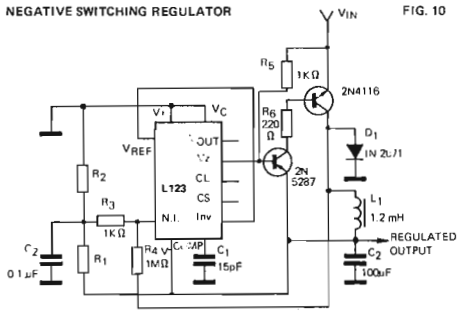
TYPICAL PERFORMANCE

Regulated Output Voltage	+ 5 V
Line Regulation (ΔV_{IN} = 30V)	10 mV
Load Regulation (ΔI_L = 2 A)	80 mV

NOTE 7

NEGATIVE SWITCHING REGULATOR

FIG. 10



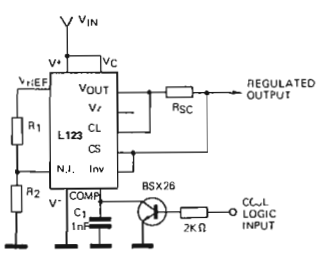
TYPICAL PERFORMANCE

Regulated Output Voltage	- 15 V
Line Regulation (ΔV_{IN} = 20V)	8 mV
Load Regulation (ΔI_L = 2 A)	8 mV

NOTE 3
NOTE 7

REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING

FIG. 11



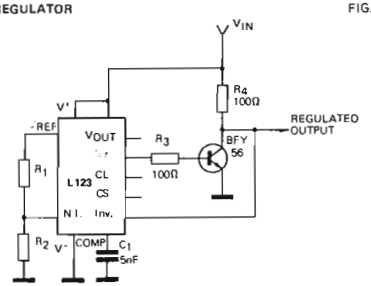
TYPICAL PERFORMANCE

Regulated Output Voltage	5 V
Line Regulation (ΔV_{IN} = 3V)	0.5 mV
Load Regulation (ΔI_L = 50mA)	1.5 mV

NOTE: Current limit transistor may be used for shutdown if current limiting is not required.

SHUNT REGULATOR

FIG. 12



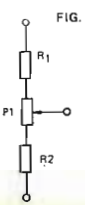
TYPICAL PERFORMANCE

Regulated Output Voltage	+ 5 V
Line Regulation (ΔV_{IN} = 10V)	2 mV
Load Regulation (ΔI_L = 100 mA)	5 mV

NOTE 3

OUTPUT VOLTAGE ADJUST

FIG. 13



LINEAR INTEGRATED CIRCUIT

L 129

PRELIMINARY DATA

5 V VOLTAGE REGULATOR

- OUTPUT CURRENT > 600 mA
- TIGHT TOLERANCE for OUTPUT VOLTAGE
- LOAD REGULATION LESS THAN 1%
- RIPPLE REJECTION 60 dB TYPICAL
- LOW OUTPUT IMPEDANCE
- EXCELLENT TRANSIENT RESPONSE
- HIGH TEMPERATURE STABILITY

The L129 is a silicon monolithic voltage regulator in Jedec TO-126 plastic package which can supply more than 600 mA. It incorporates the following functions :

– internal overload protection

– short-circuit protection

The L129 can be used for voltage regulation in consumer and industrial applications.

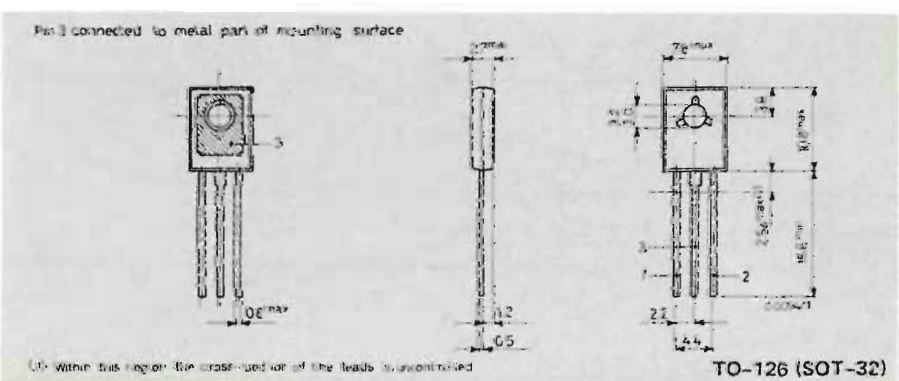
ABSOLUTE MAXIMUM RATINGS

V_I	Input supply voltage	20	V
P_{tot}	Total power dissipation at T_{amb} = 25°C	1.25	W
	at T_{case} = 25°C	14	W
T_{stg}	Storage temperature	- 55 to 125	°C
T_j	Junction temperature	150	°C
T_{op}	Operating temperature	- 20 to 85	°C

ORDERING NUMBER : L 129

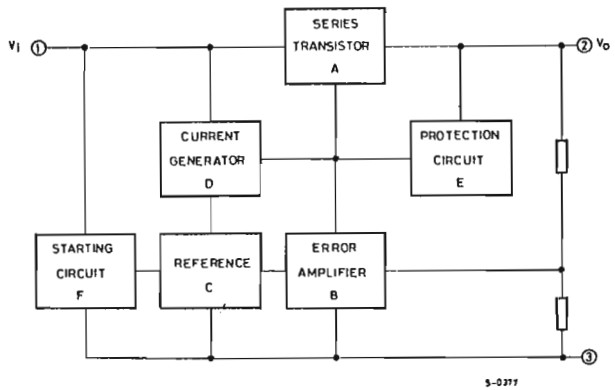
MECHANICAL DATA

Dimensions in mm

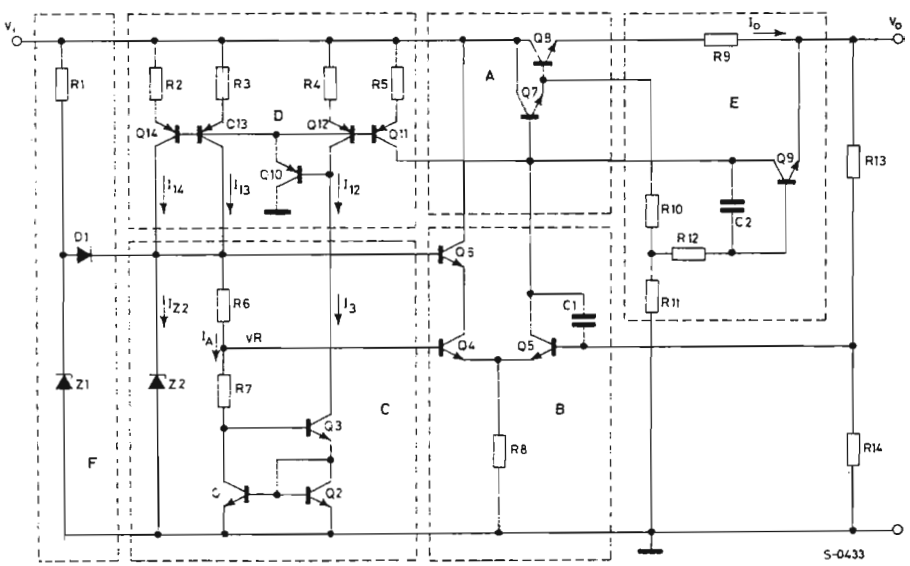


L 129

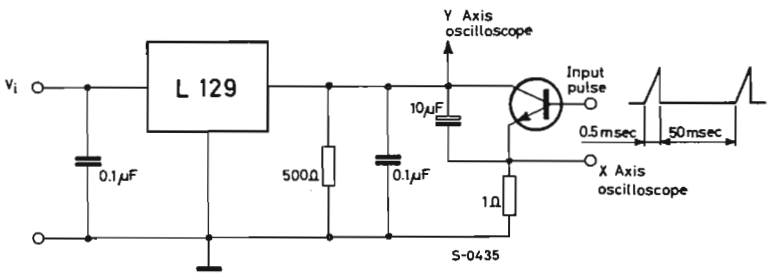
BLOCK DIAGRAM

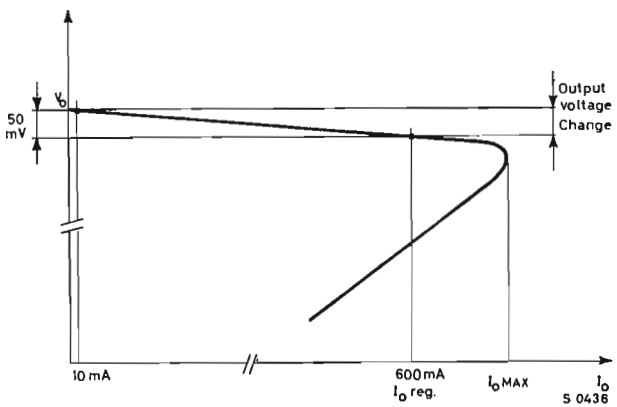


SCHEMATIC DIAGRAM



TEST CIRCUIT with output characteristic





THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	9 °C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100 °C/W

ELECTRICAL CHARACTERISTICS

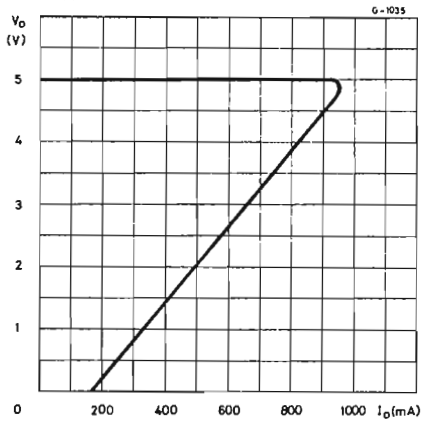
(T_j = 25°C, V_i = 12 V unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_o	Output voltage	7.5V ⩽ V_i ⩽ 20V I_o = 10mA C_L = 10 µF	4.75	5	5.25	V
ΔV_o*	Load regulation	I_o = 10 to 600 mA C_L = 10 µF		0.3	1	%V
I_o*	Regulated output current	$\frac{\Delta V_o}{V_o}$ ⩽ 1%	600	850		mA
I_{oMAX}*	Maximum output current	T_{case} = 25°C T_{case} = 85°C		0.93 1	1.2	A A
I_{sc}	Output short-circuit current	V_o = 0		200	250	mA
I_d	Quiescent drain current	V_i = 20V I_o = 0		9		mA
ΔV_o	Line regulation	V_i = 7.5 to 12V I_o = 10 mA C_L = 10 µF		5	23	mV
$\frac{\Delta V_o}{\Delta T_{amb}}$	Temperature coefficient	I_o = 10mA C_L = 10 µF T_{amb} = - 20 to 85°C		0.5		mV/°C
e_N	Output noise voltage	I_o = 10 mA C_L** = 20 µF B = 10 Hz to 100 kHz		70		µV
R_o	Output resistance	I_o = 600 mA		15		mΩ
SVR	Supply voltage rejection	V_i = 10V I_o = 10mA ΔV_i = 4V peak to peak f = 100 Hz C_L = 10 µF	46	60		dB

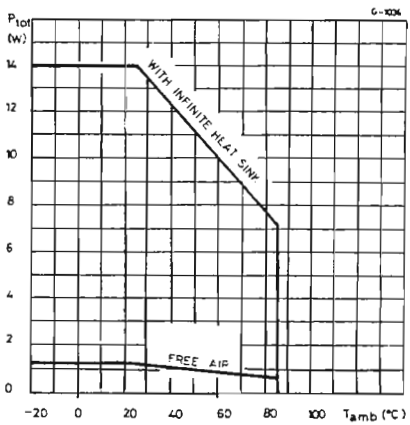
* Refer to the test circuit

** Tantalum capacitor

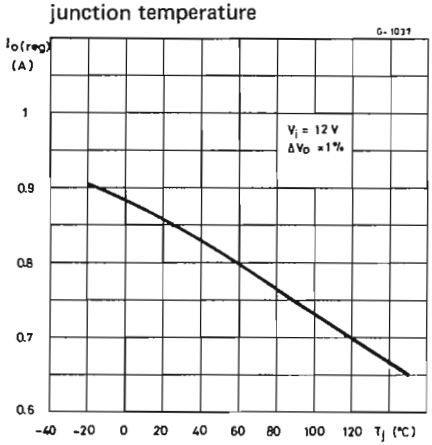
Typical output voltage versus output current



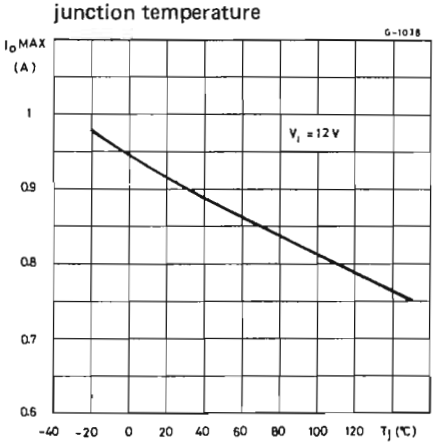
Power rating chart



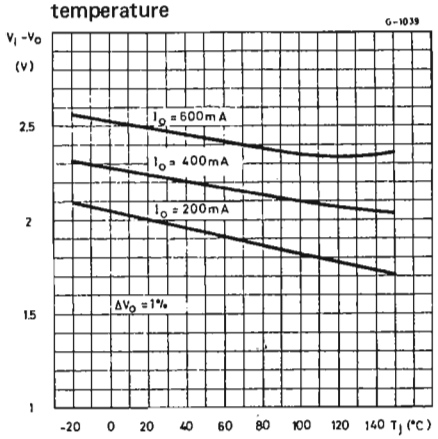
Typical regulated output current versus junction temperature



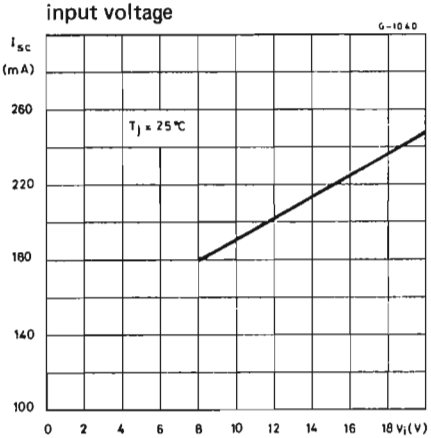
Maximum output current versus junction temperature



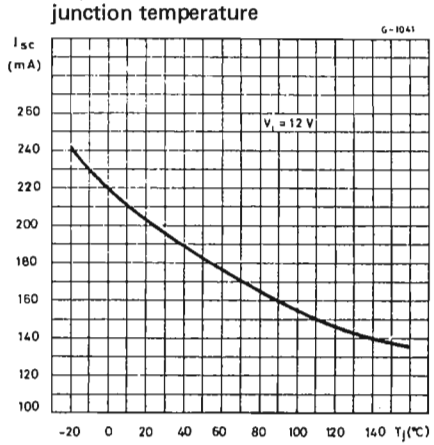
Typical dropout voltage versus junction temperature



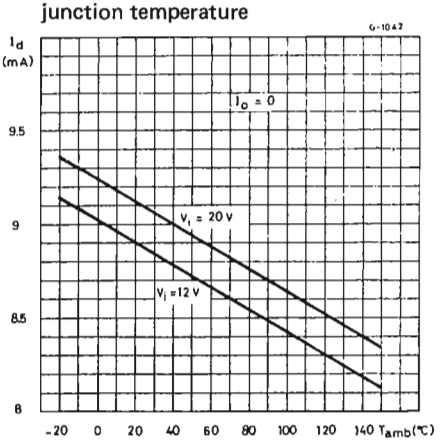
Typical short-circuit current versus input voltage



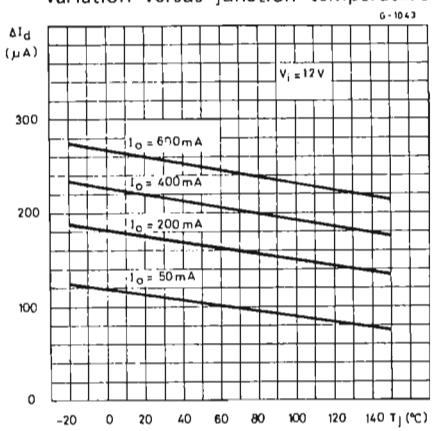
Typical short-circuit current versus junction temperature



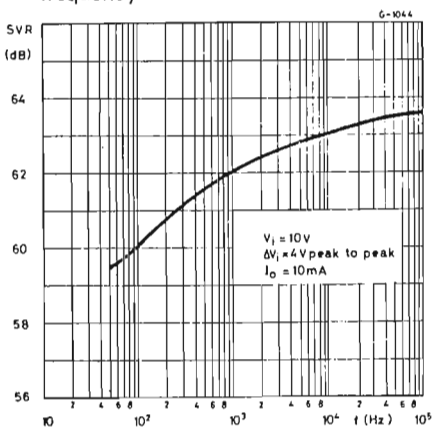
Typical quiescent drain current versus junction temperature



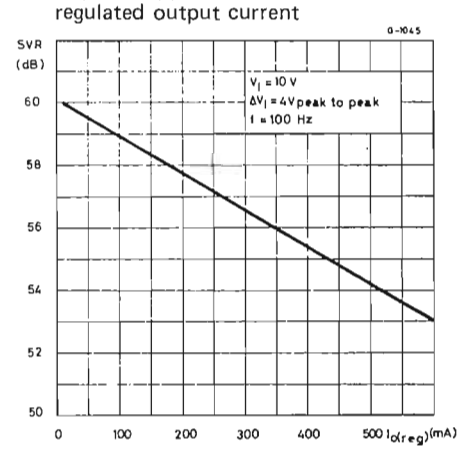
Typical quiescent drain current variation versus junction temperature



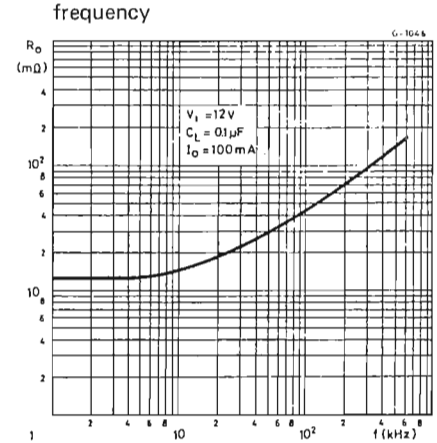
Typical supply voltage rejection versus frequency



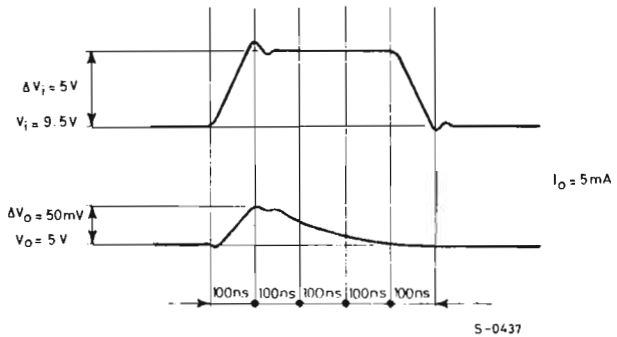
Typical supply voltage rejection versus regulated output current



Typical output resistance versus frequency

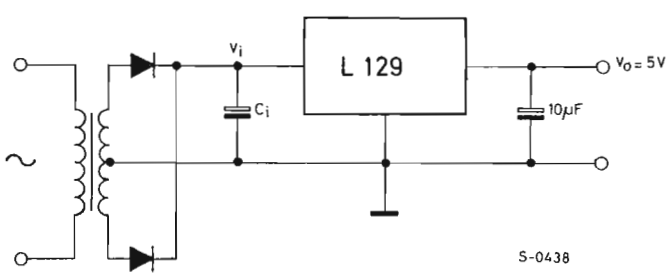


Typical line transient response



APPLICATION INFORMATION

Typical connection circuit



APPLICATION INFORMATION (continued)

Circuit for increasing output voltage

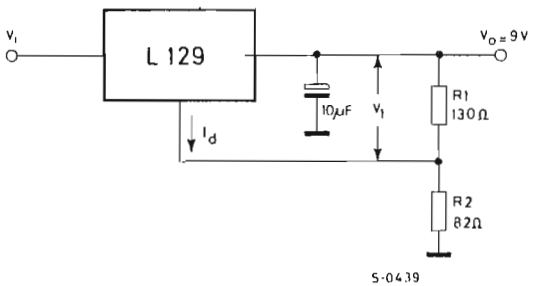
$V_o = V_1 \ (1 + \frac{R2}{R1}) + I_d \cdot R2$

$V_i = 16V$

$I_d = 9\ mA$

$\frac{\delta I_d}{\delta T_{amb}} = -7\ \mu A/°C$ typ.

$\frac{\delta I_d}{\delta V_i} = 30\ \mu A/V$ typ.



Circuit for increasing output current

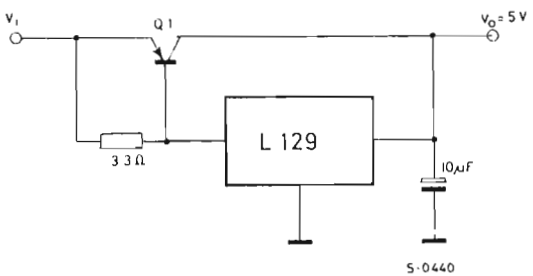
$V_i = 12V$

$I_{oMAX} = 5A$

$R_o \simeq 2m\Omega$

Q1 = PNP transistor

$h_{FEQ1} \geqslant 20$ at $I_{CQ1} = 5A$



Switching regulator with short-circuit protection

$V_o = 5V$

$I_o \leqslant 4A$

$\Delta V_o \simeq 100$ mV peak to peak

$f \simeq 10$ kHz

$\eta = \frac{P_o}{P_i} \simeq 65\%$

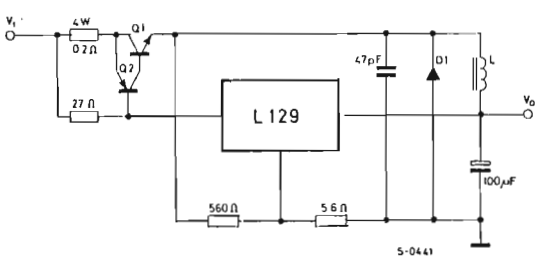
$V_i = 10$ to $20V$

Q1 = BD X 70

Q2 = BC 116

D1 = Diode with $I_{FM} = 5A$

$L \simeq 1.5$ mH



LINEAR INTEGRATED CIRCUIT

L 130

PRELIMINARY DATA

12V VOLTAGE REGULATOR

- OUTPUT CURRENT > 500 mA
- TIGHT TOLERANCE for OUTPUT VOLTAGE
- LOAD REGULATION LESS THAN 1%
- RIPPLE REJECTION 60 dB TYPICAL
- LOW OUTPUT IMPEDANCE
- EXCELLENT TRANSIENT RESPONSE
- HIGH TEMPERATURE STABILITY

The L130 is a silicon monolithic voltage regulator in Jedec TO-126 plastic package which can supply more than 500 mA. It incorporates the following functions :

— internal overload protection
— short-circuit protection.

The L130 can be used for voltage regulation in consumer and industrial applications.

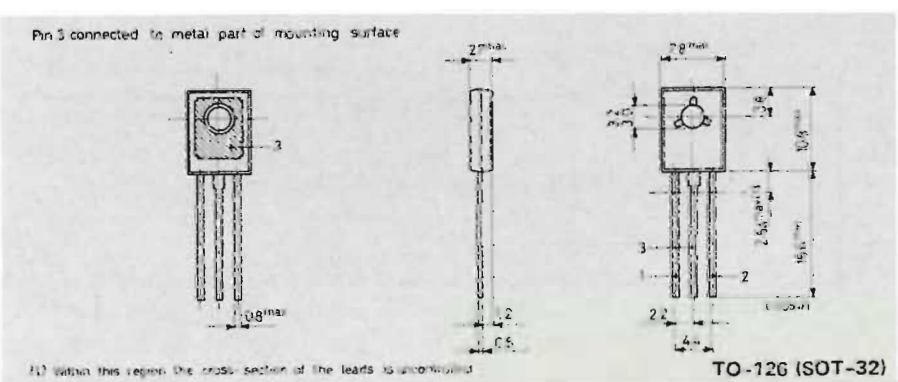
ABSOLUTE MAXIMUM RATINGS

V_i	Input supply voltage	27	V
P_{tot}	Total power dissipation at T_{amb} = 25°C	1.25	W
	at T_{case} = 25°C	14	W
T_{stg}	Storage temperature	-55 to 125	°C
T_j	Junction temperature	150	°C
T_{op}	Operating temperature	-20 to 85	°C

ORDERING NUMBER : L 130

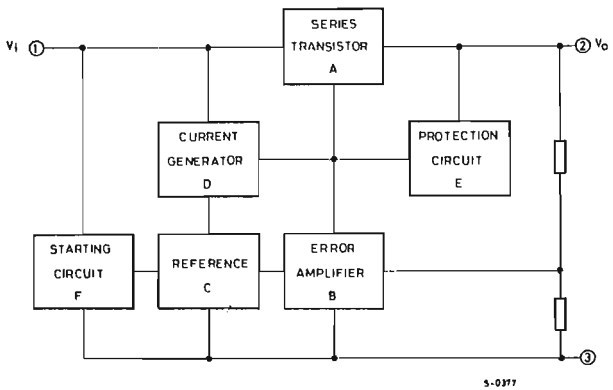
MECHANICAL DATA

Dimensions in mm

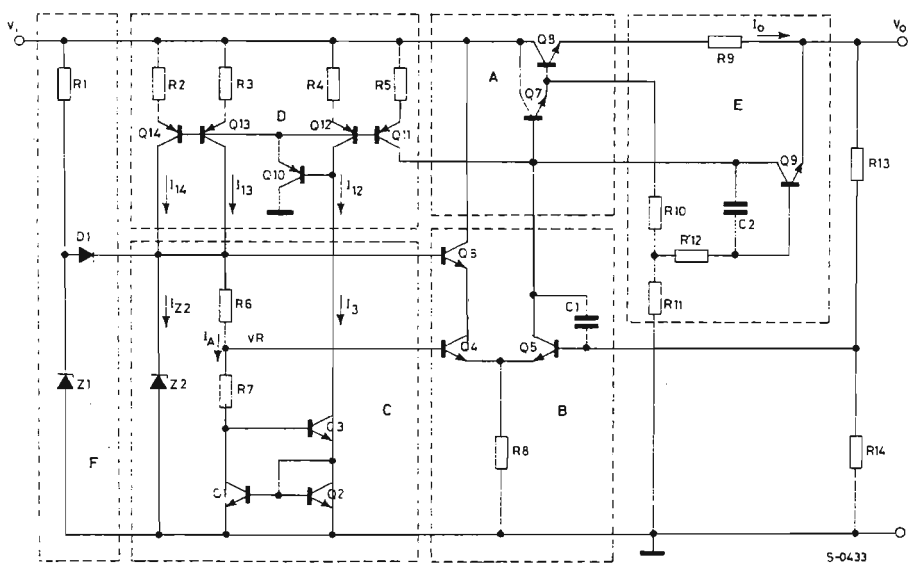


L 130

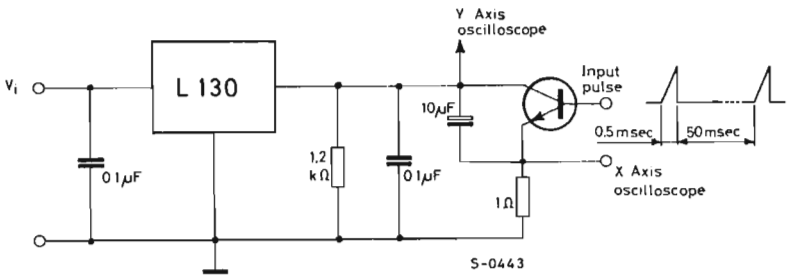
BLOCK DIAGRAM

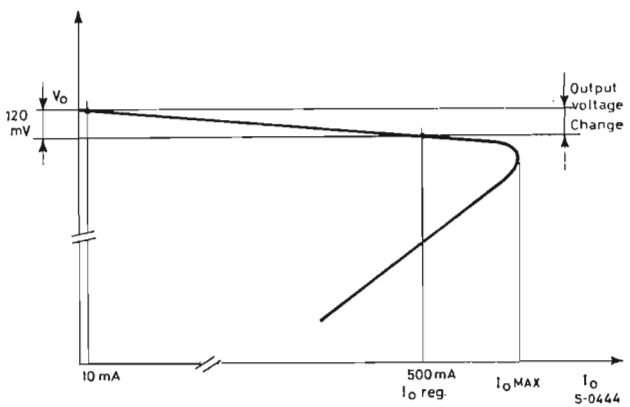


SCHEMATIC DIAGRAM



TEST CIRCUIT with output characteristic





THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	9 °C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100 °C/W

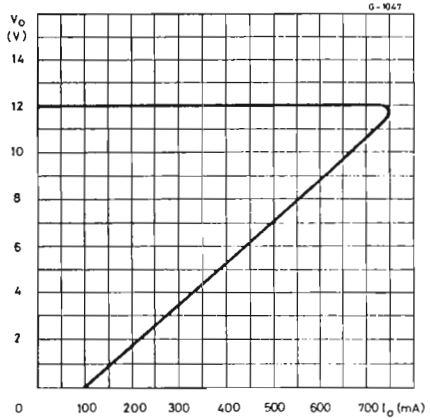
ELECTRICAL CHARACTERISTICS

($T_J = 25°C$, $V_I = 21$ V unless otherwise specified)

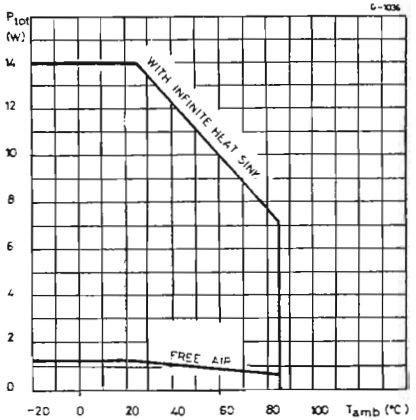
Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_o	Output voltage	$14.5V \leqslant V_i \leqslant 27V$ $I_o = 10mA$ $C_L = 10\ \mu F$	11.4	12	12.6	V
ΔV_o*	Load regulation	$I_o = 10$ to 500mA $C_L = 10\ \mu F$		0.3	1	%V
I_o*	Regulated output current	$\frac{\Delta V_o}{V_o} \leqslant 1\%$	500	720		mA
$I_{o\,MAX}$*	Maximum output current	$T_{case} = 25°C$ $T_{case} = 85°C$		0.75 0.8	1	A A
I_{sc}	Output short-circuit current	$V_o = 0$		100	200	mA
I_d	Quiescent drain current	$V_i = 27V$ $I_o = 0$		10		mA
ΔV_o	Line regulation	$V_i = 14.5$ to 21V $I_o = 10mA$ $C_L = 10\ \mu F$		6	33	mV
$\frac{\Delta V_o}{\Delta T_{amb}}$	Temperature coefficient	$I_o = 10mA$ $C_L = 10\ \mu F$ $T_{amb} = -20$ to 85°C		1.2		mV/°C
e_N	Output noise voltage	$I_o = 10mA$ C_L**$= 20\ \mu F$ B = 10 Hz to 100 kHz		150		μV
R_o	Output resistance	$I_o = 500mA$		20		mΩ
SVR	Supply voltage rejection	$V_i = 19V$ $I_o = 10mA$ $\Delta V_i = 4V$ peak to peak f = 100 Hz $C_L = 10\ \mu F$	46	60		dB

* Refer to the test circuit.
** Tantalum capacitor.

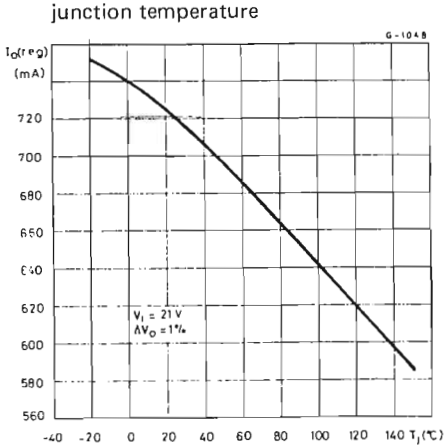
Typical output voltage versus output current



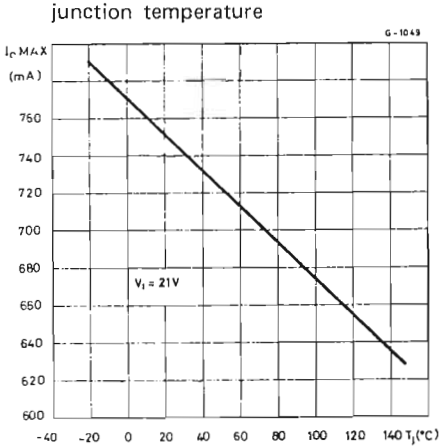
Power rating chart



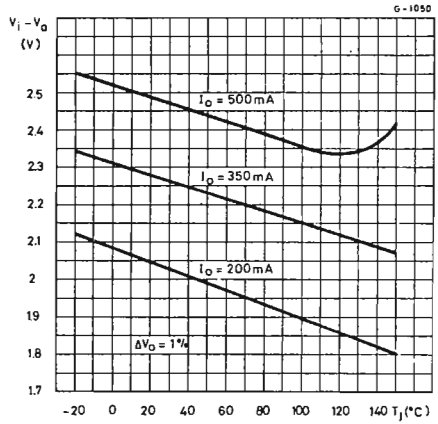
Typical regulated output current versus junction temperature



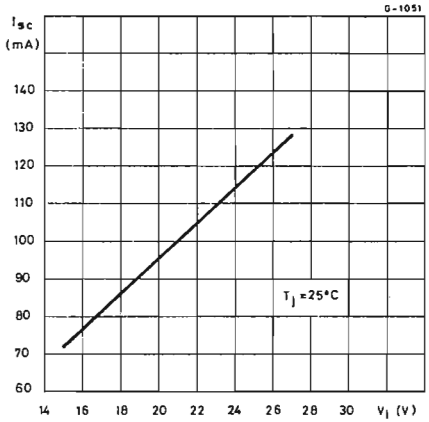
Maximum output current versus junction temperature



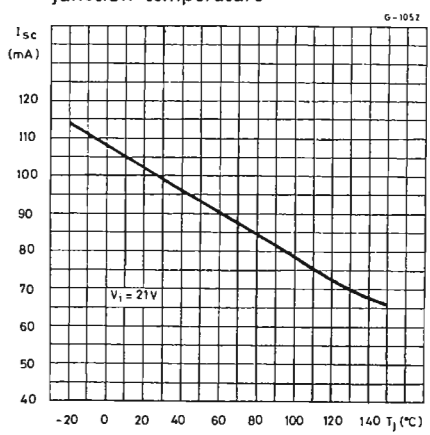
Typical dropout voltage versus junction temperature



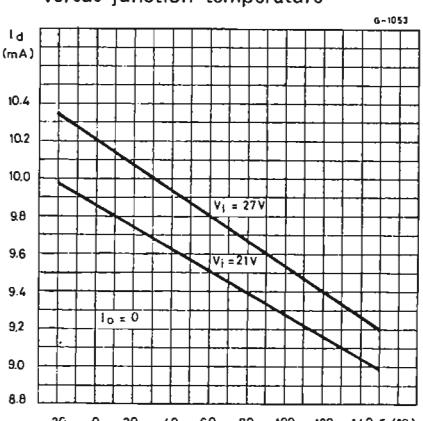
Typical short-circuit current versus input voltage



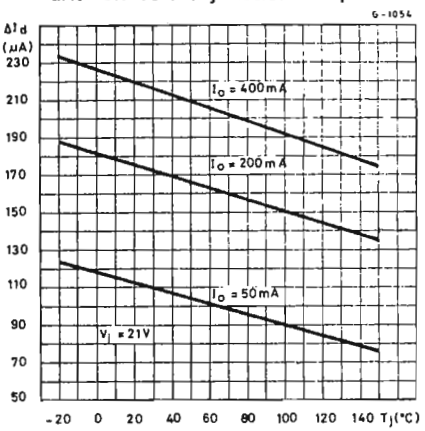
Typical short-circuit current versus junction temperature



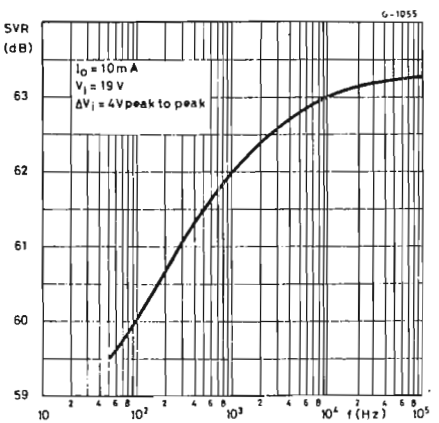
Typical quiescent drain current versus junction temperature



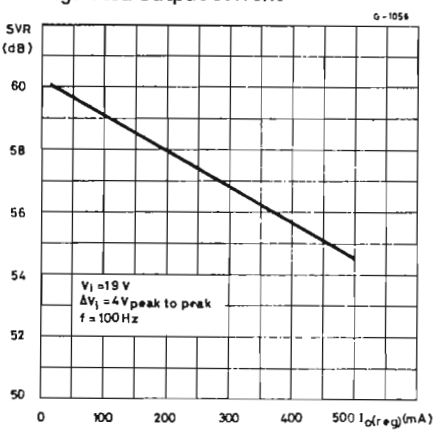
Typical quiescent drain current variation versus junction temperature



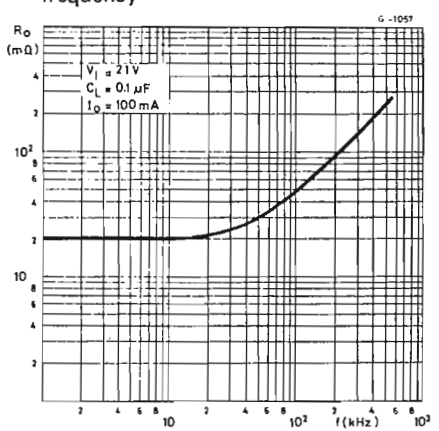
Typical supply voltage rejection versus frequency



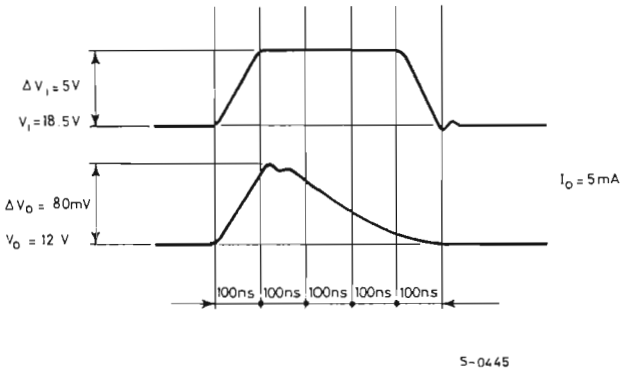
Typical supply voltage rejection versus regulated output current



Typical output resistance versus frequency

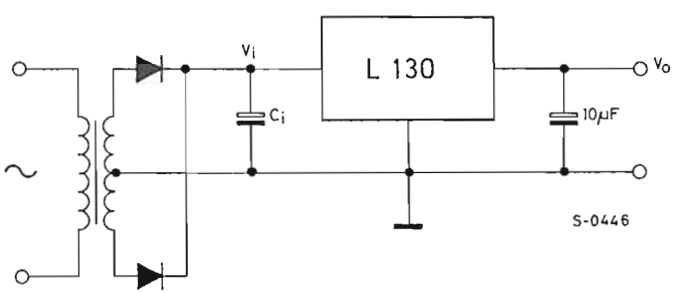


Typical line transient response



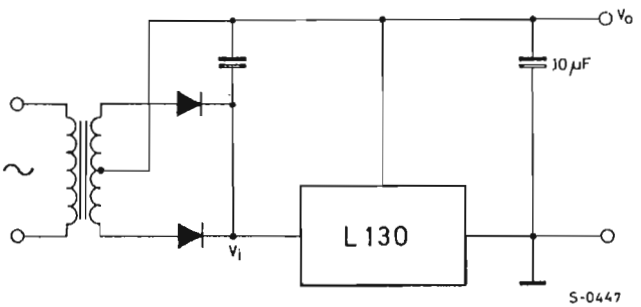
APPLICATION INFORMATION

Typical connection circuit

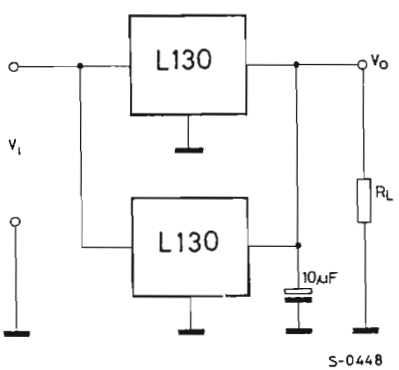


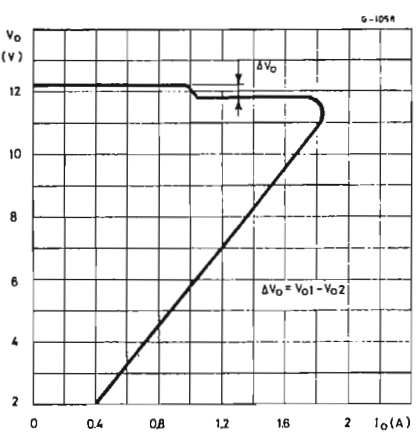
APPLICATION INFORMATION (continued)

Negative output voltage circuit.



Parallel connected voltage regulators and its output characteristics.





LINEAR INTEGRATED CIRCUIT

L 131

PRELIMINARY DATA

15V VOLTAGE REGULATOR

- OUTPUT CURRENT > 450 mA
- TIGHT TOLERANCE for OUTPUT VOLTAGE
- LOAD REGULATION LESS THAN 1%
- RIPPLE REJECTION 56 dB TYPICAL
- LOW OUTPUT IMPEDANCE
- EXCELLENT TRANSIENT RESPONSE
- HIGH TEMPERATURE STABILITY

The L131 is a silicon monolithic voltage regulator in Jedec TO-126 plastic package which can supply more than 450 mA. It incorporates the following functions :
– internal overload protection
– short-circuit protection.
The L131 can be used for voltage regulation in consumer and industrial applications.

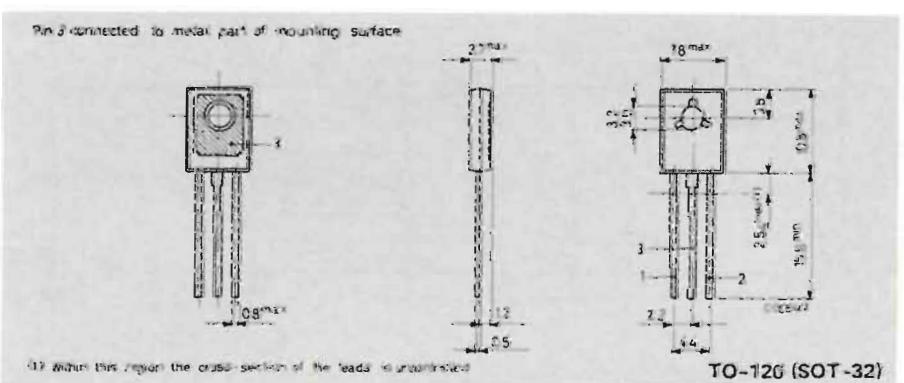
ABSOLUTE MAXIMUM RATINGS

V_i	Input supply voltage		27	V
P_{tot}	Total power dissipation	at $T_{amb} = 25°C$	1.25	W
		at $T_{case} = 25°C$	14	W
T_{stg}	Storage temperature		- 55 to 125	°C
T_j	Junction temperature		150	°C
T_{op}	Operating temperature		- 20 to 85	°C

ORDERING NUMBER : L 131

MECHANICAL DATA

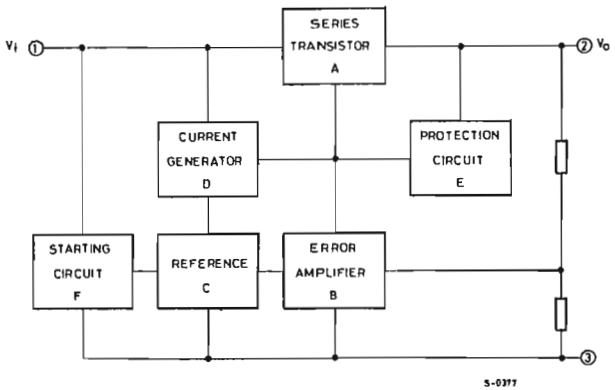
Dimensions in mm



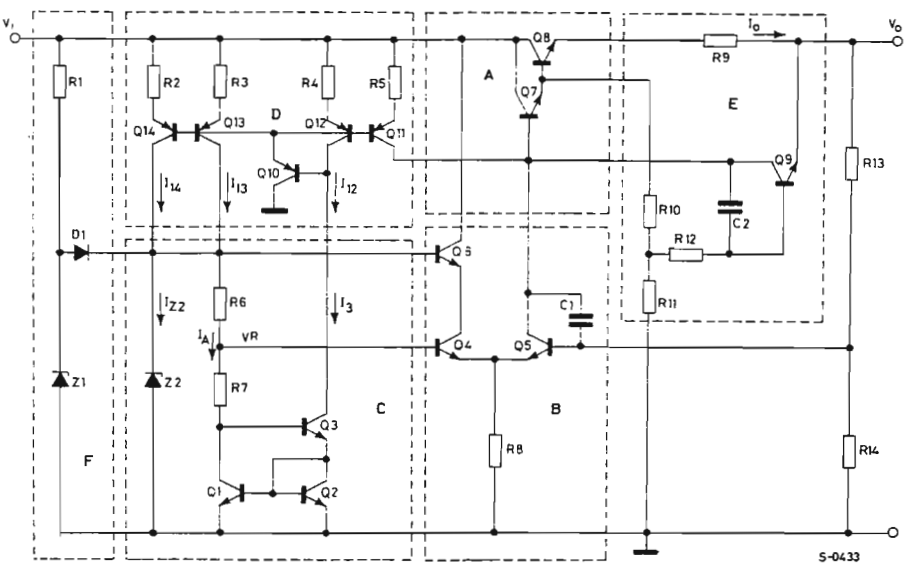
TO-126 (SOT-32)

L 131

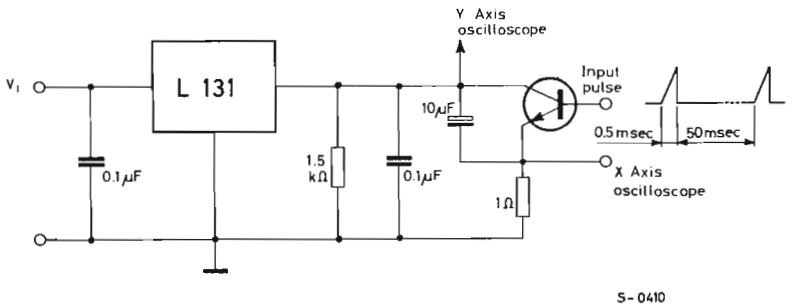
BLOCK DIAGRAM

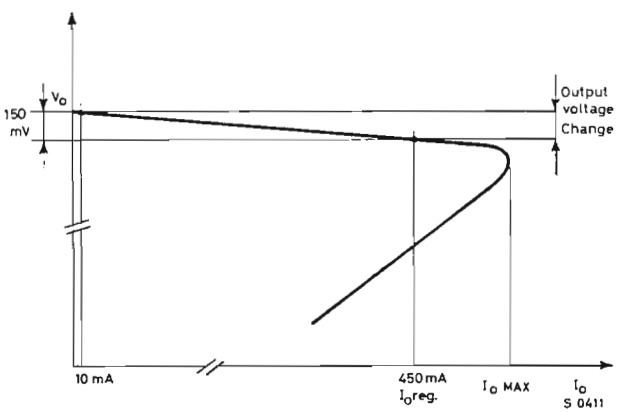


SCHEMATIC DIAGRAM



TEST CIRCUIT with output characteristic





THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	9 °C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100 °C/W

ELECTRICAL CHARACTERISTICS

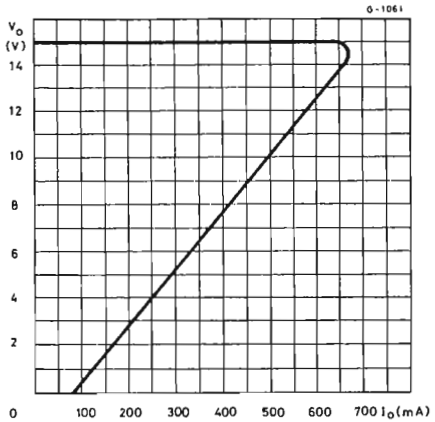
(T_j = 25°C, V_i = 24V unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_o	Output voltage	17.5V ⩽ V_i ⩽ 27V I_o = 10mA C_L = 10 μF	14.25	15	15.75	V
ΔV_o*	Load regulation	I_o = 10 to 450 mA C_L = 10 μF		0.3	1	%V
I_o*	Regulated output current	$\frac{\Delta V_o}{V_o}$ ⩽ 1%	450	600		mA
I_{oMAX}*	Maximum output current	T_{case} = 25°C T_{case} = 85°C		0.68 0.8	0.9	A A
I_{sc}	Output short-circuit current	V_o = 0		85	160	mA
I_d	Quiescent drain current	V_i = 27V I_o = 0		10		mA
ΔV_o	Line regulation	V_i = 17.5 to 24V I_o = 10 mA C_L = 10 μF		6	33	mV
$\frac{\Delta V_o}{\Delta T_{amb}}$	Temperature coefficient	I_o = 10mA C_L = 10 μF T_{amb} = - 20 to 85°C		1.5		mV/°C
e_N	Output noise voltage	I_o = 10 mA C_L** = 20 μF B = 10 Hz to 100 kHz		180		μV
R_o	Output resistance	I_o = 450 mA		60		mΩ
SVR	Supply voltage rejection	V_i = 22V I_o = 10mA ΔV_i = 4V peak to peak f = 100 Hz C_L = 10 μF	46	56		dB

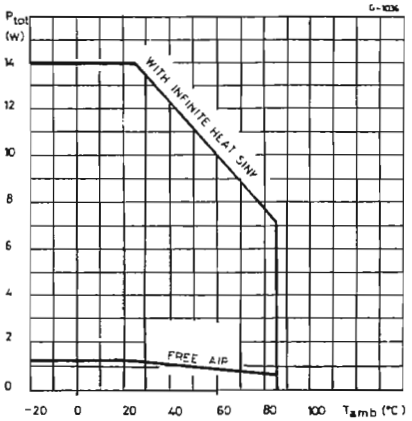
* Refer to the test circuit

** Tantalum capacitor

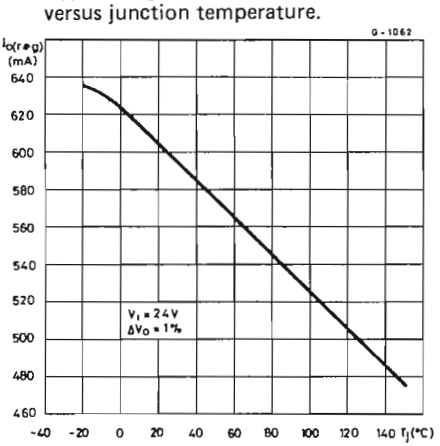
Typical output voltage versus output current.



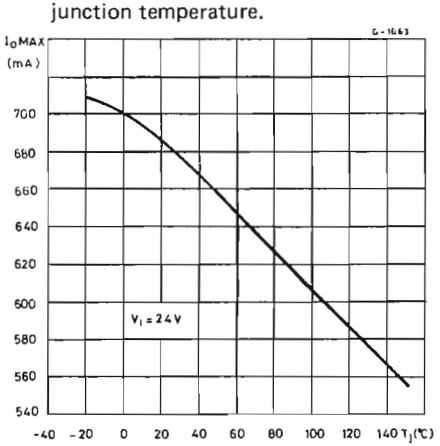
Power rating chart



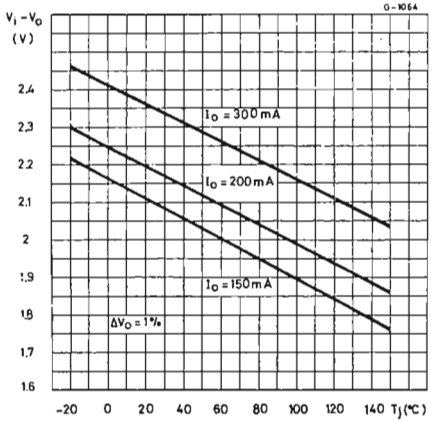
Typical regulated output current versus junction temperature.



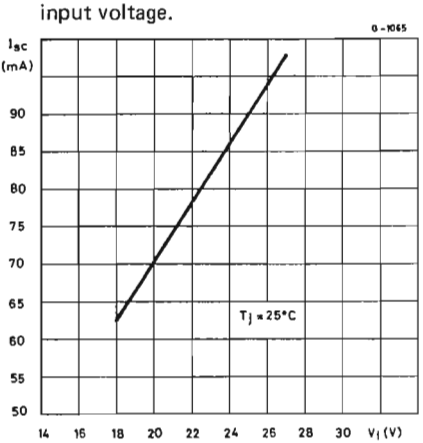
Maximum output current versus junction temperature.



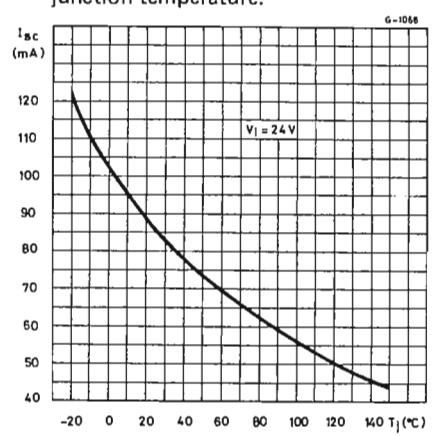
Typical dropout voltage versus junction temperature.



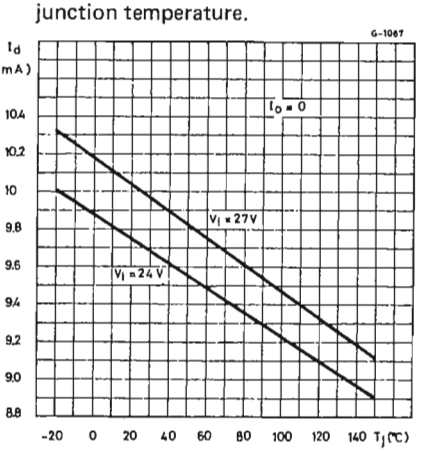
Typical short-circuit current versus input voltage.



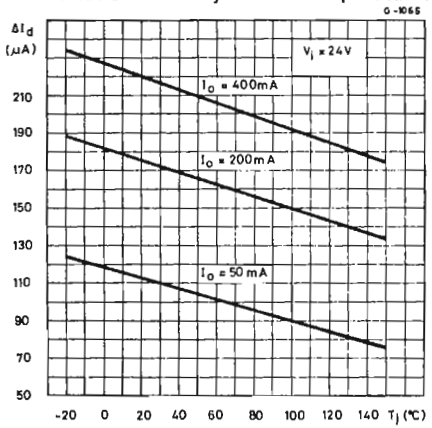
Typical short-circuit current versus junction temperature.



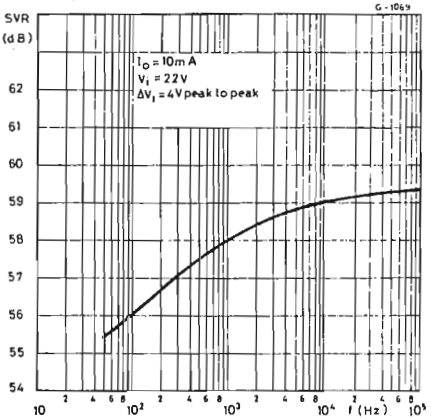
Typical quiescent drain current versus junction temperature.



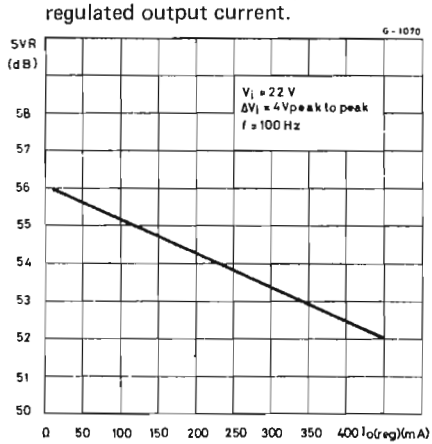
Typical quiescent drain current variation versus junction temperature.



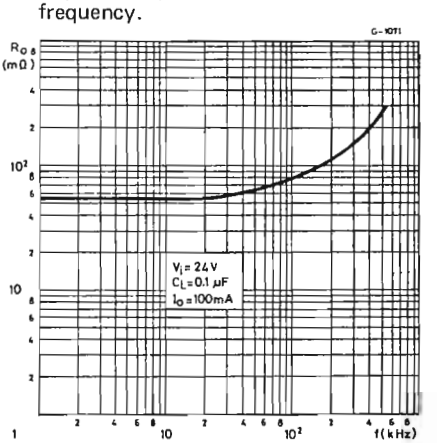
Typical supply voltage rejection versus frequency.



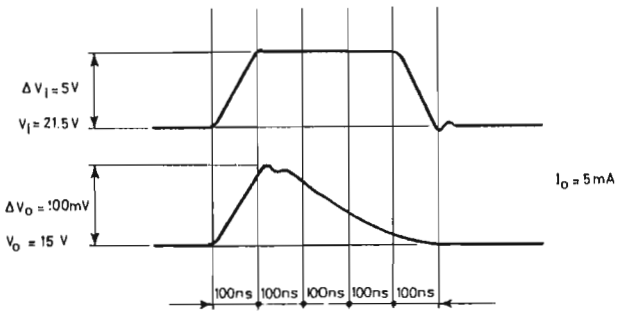
Typical supply voltage rejection versus regulated output current.



Typical output resistance versus frequency.

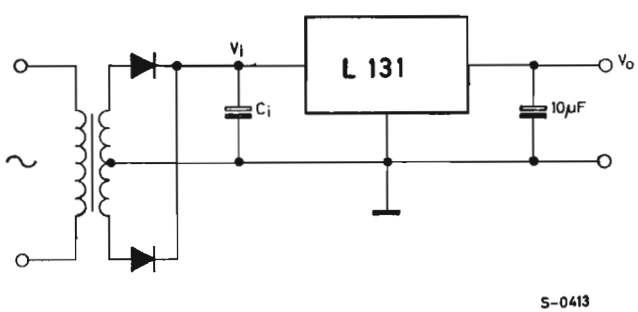


Typical line transient response.



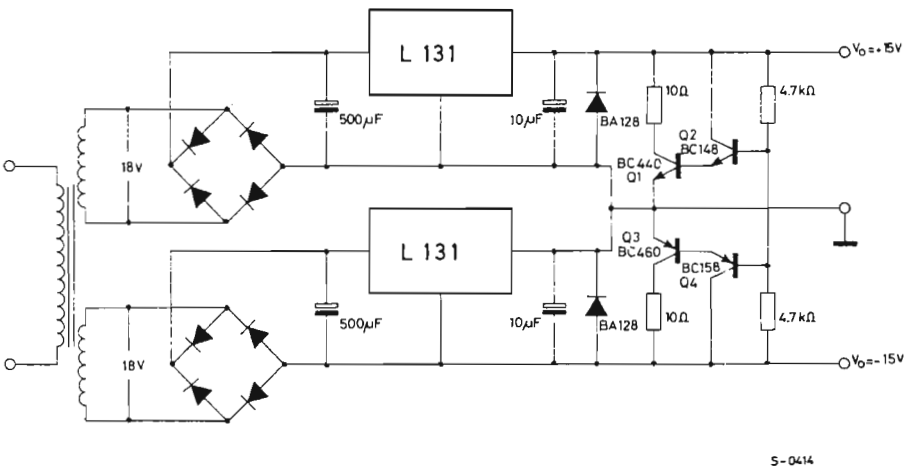
APPLICATION INFORMATION

Typical connection circuit.

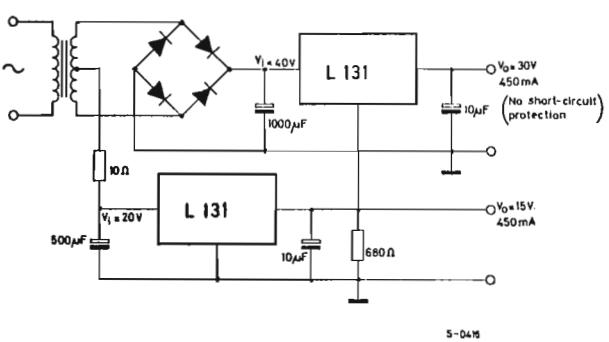


APPLICATION INFORMATION (continued)

Symmetrical ± 15V voltage regulator circuit



Series regulators circuit connection



APPLICATION INFORMATION (continued)

Low consumption circuit to increase output voltage

$$V_o = V_1 \left(1 + \frac{R2}{R1}\right) + V_{BE} \left(1 + \frac{R2}{R1}\right) + \frac{I_d}{h_{FEQ1}} \cdot R2$$

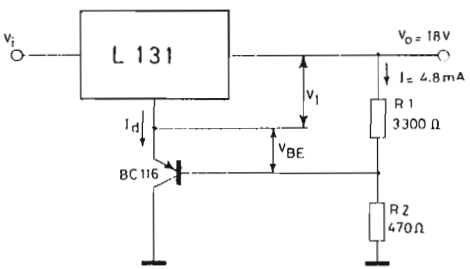
$I_d = 10\ mA$

$V_i = 25V$

$\frac{\delta I_d}{\delta T_{amb}} = -7\ \mu A/°C$ typ.

$\frac{\delta I_d}{\delta V_i} = 30\ \mu A/V$ typ.

$\frac{\delta V_{BE}}{\delta T_{amb}} = -2\ mV/°C$



S-0416

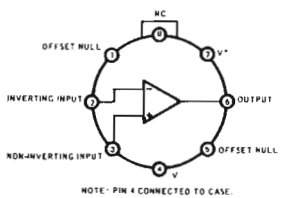
high performance operational amplifier

EXTENDED TEMPERATURE RANGE, - 55°C + 125°C

- No frequency compensation required
- Short-circuit protection
- Offset voltage null capability
- Large common-mode and differential voltage ranges
- Low power consumption
- No latch up

The L 141 is a high performance monolithic operational amplifier constructed on a single silicon chip, using the Planar epitaxial process. It is intended for a wide range of analog applications. High common mode voltage range and absence of "latch-up" tendencies make the L 141 ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications. The L141 is short-circuit protected, has the same pin configuration as the popular μA709 operational amplifier, but requires no external components for frequency compensation. The internal 6dB/octave roll-off insures stability in closed loop applications.

CONNECTION DIAGRAM
(Top view)



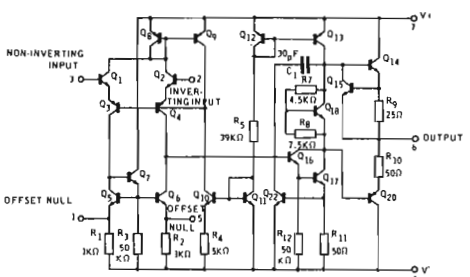
NOTE: PIN 4 CONNECTED TO CASE.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

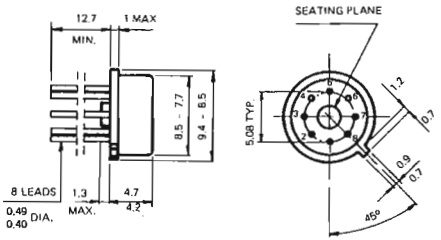
Supply Voltage	± 22 V
Internal Power Dissipation (1)	500 mW
Differential Input Voltage	± 30 V
Input Voltage (2)	± 15 V
Storage Temperature Range	- 65°C to + 150°C
Operating Temperature Range	- 55°C to + 125°C
Lead Temperature (Soldering, 60 sec.)	300°C
Output Short-Circuit Duration (3)	Indefinite

Notes :
1) Rating applies for case temperatures to 125°C; derate linearly at 6,5 mW/°C for ambient temperaturesabove + 75°C.
2) For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.
3) Short circuit may be to ground or either supply. Rating applies to + 125°C case temperature or + 75°C amblant temperature.

SCHEMATIC DIAGRAM



PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-99 outline



Notes: All dimensions in mm.

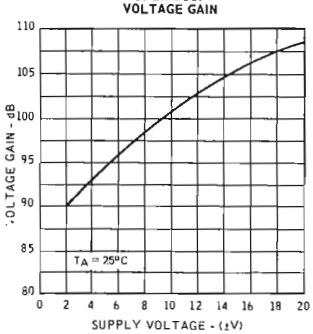
ORDERING NUMBER

L141 T2

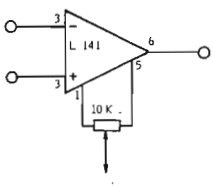
ELECTRICAL CHARACTERISTICS ($V_S = \pm 15V$, $T_A = 25°C$ unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	$R_S \leq 10\ k\Omega$		1	5	mV
Input Offset Current			30	200	nA
Input Bias Current			200	500	nA
Input Resistance		0.3	1		MΩ
Large-Signal Voltage Gain	$R_L \geq 2\ k\Omega$, $V_{OUT} = \pm 10V$	50.000	200,000		
Output Voltage Swing	$R_L \geq 10\ k\Omega$	± 12	± 14		V
	$R_L \geq 2\ k\Omega$	± 10	± 13		V
Input Voltage Range		± 12	± 13		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$		30	150	μV/V
Power Consumption			50	85	mW
Transient Response (unity gain)	$V_{in} = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF				
Risetime			0.3		μs
Overshoot			5		%
Slew Rate (unity gain)	$R_L \geq 2\ k\Omega$		0.5		V/μs
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage	$R_S \leq 10\ k\Omega$			6	mV
Input Offset Current				500	nA
Input Bias Current				1.5	μA
Large-Signal Voltage Gain	$R_L \geq 2\ k\Omega$ $V_{OUT} = \pm 10V$	25.000			
Output Voltage Swing	$R_L \geq 2\ k\Omega$	± 10			V

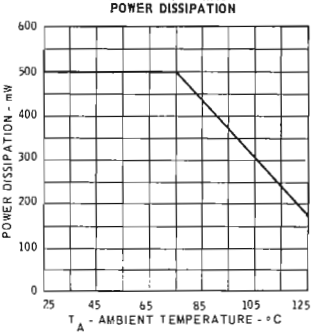
OPEN LOOP VOLTAGE GAIN



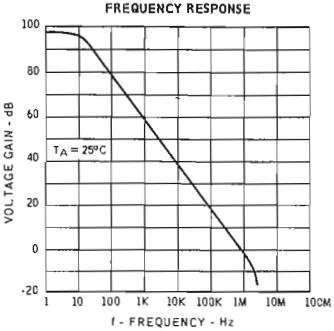
VOLTAGE OFFSET NULL CIRCUIT



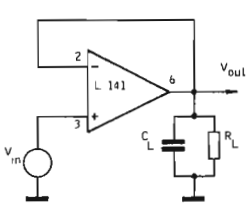
ABSOLUTE MAXIMUM POWER DISSIPATION



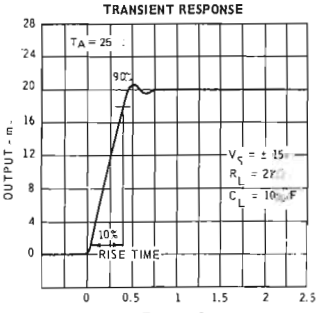
OPEN LOOP FREQUENCY RESPONSE



TRANSIENT RESPONSE TEST CIRCUIT



TRANSIENT RESPONSE



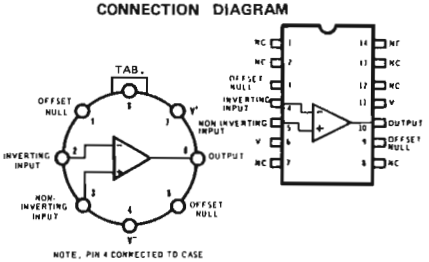
high performance operational amplifier

STANDARD TEMPERATURE RANGE, 0°C + 70°C

- No frequency compensation required
- Short-circuit protection
- Offset voltage null capability
- Large Common-Mode and differential voltage ranges
- Low power consumption
- No latch up

The L 141 is a high performance monolithic operational amplifier constructed on a single silicon chip, using the Planar epitaxial process. It is intended for a wide range of analog applications. High common mode voltage range and absence of "latch-up" tendencies make the L 141 ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications. The L 141 is short-circuit protected, has the same pin configuration as the popular μA709 operational amplifier, but requires no external components for frequency compensation. The internal 6dB/octave roll-off insures stability in closed loop applications.

CONNECTION DIAGRAM



NOTE, PIN 4 CONNECTED TO CASE

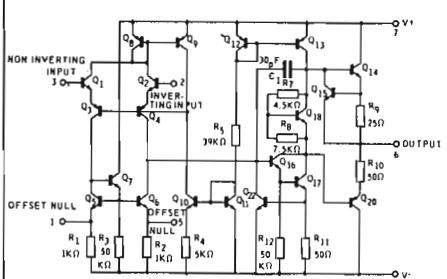
(top view)

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

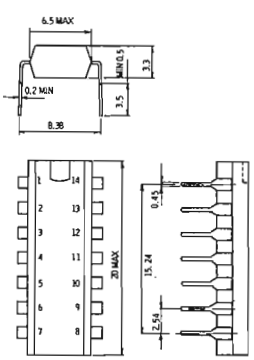
Supply Voltage	± 18 V
Internal Power Dissipation	500 mW
Differential Input Voltage	± 30 V
Input Voltage (1)	± 15 V
Storage Temperature Range	- 65°C to + 150°C
Operating Temperature Range	0°C to + 70°C
Lead Temperature (Soldering, 60 sec)	300°C
Output Short-Circuit Duration (2)	Indefinite

Notes :
1)For supply voltages less than ± 15V, the absolute maximum input voltage is equal to the supply voltage.
2) Short circuit may be to ground or either supply.

SCHEMATIC DIAGRAM

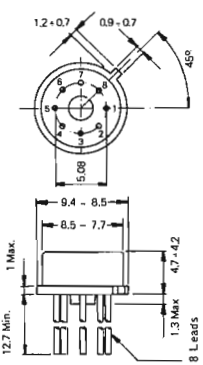


PHYSICAL DIMENSIONS
14-pin plastic DIP



Note : all dimensions in mm.

PHYSICAL DIMENSIONS
similar to
Jedec TO 99 outline



Notes: All dimensions in mm.

ORDERING NUMBER

L141 B1 (for TO116 package)
L141 T1 (for TO 99 package)

MAY 1969

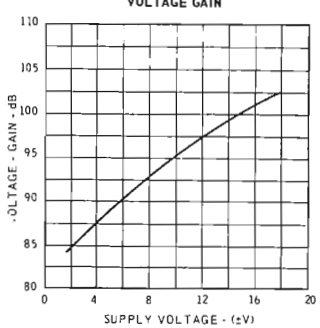
STANDARD TEMPERATURE RANGE

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified)

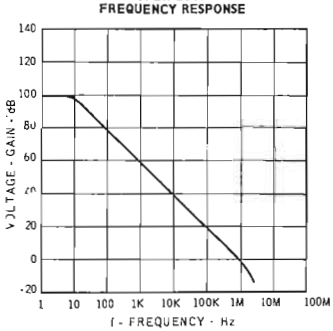
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	$R_S \leq 10\,k\Omega$		2	6	mV
Input Offset Current			30	200	nA
Input Bias Current			200	500	nA
Input Resistance		0.3	1		MΩ
Large-Signal Voltage Gain	$R_L \geq 2\,k\Omega$, $V_{OUT} = \pm 10$ V	20.000	100.000		
Output Voltage Swing	$R_L \geq 10\,k\Omega$	±12	±14		V
	$R_L \geq 2\,k\Omega$	±10	±13		V
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10\,k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\,k\Omega$		30	150	μV/V
Power Consumption			50	85	mW
Transient Response (unity gain)	$V_{in} = 20$ mV, $R_L = 2\,k\Omega$, $C_L \leq 100$ pF				
Risetime			0.3		μs
Overshoot			5		%
Slew Rate (unity gain)	$R_L \geq 2\,k\Omega$		0.5		V/μs
The following specifications apply for $0°C \leq T_A \leq +70°C$:					
Input Offset Voltage	$R_S \leq 10\,k\Omega$			7.5	mV
Input Offset Current				300	nA
Input Bias Current				800	nA
Large-Signal Voltage Gain	$R_L \geq 2\,k\Omega$ $V_{OUT} = \pm 10$ V	15.000			
Output Voltage Swing	$R_L \geq 2\,k\Omega$	± 10			V

TYPICAL PERFORMANCE CURVES (25°C free air temperature unless otherwise noted)

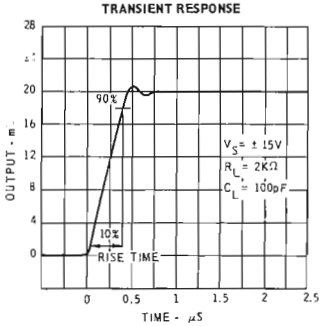
OPEN LOOP VOLTAGE GAIN



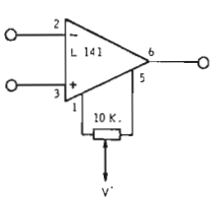
OPEN LOOP FREQUENCY RESPONSE



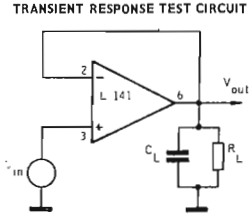
TRANSIENT RESPONSE



VOLTAGE OFFSET NULL CIRCUIT



TRANSIENT RESPONSE TEST CIRCUIT



Dual frequency compensated operational amplifier

STANDARD TEMPERATURE RANGE.
0° C to 70° C

- NO FREQUENCY COMPENSATION REQUIRED
- SHORT-CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- LARGE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW POWER CONSUMPTION
- NO LATCH-UP

The L147B1 is a pair of high performance monolithic operational amplifiers intended for a wide range of analogue applications where board space or weight are important. High common mode voltage range and absence of "latch-up" make the L147B1 ideal for use as a voltage follower. The high gain and wide range of operating voltage provide superior performance in integrator, summing amplifier and general feedback applications. The L147B1 is short-circuit protected and requires no external components for frequency compensation. The internal 6 dB/octave roll-off ensures stability in closed loop applications. For single amplifier performance see L 141 data sheet.

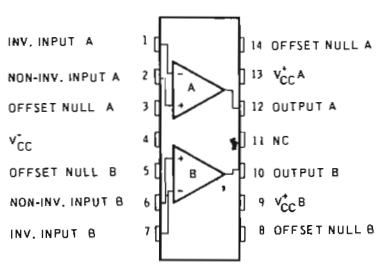
ORDERING NUMBER
L 147 B1

Notes on the following page.

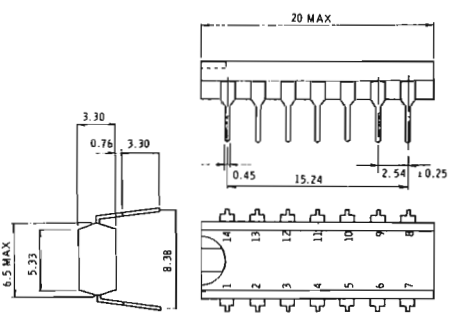
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	± 18 V
Differential Input Voltage	± 30 V
Input Voltage Range (Note 1)	± 15 V
Voltage Between Offset Null and V_{CC}^-	± 0.5 V
Storage Temperature Range	-55° C to 125° C
Power Dissipation ($T_A \leq 70°C$)	500 mW
Operating Temperature Range	0° C to 70° C
Thermal Resistance J-A	110° C/W
Output Short-Circuit Duration (Note 2)	Indefinite
Lead Temperature (Soldering, 10 sec time limit)	260° C
Max Junction Temperature	125° C

CONNECTION DIAGRAM
(Top view)



PHYSICAL DIMENSIONS
14 pin plastic DIP



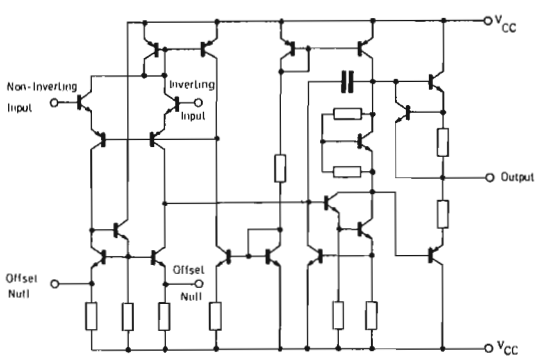
Note : all dimensions in mm.

STANDARD TEMPERATURE RANGE

ELECTRICAL CHARACTERISTICS (T_A = 25°C; V_{CC}=±15V unless otherwise specified), for each amplifier.

PARAMETER	CONDITIONS	Min.	Typ.	Max.	UNIT
Input Offset Voltage	$R_S \leq 10\,k\Omega$		± 1	± 6	mV
Input Offset Current			20	200	nA
Input Bias Current			80	500	nA
Input Resistance		0.3	2		MΩ
Input Capacitance			1.4		pF
Offset Voltage Adjustment Range			±15		mV
Input Voltage Range		± 12	±13		V
Large Signal Voltage Gain	$R_L \geq 2\,k\Omega$ V_{OUT} = ± 10V	50.000	200.000		
Common Mode Rejection Ratio	$R_S \leq 10\,k\Omega$	70	90		dB
Output Resistance			75		Ω
Supply Voltage Rejection Ratio	$R_S \leq 10\,k\Omega$		30	150	µV/ V
Output Short -Circuit Current			25		mA
Supply Current			1.7	2.8	mA
Output Voltage Swing	$R_L \geq 2\,k\Omega$	±10	± 13		V
	$R_L \geq 10\,k\Omega$	±12	± 14		V
Power Consumption			50	85	mW
Transient Response (unity gain):	V_{IN} = 20mV R_L=2kΩ $C_L \leq 100pF$				
Risetime			0.3		µs
Overshoot			5		%
Slew Rate	$R_L \geq 2\,k\Omega$		0.5		V/ µs
Channel Separation			120		dB
The following specifications apply for $0°C \leq T_A \leq 70°C$:					
Input Offset Voltage	$R_S \leq 10\,k\Omega$		± 1	± 7.5	mV
Input Offset Current				300	nA
Input Bias Current			30	800	nA
Large Signal Voltage Gain	$R_L \geq 2\,k\Omega$ V_{OUT} = ± 10V	25.000			
Output Voltage Swing	$R_L \geq 2\,k\Omega$	±10	± 13		V

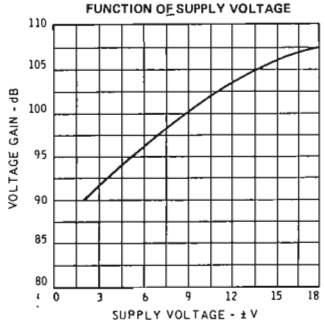
EQUIVALENT CIRCUIT (Each side)



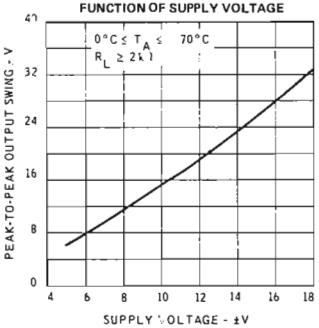
Notes :
1) For supply voltages less than ± 15V, the absolute maximum input voltage is equal to the supply voltage.
2) Short-circuit to ground for both sections or to either supply (for one section only).

TYPICAL ELECTRICAL CHARACTERISTICS (Each amplifier)

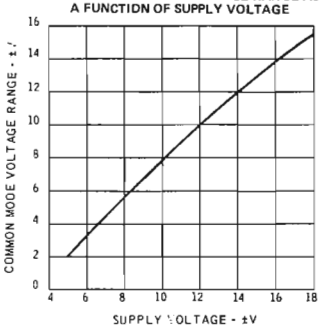
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



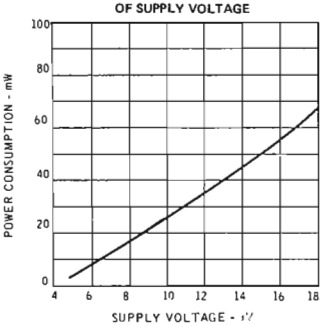
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



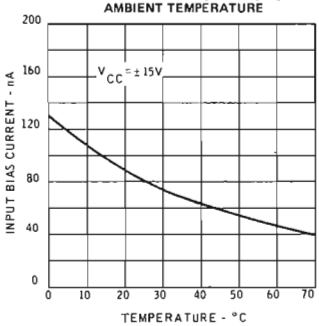
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



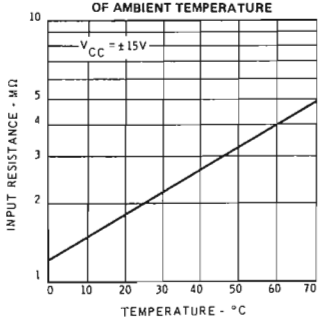
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



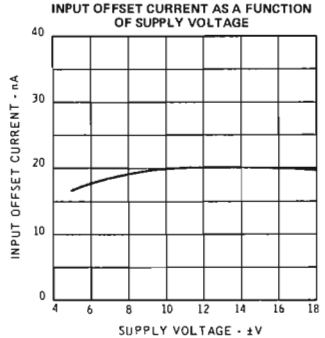
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



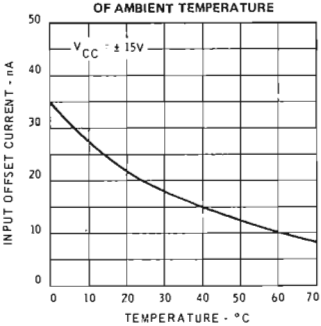
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



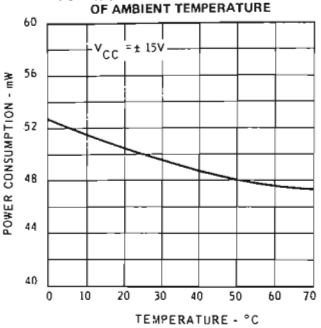
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

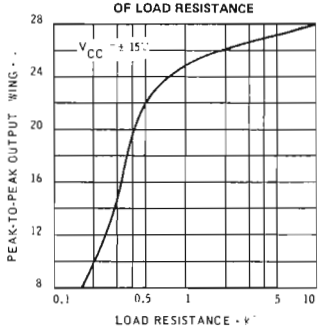


POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE

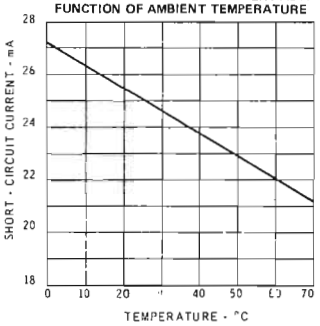


TYPICAL ELECTRICAL CHARACTERISTICS (Each amplifier)

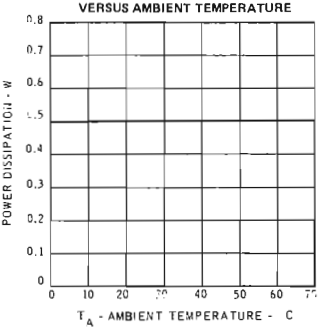
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



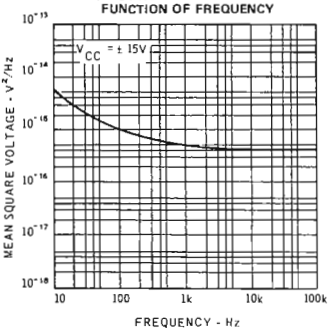
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



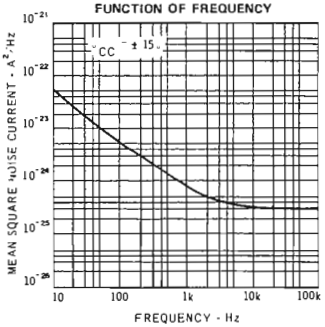
MAX ALLOWABLE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



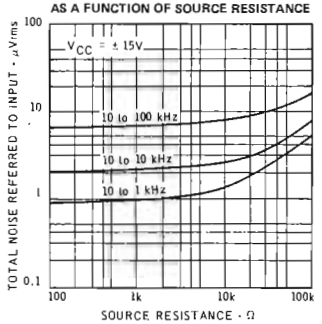
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



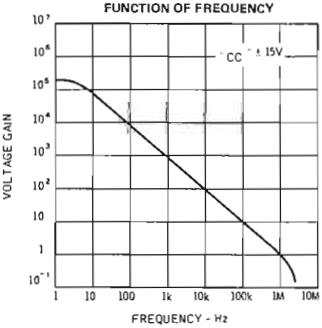
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



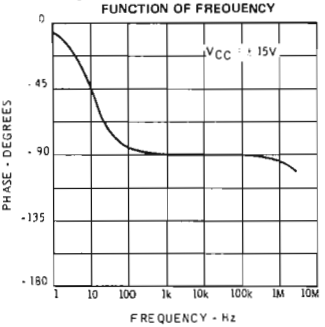
BROADBAND NOISE FOR VARIOUS BANDWIDTH AS A FUNCTION OF SOURCE RESISTANCE



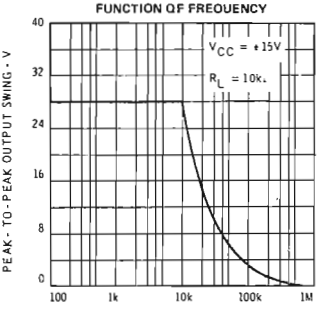
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY

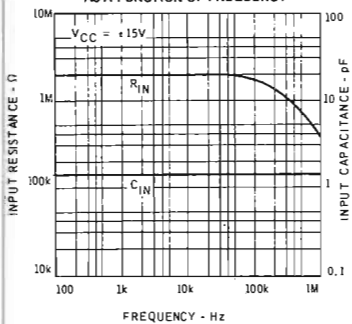


OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY

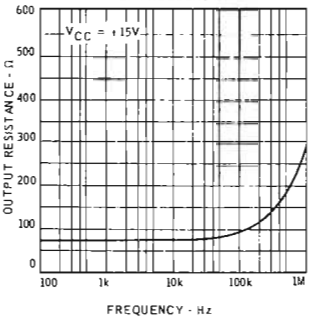


TYPICAL ELECTRICAL CHARACTERISTICS (Each amplifier)

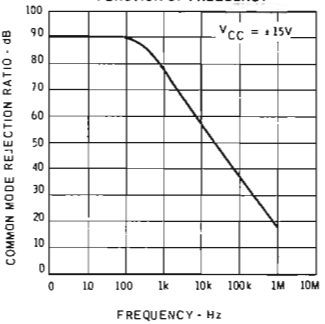
INPUT RESISTANCE AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



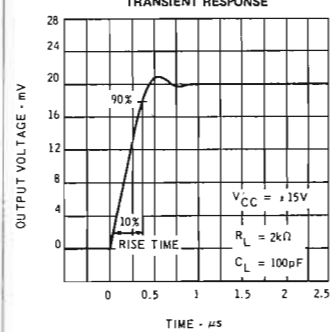
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY



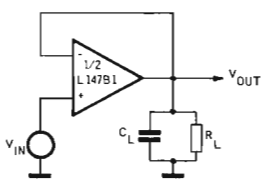
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



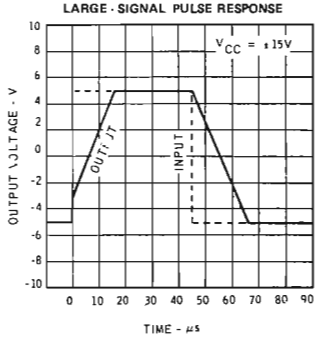
TRANSIENT RESPONSE



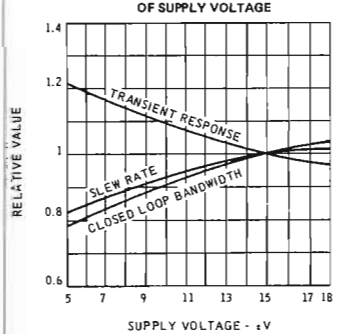
TRANSIENT RESPONSE TEST CIRCUIT



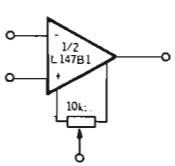
VOLTAGE FOLLOWER LARGE-SIGNAL PULSE RESPONSE



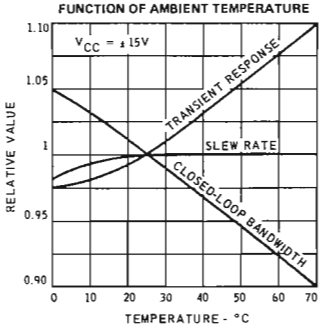
FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



VOLTAGE OFFSET NULL CIRCUIT

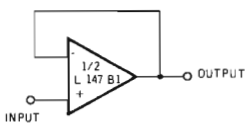


FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



TYPICAL APPLICATIONS

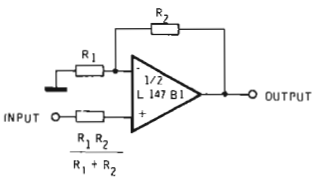
UNITY-GAIN VOLTAGE FOLLOWER



$R_{IN} = 400\ M\Omega$ $\quad R_{out} << 1\ \Omega$

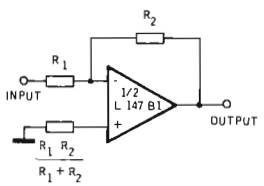
$C_{IN} = 1\ pF$ $\quad$ B.W. = 1 MHz

NON-INVERTING AMPLIFIER



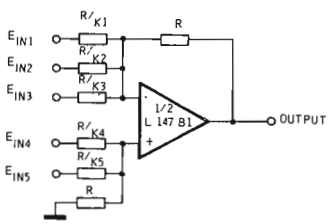
GAIN	R_1	R_2	B.W.	R_{IN}
10	1 kΩ	9 kΩ	100 kHz	400 MΩ
100	100 Ω	9.9 kΩ	10 kHz	280 MΩ
1000	100 Ω	99.9 kΩ	1 kHz	80 MΩ

INVERTING AMPLIFIER



GAIN	R_1	R_2	B.W.	R_{IN}
1	10 kΩ	10 kΩ	1 MHz	10 kΩ
10	1 kΩ	10 kΩ	100 kHz	1 kΩ
100	1 kΩ	100 kΩ	10 kHz	1 Ω
1000	100 Ω	100 kΩ	1 kHz	100 Ω

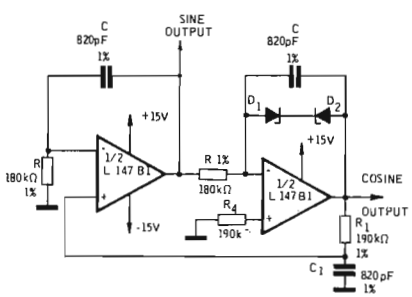
WEIGHTED AVERAGING AMPLIFIER



If $k_1 + k_2 + k_3 = k_4 + k_5$ the response equation is given by

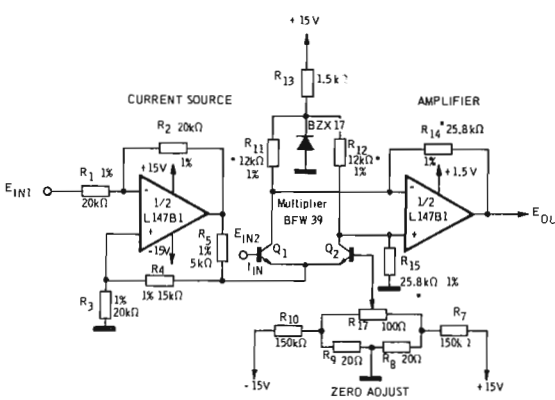
$E_{out} = E_{IN1} K_1 + E_{IN2} K_2 + E_{IN3} - E_{IN4} K_4 - E_{IN5} K_5$

QUADRATURE OSCILLATOR



$$f = \frac{1}{2\pi RC}$$

ANALOGUE-MULTIPLIER

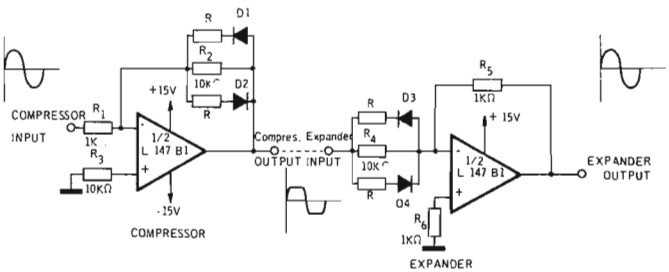


* Matched to 0.1%

$E_{OUT} = 100\ E_{IN1} \times E_{IN2}$

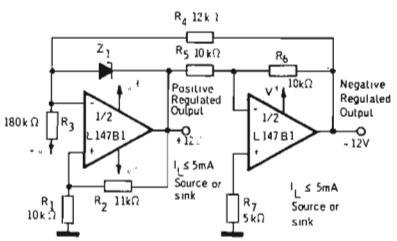
TYPICAL APPLICATIONS (contd)

COMPRESSOR/EXPANDER AMPLIFIERS



Maximum compression expansion ratio = R_1/R $(10k\Omega > R \geq 0)$
Note : diodes D_1 through D_4 are matched BAW 55 or equivalent

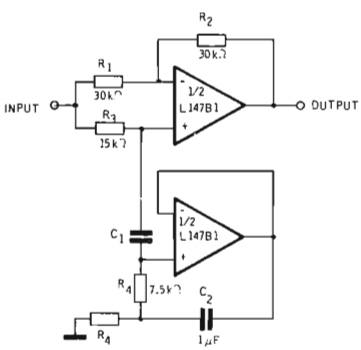
TRACKING POSITIVE AND NEGATIVE VOLTAGE REFERENCES



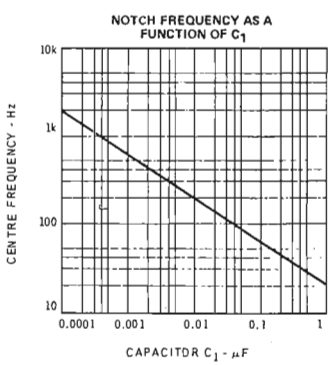
$$\text{Positive output} = V_{Z1} \times \frac{R_1 + R_2}{R_2}$$

$$\text{Negative output} = -\text{positive output} \times \frac{R_6}{R_5}$$

NOTCH FILTER USING THE L 147B1 AS A GYRATOR



Trim R_3 such that $\frac{R_1}{R_2} = \frac{R_3}{2R_4}$



DEFINITION OF TERMS :

INPUT OFFSET VOLTAGE – That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT – The difference in the currents into the two input terminals with the output at zero volts.

INPUT BIAS CURRENT – The average of the two input currents.

INPUT RESISTANCE – The resistance looking into either input terminal with the other grounded.

INPUT CAPACITANCE – The capacitance looking into either input terminal with the other grounded.

LARGE-SIGNAL VOLTAGE GAIN – The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT RESISTANCE – The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and terminal feedback.

OUTPUT SHORT-CIRCUIT CURRENT – The maximum output current available from the amplifier with the output shorted to ground or to either supply

SUPPLY CURRENT – The DC current from the supplies required to operate the amplifier with the output at zero and with no load current.

POWER CONSUMPTION – The DC power required to operate the amplifier with the output at zero and with no load current.

TRANSIENT RESPONSE – The closed-loop step-function response of the amplifier under small-signal conditions.

INPUT VOLTAGE RANGE – The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO – The ratio of the input voltage range to the maximum change in input offset voltage over this range.

SUPPLY VOLTAGE REJECTION RATIO – The ratio of the change in input voltage to the change in supply voltage producing it.

OUTPUT VOLTAGE SWING – The peak output swing, referred to zero, that can be obtained without clipping.

EXTENDED TEMPERATURE RANGE,
-55 °C ÷ +125° C

High performance operational amplifier

- SHORT-CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW POWER CONSUMPTION
- NO LATCH-UP

The L 148 T2 is a high performance monolithic operational amplifier intended for a wide range of analog applications where tailoring of frequency characteristics is desirable. High common mode voltage range and absence of "latch-up" make the L 148 T2 ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier and general feedback applications. The L 148 T2 is short-circuit protected and has the same pin configuration as the L 141 operational amplifier. Unity gain frequency compensation is achieved by means of a single 30pF capacitor.

ABSOLUTE MAXIMUM RATINGS

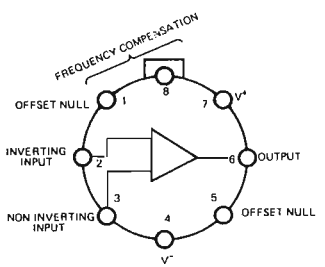
Supply Voltage	± 22 V
Internal Power Dissipation (1)	500 mW
Differential Input Voltage	± 30 V
Input Voltage (2)	± 15 V
Storage Temperature Range	-65°C ÷ 150°C
Operating Temperature Range	-55°C ÷ 125°C
Lead Temperature (Soldering, 60 sec.)	300°C
Output Short-Circuit Duration (3)	Indefinite

ORDERING NUMBER

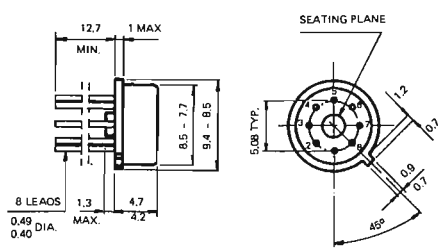
L148 T2

Notes on the following page.

CONNECTION DIAGRAM
(Top view)



PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-99 outline



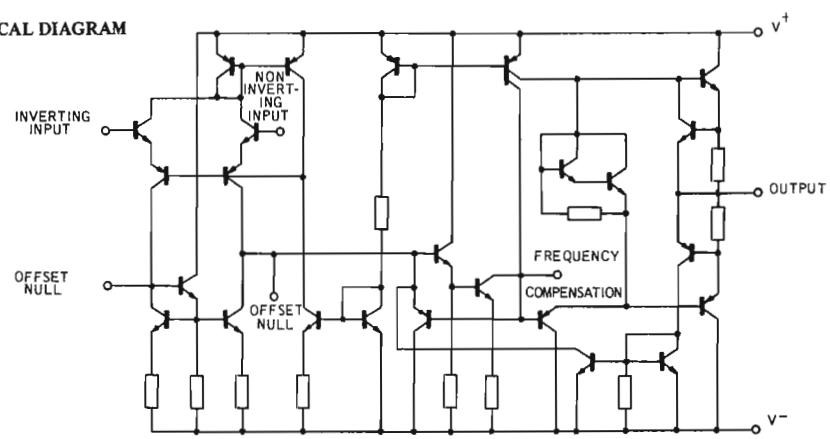
Note : All dimensions in mm.

EXTENDED TEMPERATURE RANGE

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15V$, $T_A = 25°C$ unless otherwise specified)

PARAMETER	CONDITION	Min.	Typ.	Max.	Unit
Input Offset Voltage	$R_S \leq 10\ K\Omega$		1	5	mV
Input Offset Current			20	200	nA
Input Bias Current			80	500	nA
Input Resistance		0.3	2		M Ω
Input Capacitance			1.4		pF
Large-Signal Voltage Gain	$R_L \geq 2K\Omega$ $V_{OUT} = \pm 10V$	50.000	200.000		
Output Resistance			75		Ω
Output Short-Circuit Current			25		mA
Power Consumption			50	85	mW
Transient Response (Unity Gain) :	$V_{in} = 20$ mV $C_C = 30$ pF $R_L = 2\ K\Omega$ $C_L \leq 100$ pF				
Risetime			0.3		μS
Overshoot			5		%
Slew Rate	$R_L \geq 2\ K\Omega$ $C_C = 30$ pF		0.5		V/μS
The following specification apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage	$R_S \leq 10\ K\Omega$		1	6	mV
Input Offset Current	$T_A = +125°C$		7	200	nA
	$T_A = -55°C$		85	500	nA
Input Bias Current	$T_A = +125°C$		0.03	0.5	μA
	$T_A = -55°C$		0.3	1.5	μA
Input Voltage Range		± 12	± 13		V
Common Mode Rejection Ratio	$R_S \leq 10\ K\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ K\Omega$		30	150	μV/V
Large-Signal Voltage Gain	$R_L \geq 2\ K\Omega$ $V_{OUT} = \pm 10V$	25.000			
Output Voltage Swing	$R_L \geq 10K\Omega$	± 12	± 14		V
	$R_L \geq 2\ K\Omega$	± 10	± 13		V
Power Consumption	$T_A = +125°C$		45		mW
	$T_A = -55°C$		60		mW

ELECTRICAL DIAGRAM

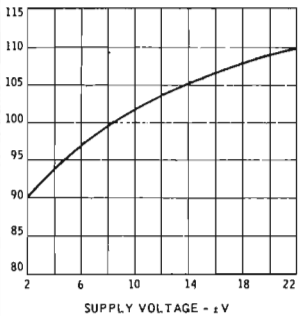


NOTES :

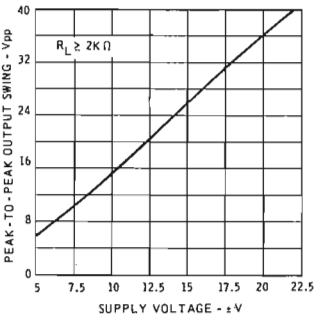
1) Rating applies for case temperatures to 125°C; derate linearly at 10 mW/°C for ambient temperatures above +75°C.
2) For supply voltage less than ± 15V, the absolute maximum input voltage is equal to the supply voltage.
3) Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

TYPICAL ELECTRICAL CHARACTERISTICS (25° C free air temperature unless otherwise noted)

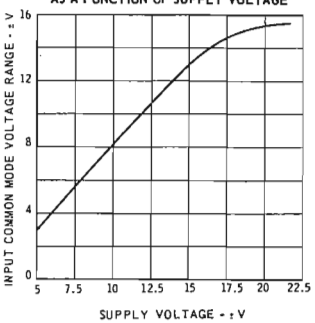
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



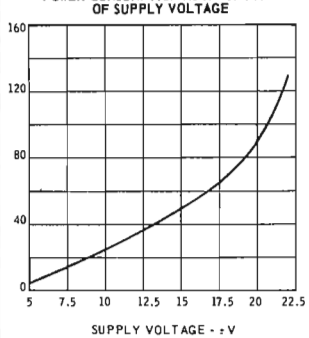
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



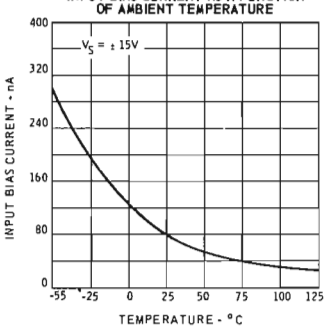
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



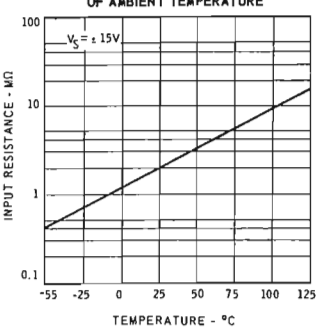
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



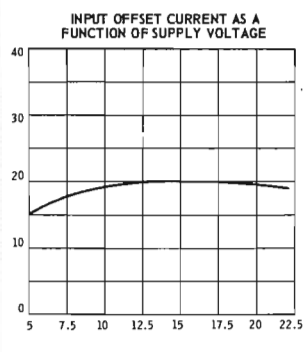
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



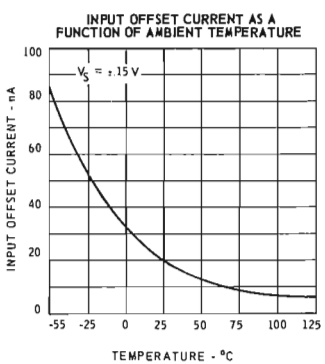
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



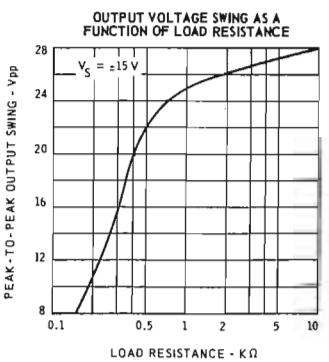
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



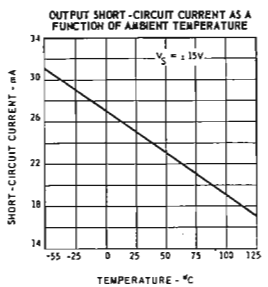
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

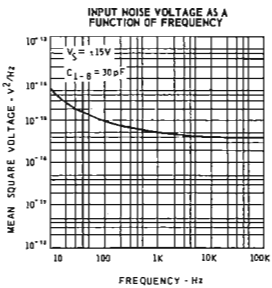


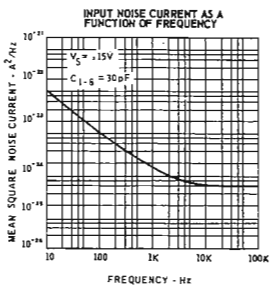
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

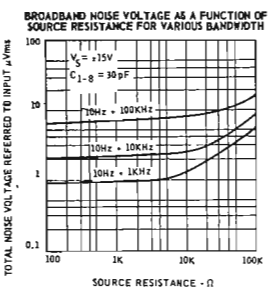


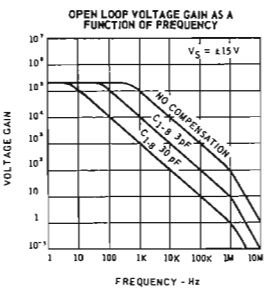
TYPICAL ELECTRICAL CHARACTERISTICS (25° C free air temperature unless otherwise noted)

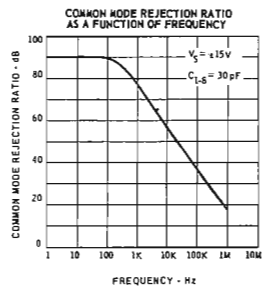


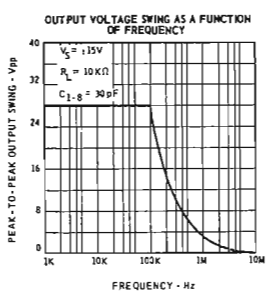


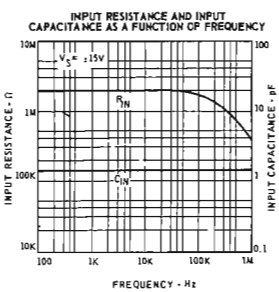


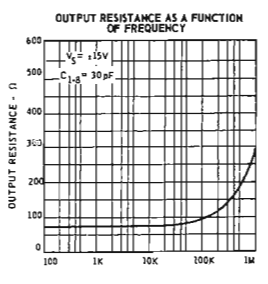






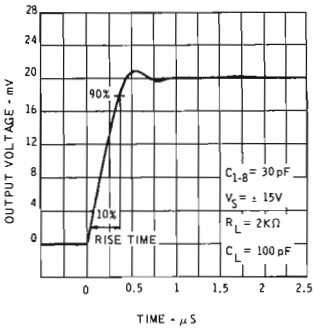




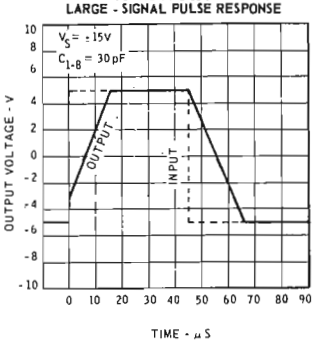


TYPICAL ELECTRICAL CHARACTERISTICS (25° C free air temperature unless otherwise noted)

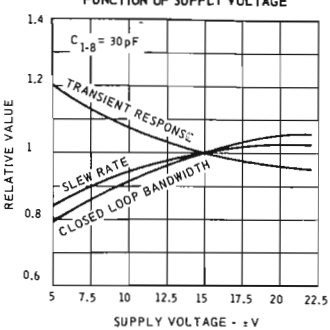
TRANSIENT RESPONSE (UNITY GAIN)



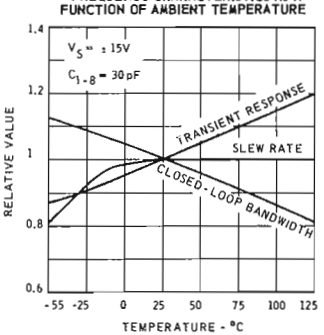
VOLTAGE FOLLOWER
LARGE - SIGNAL PULSE RESPONSE



FREQUENCY CHARACTERISTICS AS A
FUNCTION OF SUPPLY VOLTAGE



FREQUENCY CHARACTERISTICS AS A
FUNCTION OF AMBIENT TEMPERATURE



STANDARD TEMPERATURE RANGE, 0°C ÷ 70°C

High performance operational amplifier

- SHORT-CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW POWER CONSUMPTION
- NO LATCH-UP

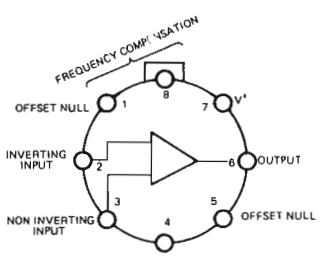
The L 148 T1 is a high performance monolithic operational amplifier intended for a wide range of analog applications where tailoring of frequency characteristics is desirable. High common mode voltage range and absence of "latch-up" make the L 148 T1 ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications. The L 148 T1 is short-circuit protected and has the same pin configuration as the L 141 operational amplifier. Unity gain frequency compensation is achieved by means of a single 30 pF capacitor. For full temperature range operation (-55°C ÷ +125°C), see L 148 T2 data sheet.

ABSOLUTE MAXIMUM RATINGS

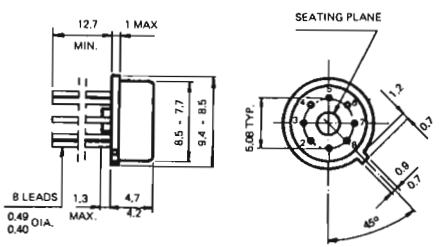
Supply Voltage	± 18V
Internal Power Dissipation (1)	500 mW
Differential Input Voltage	± 30V
Input Voltage (2)	± 15V
Storage Temperature Range	-55°C ÷ +150°C
Operating Temperature Range	0°C ÷ + 70°C
Lead Temperature (soldering, 60 secs)	300°C
Output Short-Circuit Duration (3)	Indefinite

Notes on the following page.

CONNECTION DIAGRAM
(Top view)



PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-99 outline



Note : All dimensions in mm.

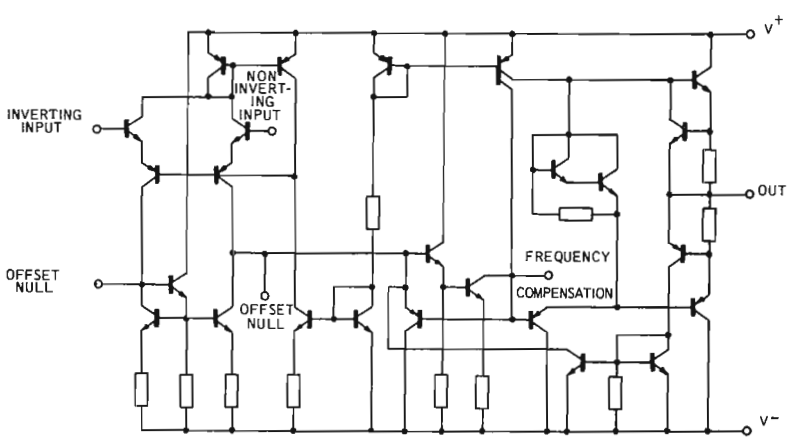
ORDERING NUMBER
L148 T1

STANDARD TEMPERATURE RANGE

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15V$, $T_A = 25°C$ unless otherwise noted)

PARAMETER	CONDITIONS		Min.	Typ.	Max.	Units
Input Offset Voltage	$R_S \leq 10K\Omega$			1	6	mV
Input Offset Current				20	200	nA
Input Bias Current				80	500	nA
Input Resistance			0.3	2		MΩ
Input Capacitance				1.4		pF
Large-Signal Voltage Gain	$R_L \geq 2K\Omega$	$V_{OUT} = \pm 10V$	50.000	200.000		
Output Resistance				75		Ω
Output Short-Circuit Current				25		mA
Power Consumption				50	85	mW
Transient Response (Unity Gain):	$V_{in} = 20mV$	$C_C = 30$ pF				
	$R_L = 2K\Omega$	$C_L \leq 100$ pF				
Risetime				0.3		μs
Overshoot				5.0		%
Slew Rate	$R_L \geq 2K\Omega$			0.5		V/μS
The following specifications apply for $0°C \leq T_A \leq +70°C$:						
Input Offset Voltage	$R_S \leq 10K\Omega$			1	7.5	mV
Input Offset Current					300	nA
Input Bias Current					800	nA
Large-Signal Voltage Gain	$R_L \geq 2K\Omega$	$V_{OUT} = \pm 10V$	25.000			
Output Voltage Swing	$R_L \geq 2K\Omega$		± 10	± 13		V
Power Consumption				50		mW

ELECTRICAL DIAGRAM

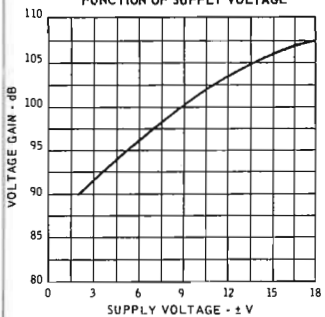


NOTES :
1) Rating applies for case temperatures to +70°C.
2) For supply voltages less than ± 15V, the absolute maximum input voltage is equal to the supply voltage.
3) Short circuit may be to ground or either supply. Rating applies to +70°C ambient temperature.

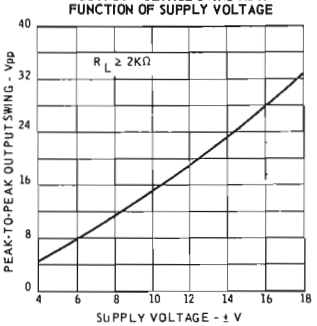
STANDARD TEMPERATURE RANGE

TYPICAL ELECTRICAL CHARACTERISTICS (25° C free air temperature unless otherwise noted)

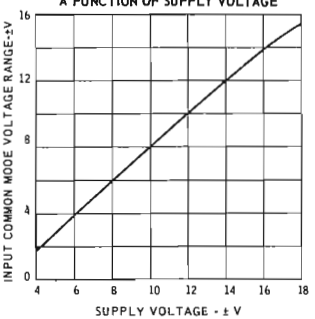
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



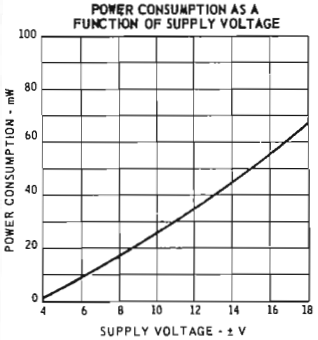
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



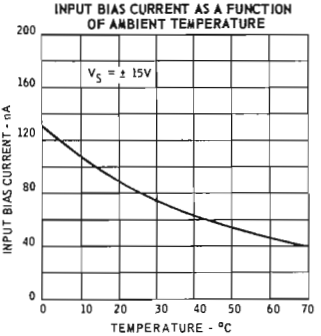
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



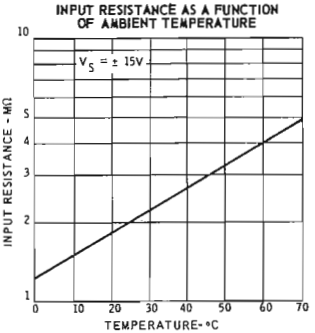
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



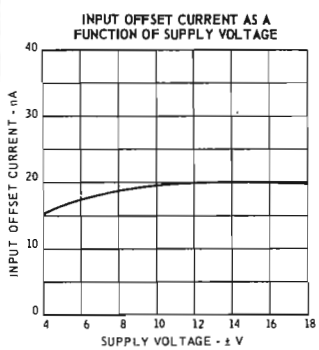
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



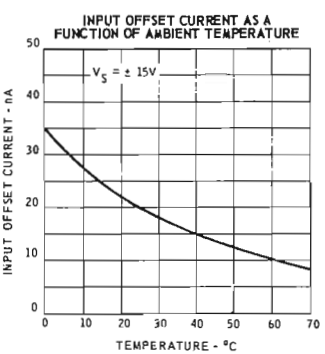
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



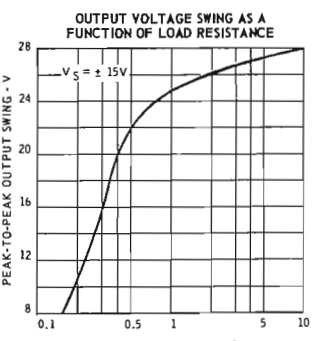
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

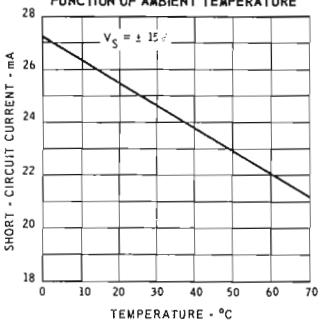


OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

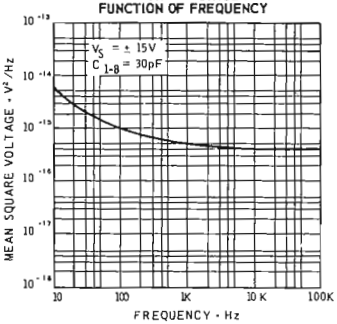


TYPICAL ELECTRICAL CHARACTERISTICS (25° C free air temperature unless otherwise noted)

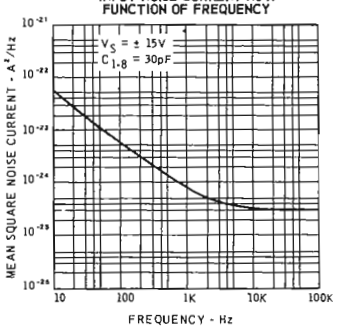
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



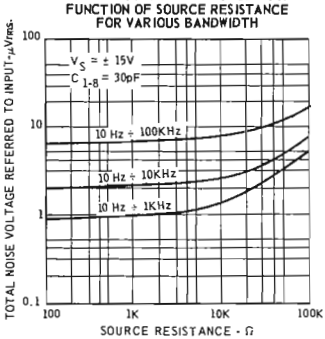
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



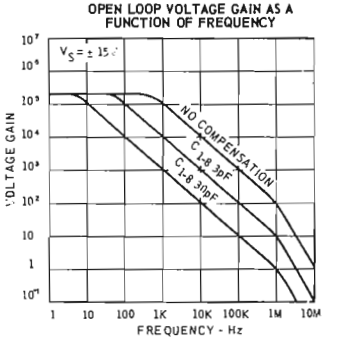
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



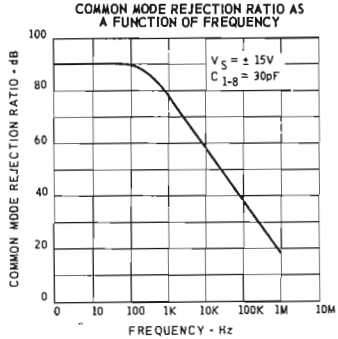
BROADBAND NOISE VOLTAGE AS A FUNCTION OF SOURCE RESISTANCE FOR VARIOUS BANDWIDTH



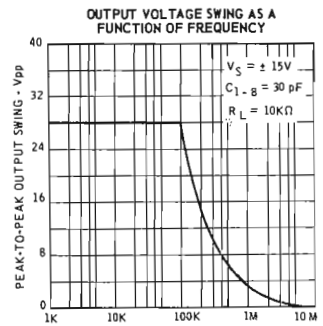
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



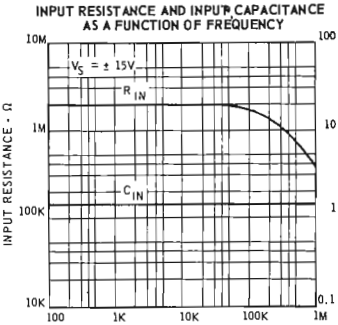
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



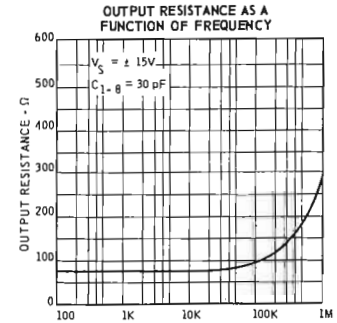
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



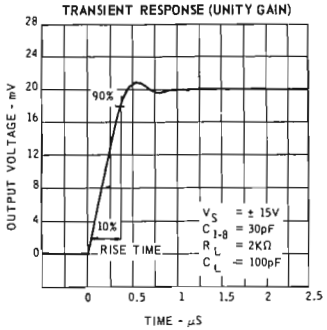
INPUT RESISTANCE AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY

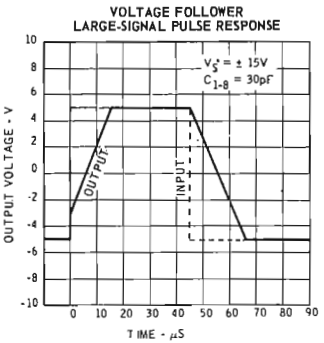


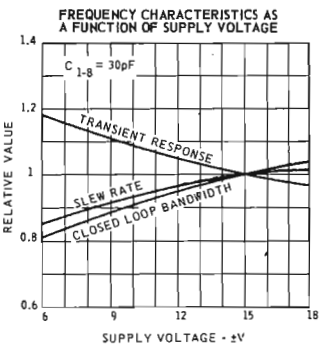
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY

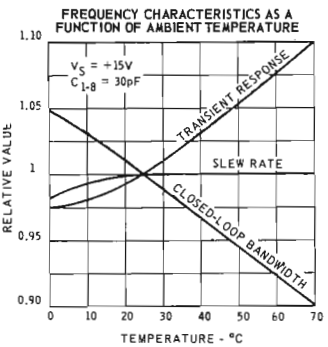


TYPICAL ELECTRICAL CHARACTERISTICS (25° C free air temperature unless otherwise noted)









Audio amplifier

INTERMEDIATE TEMPERATURE RANGE,
−40°C to 85°C

- HIGH OUTPUT POWER
- LOW DISTORTION
- LOW QUIESCENT CURRENT
- SELF CENTERING BIAS
- HIGH INPUT IMPEDANCE

The TAA 611E is a monolithic integrated circuit particularly designed for use as audio amplifier where a temperature range of -40°C to 85°C is required. The usable range of supply voltage varies from 6V to 10V. Special features of the circuit include low quiescent current, self-centering bias and direct coupling of the input. The circuit requires a minimum number of external components.

ABSOLUTE MAXIMUM RATINGS

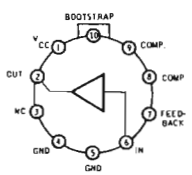
Max Supply Voltage	12 V
Input Voltage (see note)	-0.5 to + 12 V
Peak Output Current	1 A
Operating Temperature Range	-40°C to +85°C
TAA 611E 55	
Storage Temperature	-55°C to + 150°C
Maximum Junction Temperature	150°C
Power Dissipation ($T_A \leq 25°C$)	570 mW
Power Dissipation ($T_C \leq 85°C$)	1.3 W
Thermal Resistance J-A	220° C/W
Thermal Resistance J-C	50° C/W
TAA 611E 12	
Storage Temperature	-55°C to + 125°C
Maximum Junction Temperature	150°C
Power Dissipation ($T_A \leq 25°C$)	1.35 W
Thermal Resistance J-A	93° C/W

Note : for supply voltages less than 12V, the absolute max input voltage is equal to the supply voltage.

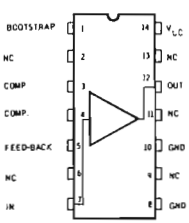
ORDERING NUMBERS

TAA 611E 55 (for package No. 1)
TAA 611E 12 (for package No. 2)

CONNECTION DIAGRAMS
(top view)



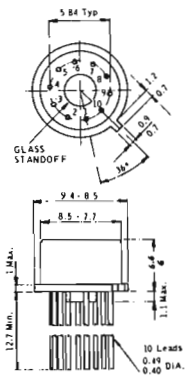
Package No. 1



Package No. 2

PACKAGE No. 1

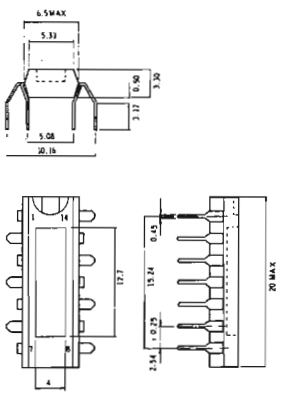
PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-100 outline



Note : All dimensions in mm.

PACKAGE No. 2

PHYSICAL DIMENSIONS
power plastic split DIP



Note : All dimensions in mm.

OUTPUT POWER AS A FUNCTION OF SUPPLY VOLTAGE AND LOADING CONDITIONS

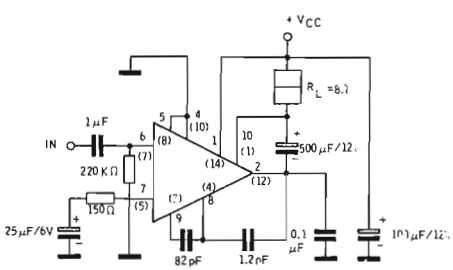
(Typical values at ambient temperature $T_A = 25°C$)

V_{CC} (V)	R_L (Ω)	P_{out} (W) at THD = 2%	P_{out} (W) THD = 10%			External Heat Sink
			Min.	Typ.	Typ. -40°C	
6	4	0.50		0.65	0.6	Not Required
	8	0.35		0.45	0.42	Not Required
9	4	1.4		1.8	1.7	For TAA 611E 55 only
	8	0.9	0.85	1.15	1.1	Not Required

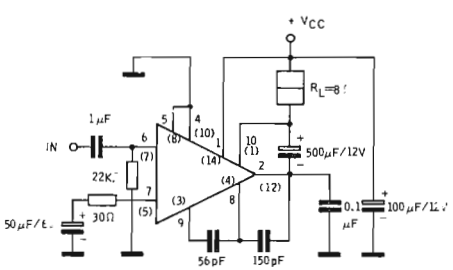
TYPICAL ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V_{CC} = 9V$ unless otherwise noted)

PARAMETER	CONDITIONS	VALUE	UNIT
Total Current (I_{CC})		3	mA
Quiescent Current of Output Transistors (I_O)		1	mA
Input Bias Current		60	nA
DC Output Voltage	$R_S = 220\ K\Omega$	4.8	V
Open Loop Voltage Gain	$R_L = 8\ \Omega$	68	dB
Supply Current	$P_{out} = 1.15W$ $R_L = 8\ \Omega$	170	mA
The Following Specifications Apply for $-40°C \leq T_A \leq 85°C$:			
Quiescent Current of Output Transistors (I_O)		1.1	mA
Open Loop Voltage Gain	$R_L = 8\ \Omega$	67	dB
Total Harmonic Distortion	Test Circuit 1: $R_L = 8\ \Omega$, f = 1KHz		
	$P_{out} = 50mW$	0.4	%
	$R_L = 8\ \Omega$, f = 1KHz, $P_{out} = 0.5W$	0.3	%
	Test Circuit 2: $R_L = 8\ \Omega$, f = 1KHz		
	$P_{out} = 50mW$	1.7	%
	$R_L = 8\ \Omega$, f = 1KHz, $P_{out} = 0.5W$	1.2	%
Feedback Resistance	Pin 2 to 7 (TAA 611E 55)	7.5	KΩ
	Pin 5 to 12 (TAA 611E 12)	7.5	KΩ
Input Impedance	Open Loop	0.75	MΩ

TEST CIRCUIT 1 ($A_V = 50$)



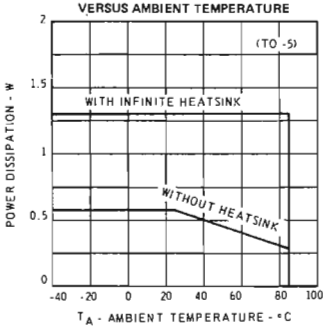
TEST CIRCUIT 2 ($A_V = 250$)



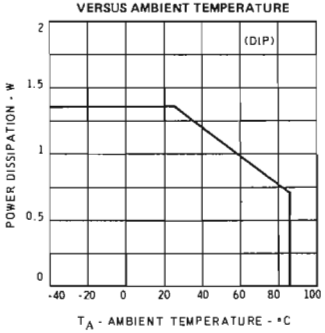
The pin numbers in brackets refer to the TAA 611E 12, and those without brackets refer to the TAA 611E 55.

TYPICAL ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

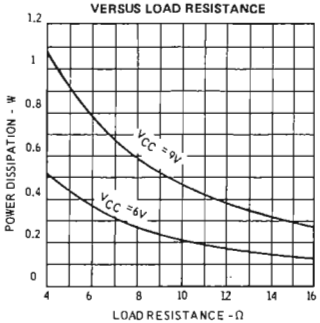
MAX ALLOWABLE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



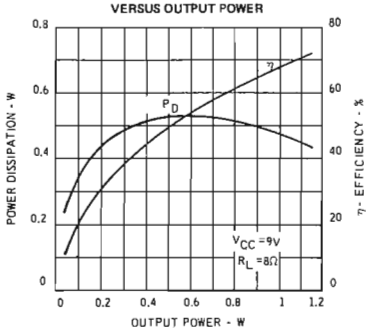
MAX ALLOWABLE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



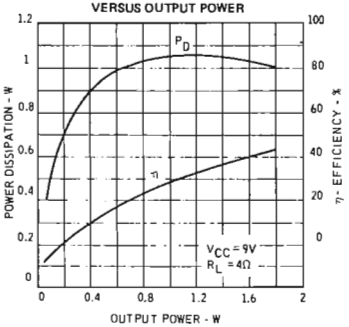
MAX POWER DISSIPATED BY THE CIRCUIT VERSUS LOAD RESISTANCE



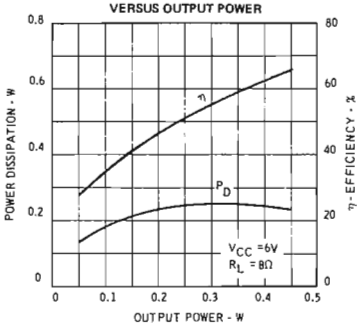
POWER DISSIPATION AND EFFICIENCY VERSUS OUTPUT POWER



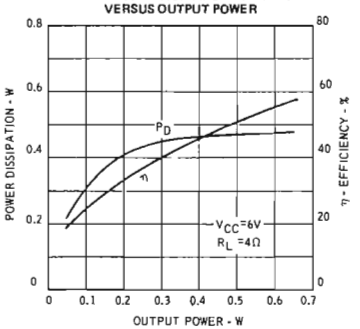
POWER DISSIPATION AND EFFICIENCY VERSUS OUTPUT POWER



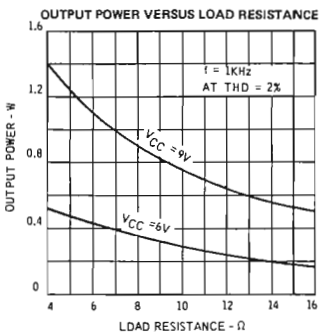
POWER DISSIPATION AND EFFICIENCY VERSUS OUTPUT POWER

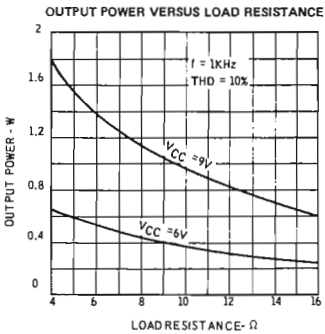


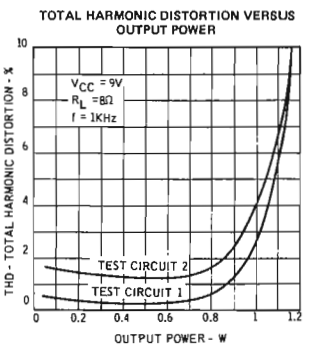
POWER DISSIPATION AND EFFICIENCY VERSUS OUTPUT POWER

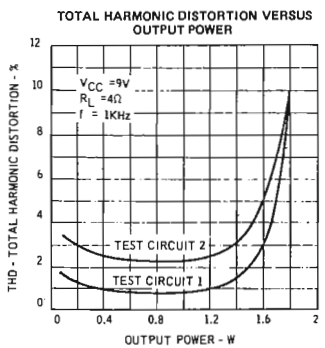


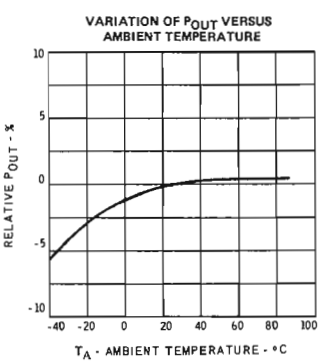
TYPICAL ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

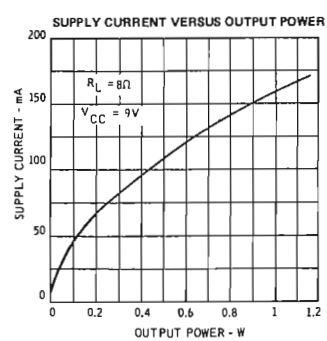




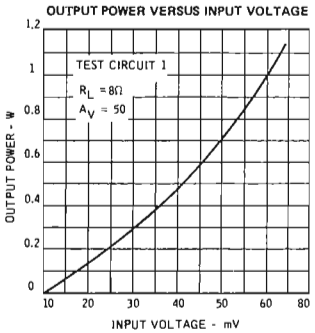


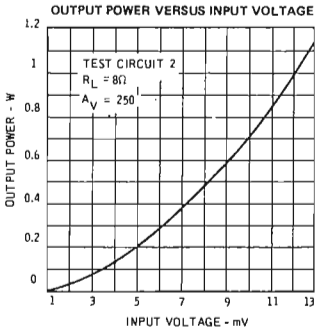


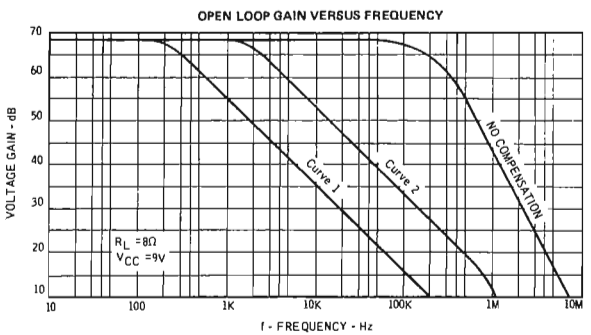




TYPICAL ELECTRICAL CHARACTERISTICS (25° free air temperature unless otherwise noted)



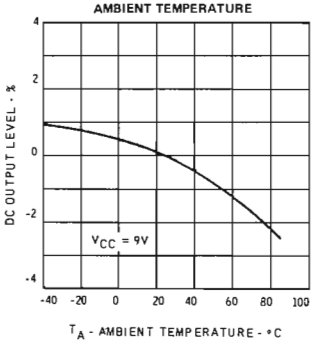




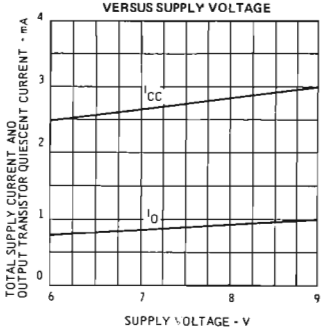
Curve 1: TAA611 E 55, C_{9-8} = 82pF C_{8-2} = 1.2 nF C_{10-1} = 0.1μF
TAA611 E 12, C_{3-4} = 82pF C_{4-12} = 1.2nF C_{1-14} = 0.1μF
Curve 2: TAA611 E 55, C_{9-8} = 56pF C_{8-2} = 150 pF C_{10-1} = 0.1μF
TAA611 E 12, C_{3-4} = 56pF C_{4-12} = 150pF C_{1-14} = 0.1μF

TYPICAL ELECTRICAL CHARACTERISTICS (25° free air temperature unless otherwise noted)

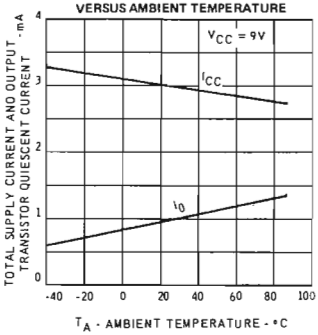
VARIATION OF DC OUTPUT LEVEL VERSUS AMBIENT TEMPERATURE



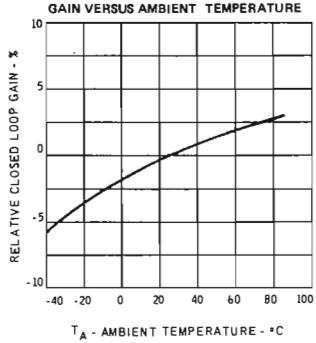
TOTAL SUPPLY CURRENT AND OUTPUT TRANSISTOR QUIESCENT CURRENT VERSUS SUPPLY VOLTAGE



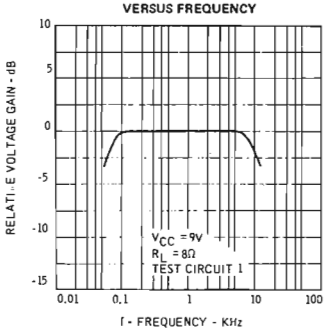
TOTAL SUPPLY CURRENT AND OUTPUT TRANSISTOR QUIESCENT CURRENT VERSUS AMBIENT TEMPERATURE



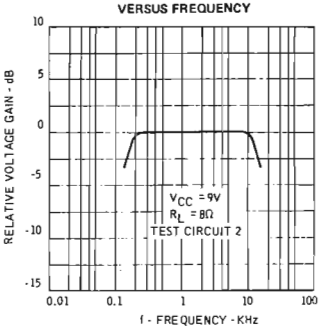
VARIATION OF CLOSED LOOP RELATIVE GAIN VERSUS AMBIENT TEMPERATURE



RELATIVE VOLTAGE GAIN VERSUS FREQUENCY



RELATIVE VOLTAGE GAIN VERSUS FREQUENCY



Audio amplifier

INTERMEDIATE TEMPERATURE RANGE,
- 40° C to 85° C

- OUTPUT POWER 2.1 W
- LOW DISTORTION
- LOW QUIESCENT CURRENT
- SELF CENTERING BIAS
- HIGH INPUT IMPEDANCE

The TAA 611 F is a monolithic integrated circuit particularly designed for use as audio amplifier where a temperature range of -40°C to 85°C is required. The usable range of supply voltage varies from 6 to 15V. Special features of the circuit include low quiescent current, self-centering bias and direct coupling of the input. The circuit requires a minimum number of external components. The package is a special plastic DIP with a copper bar inserted in the plastic which ensures low thermal resistance.

ABSOLUTE MAXIMUM RATINGS

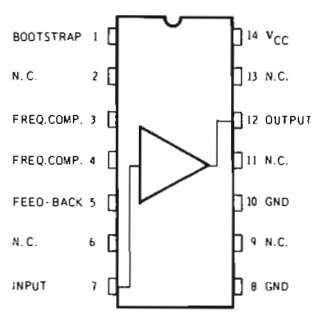
Maximum Operating Supply Voltage	15 V
Input Voltage (see note)	-0.5V to +15 V
Peak Output Current	1 A
Storage Temperature	-55°C to +125°C
Operating Temperature Range	-40°C to +85°C
Max Junction Temperature	150°C
Power Dissipation $T_A \leq 25°C$	1.35W
Thermal Resistance J-A	93°C/W

Note : For supply voltages less than 15V, the absolute max input voltage is equal to the supply voltage.

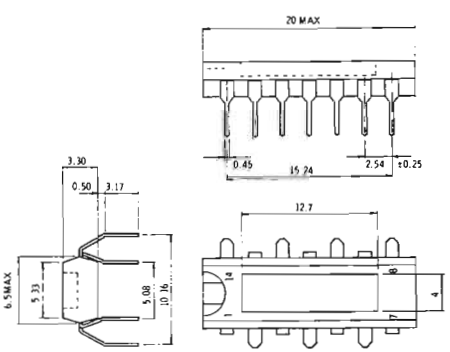
ORDERING NUMBER

TAA 611F 12

CONNECTION DIAGRAM
(Top view)



PHYSICAL DIMENSIONS
Power plastic split DIP



Note : All dimensions in mm.

OUTPUT POWER AS A FUNCTION OF SUPPLY VOLTAGE AND LOADING CONDITIONS

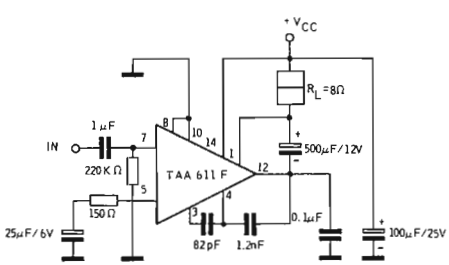
(Typical values at ambient temperature $T_A = 25°C$)

V_{CC} (V)	R_L (Ω)	P_{out} (W) at THD = 2%	P_{out} (W) at THD = 10%		
			Min.	Typ.	Typ. -40°C
9	8	0.9		1.15	1.1
12	8	1.7	1.5	2.1	2

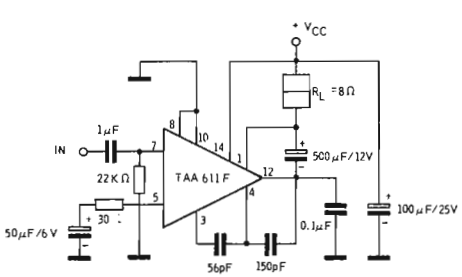
TYPICAL ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

PARAMETER	CONDITIONS	VALUES (V_{CC} = 9V)	VALUES (V_{CC} = 12V)	UNIT
Total Current (I_{CC})		3	3.5	mA
Quiescent Current of Output Transistors (I_O)		1	1.2	mA
Input Bias Current		60	75	nA
DC Output Voltage	R_S = 220 KΩ	4.8	6.3	V
Open Loop Voltage Gain	R_L = 8Ω	68	70	dB
Total Harmonic Distortion	Test Circuit 1: R_L = 8 Ω, f = 1KHz P_{out} = 1W		0.2	%
	Test Circuit 2: R_L = 8 Ω, f = 1KHz P_{out} = 1W		1	%
Supply Current	R_L = 8 Ω P_{out} = 1.15W	170		mA
	R_L = 8 Ω P_{out} = 2.1		235	mA
The Following Specifications Apply for -40°C ≤ T_A ≤ 85°C:				
Quiescent Current of Output Transistors (I_O)		1.1	1.3	mA
Open Loop Voltage Gain	R_L = 8 Ω	67	70	dB
Total Harmonic Distortion	Test Circuit 1: R_L = 8 Ω, f = 1KHz P_{out} = 50mW	0.4	0.3	%
	R_L = 8 Ω, f = 1KHz, P_{out} = 0.5W	0.3		%
	Test Circuit 2: R_L = 8 Ω, f = 1KHz P_{out} = 50mW	1.7	1.5	%
	R_L = 8 Ω, f = 1KHz, P_{out} = 0.5W	1.2		%
Feedback Resistance	Pin 5 to 12	7.5	7.5	KΩ
Input Impedance	Open Loop	0.75	0.75	MΩ

TEST CIRCUIT 1 (A_V = 50)

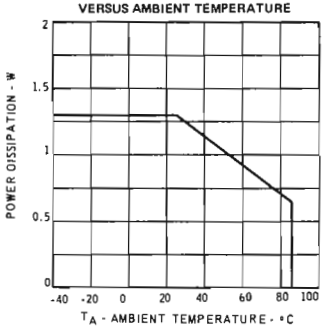


TEST CIRCUIT 2 (A_V = 250)

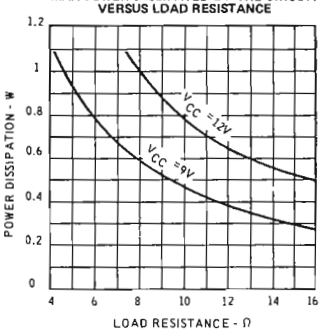


TYPICAL ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

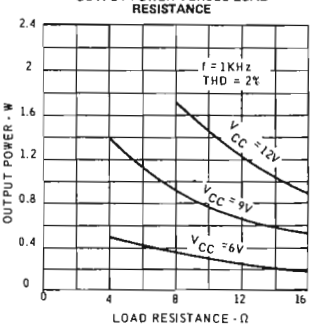
MAX ALLOWABLE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



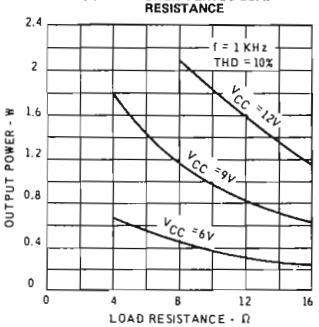
MAX POWER DISSIPATED BY THE CIRCUIT VERSUS LOAD RESISTANCE



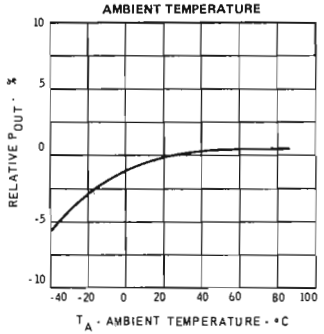
OUTPUT POWER VERSUS LOAD RESISTANCE



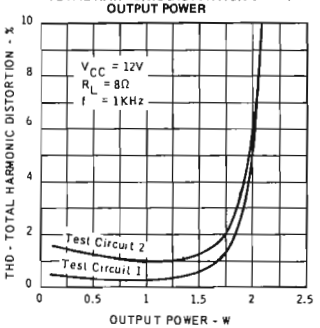
OUTPUT POWER VERSUS LOAD RESISTANCE



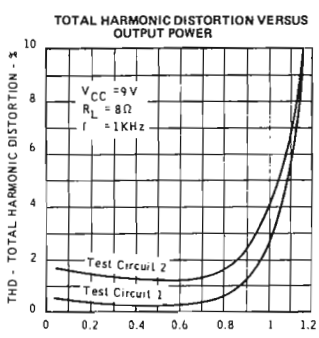
VARIATION OF P_{OUT} VERSUS AMBIENT TEMPERATURE



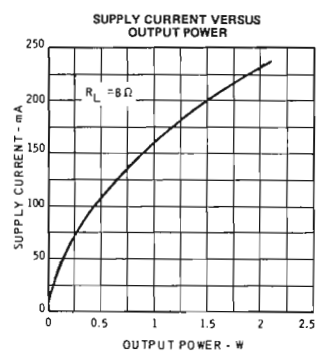
TOTAL HARMONIC DISTORTION VERSUS OUTPUT POWER



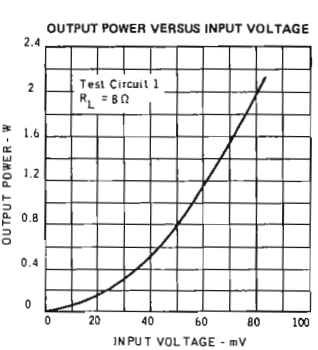
TOTAL HARMONIC DISTORTION VERSUS OUTPUT POWER



SUPPLY CURRENT VERSUS OUTPUT POWER

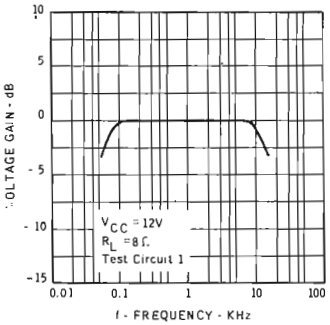


OUTPUT POWER VERSUS INPUT VOLTAGE

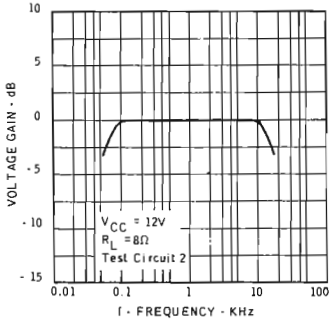


TYPICAL ELECTRICAL CHARACTERISTICS (25 °C free air temperature unless otherwise noted)

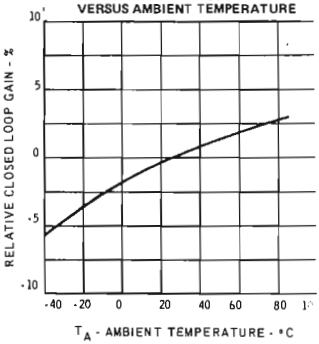
RELATIVE VOLTAGE GAIN VERSUS FREQUENCY



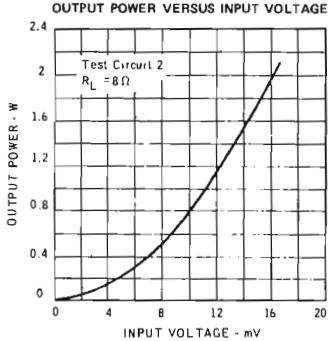
VOLTAGE GAIN VERSUS FREQUENCY



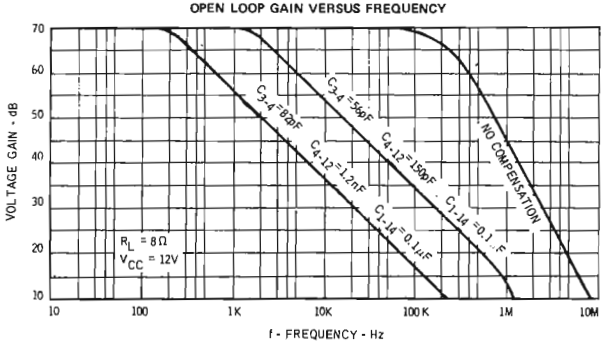
VARIATION OF CLOSED LOOP RELATIVE VERSUS AMBIENT TEMPERATURE



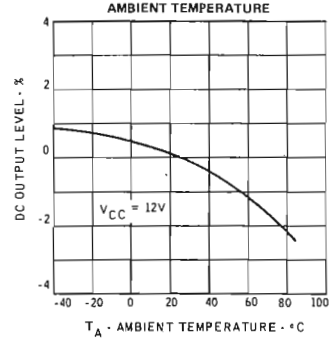
OUTPUT POWER VERSUS INPUT VOLTAGE



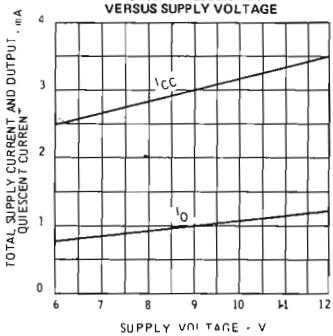
OPEN LOOP GAIN VERSUS FREQUENCY



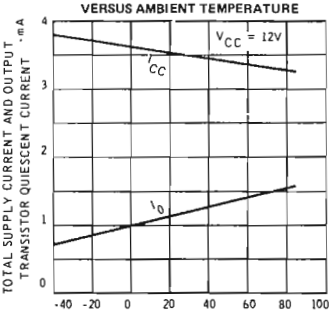
VARIATION OF DC OUTPUT LEVEL VERSUS AMBIENT TEMPERATURE



TOTAL SUPPLY CURRENT AND OUTPUT TRANSISTOR QUIESCENT CURRENT VERSUS SUPPLY VOLTAGE



TOTAL SUPPLY CURRENT AND OUTPUT TRANSISTOR QUIESCENT CURRENT VERSUS AMBIENT TEMPERATURE

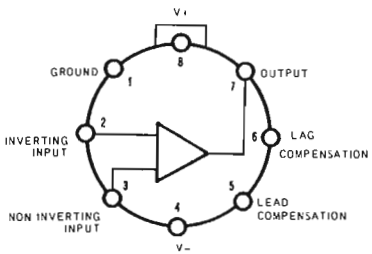


high gain, wideband dc amplifier

EXTENDED TEMPERATURE RANGE, −55°C ÷ 125°C

The µA702A is a complete DC amplifier constructed on a single silicon chip, using the Planar epitaxial process. It is intended for use as an operational amplifier in high speed analog computers, as a precision instrumentation amplifier, or in other applications requiring a feedback amplifier useful from DC to 30 MHz.

CONNECTION DIAGRAM
(Top View)



Note : Pin 4 connected to case

ORDERING NUMBER
U5B771231X

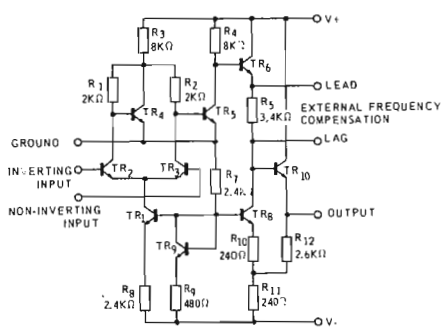
ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Total Supply Voltage Between V + and V− Terminals	21 V
Peak Load Current	50 mA
Internal Power Dissipation (Note 1)	300 mW
Storage Temperature Range	-65°C to + 150°C
Operating Temperature Range	-55°C to + 125°C
Differential Input Voltage	± 5 V
Input Voltage, Either Input	+ 1.5 V to -6V
Lead Temperature (Soldering, 60 sec)	300°C

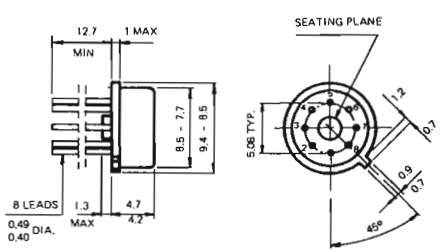
NOTE :

(1) Rating applies for case temperatures to 125°C; derate linearly at 6.6 mW/°C for ambient temperatures above 105°C.

SCHEMATIC DIAGRAM



PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-99 outline



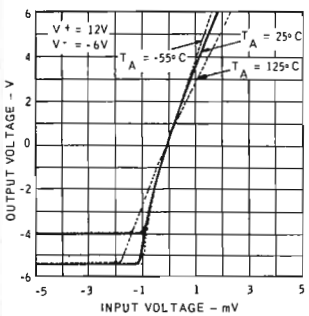
Notes: All dimensions in mm.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

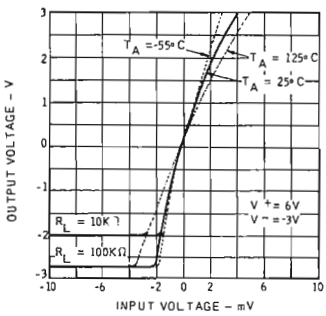
PARAMETER (see definitions)	CONDITIONS	V+ = 12V, V⁻ = -6 V			V+ = 6 V, V⁻ = -3V			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Offset Voltage	$R_S \leq 2\ k\Omega$		0.5	2		0.7	3	mV
Input Offset Current			180	500		120	500	nA
Input Bias Current			2	5		1.2	3.5	μA
Input Resistance		16	40		22	67		kΩ
Input Voltage Range		-4		0.5	-1.5		0.5	V
Common Mode Rejection Ratio	$R_S \leq 2\ k\Omega$, $f \leq 1$ kHz	80	100		80	100		dB
Large-Signal Voltage Gain	$R_L \geq 100\ k\Omega$, $V_{out} = \pm 5V$	2500	3600	6000				
	$R_L \geq 100\ k\Omega$, $V_{out} = \pm 2.5V$				600	900	1500	
Output Resistance			200	500		300	700	Ω
Supply Current	$V_{out} = 0$		5	6.7		2.1	3.3	mA
Power Consumption	$V_{out} = 0$		90	120		19	30	mW
Transient Response (unity-gain)	$C_1 = 0{,}01\ \mu F$, $R_1 = 20\ \Omega$, $R_L \geq 100\ k\Omega$, $V_{in} = 10$ mV							
Risetime			25	120				ns
Overshoot	$C_L = 100$ pF		10	50				%
Transient Response (x100 gain)	$C_3 = 50$ pF, $R_L = 100\ k\Omega$, $V_{in} = 1$ mV							
Risetime			10	30				ns
Overshoot			20	40				%
The following specifications apply for -55°C ≤ T_A ≤ 125°C:								
Input Offset Voltage	$R_S \leq 2\ k\Omega$			3			4	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\ \Omega$, T_A = 25°C to T_A = 125°C		2.5	10		3.5	15	μV/°C
	$R_S = 50\ \Omega$, T_A = 25°C to T_A = -55°C		2	10		3	15	μV/°C
Input Offset Current	T_A = 125°C		80	500		50	500	nA
	T_A = -55°C		400	1500		280	1500	nA
Average Temperature Coefficient of Input Offset Current	T_A = 25°C to T_A = 125°C		1	5		0.7	4	nA/°C
	T_A = 25°C to T_A = -55°C		3	16		2	13	nA/°C
Input Bias Current	T_A = -55°C		4.3	10		2.6	7.5	μA
Input Resistance		6			8			kΩ
Common Mode Rejection Ratio	$R_S \leq 2\ k\Omega$, $f \leq 1$ kHz	70	95		70	95		dB
Supply Voltage Rejection Ratio	V+ = 12V, V⁻ = -6 V to V+ = 6 V, V⁻ = -3 V, $R_S \leq 2$ KΩ		75	200		75	200	μV/V
Large-Signal Voltage Gain	$R_L \geq 100\ k\Omega$, $V_{out} = \pm 5V$	2000		7000				
	$R_L \geq 100\ k\Omega$, $V_{out} = \pm 2.5V$				500		1750	
Output Voltage Swing	$R_L \geq 100\ k\Omega$	±5	±5.3		±2.5	±2.7		V
	$R_L \geq 10\ k\Omega$	±3.5	±4		±1.5	±2		V
Supply Current	T_A = 125°C, $V_{out} = 0$		4.4	6.7		1.7	3.3	mA
	T_A = -55°C, $V_{out} = 0$		5	7.5		2.1	3.9	mA
Power Consumption	T_A = 125°C, $V_{out} = 0$		80	120		15	30	mW
	T_A = -55°C, $V_{out} = 0$		90	135		19	35	mW

TYPICAL ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

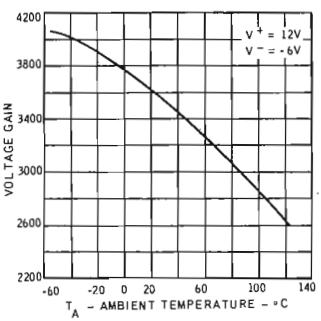
VOLTAGE TRANSFER CHARACTERISTIC



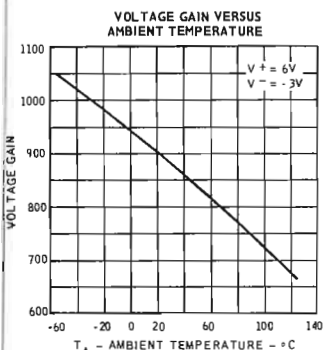
VOLTAGE TRANSFER CHARACTERISTIC



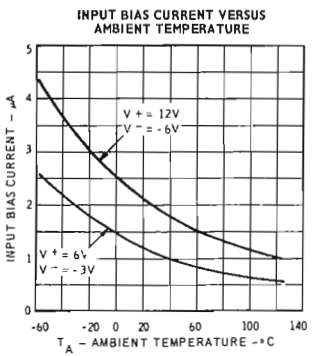
VOLTAGE GAIN VERSUS AMBIENT TEMPERATURE



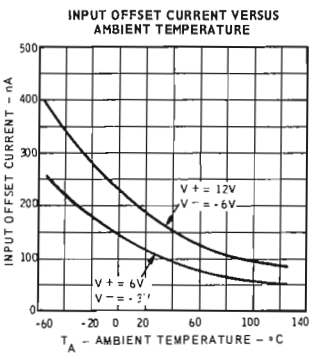
VOLTAGE GAIN VERSUS AMBIENT TEMPERATURE



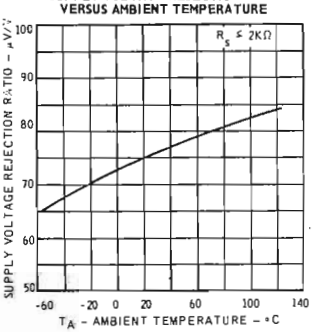
INPUT BIAS CURRENT VERSUS AMBIENT TEMPERATURE



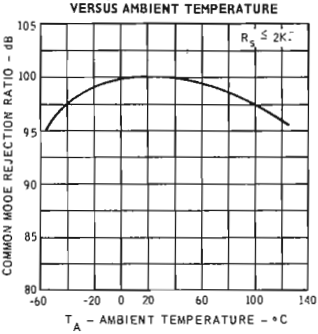
INPUT OFFSET CURRENT VERSUS AMBIENT TEMPERATURE



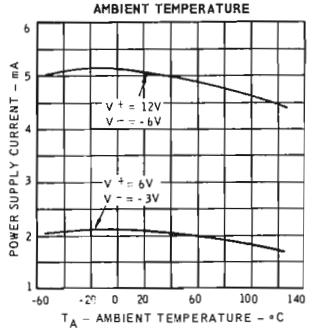
SUPPLY VOLTAGE REJECTION RATIO VERSUS AMBIENT TEMPERATURE



COMMON MODE REJECTION RATIO VERSUS AMBIENT TEMPERATURE

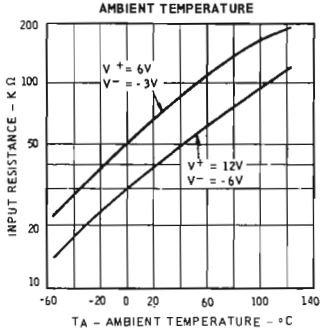


POWER SUPPLY CURRENT VERSUS AMBIENT TEMPERATURE

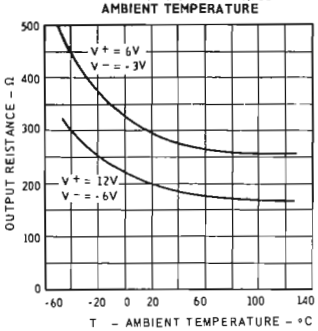


TYPICAL ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

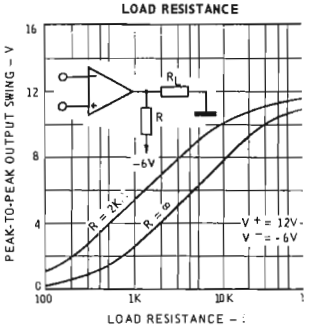
INPUT RESISTANCE VERSUS AMBIENT TEMPERATURE



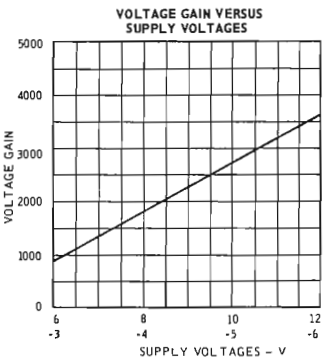
OUTPUT RESISTANCE VERSUS AMBIENT TEMPERATURE



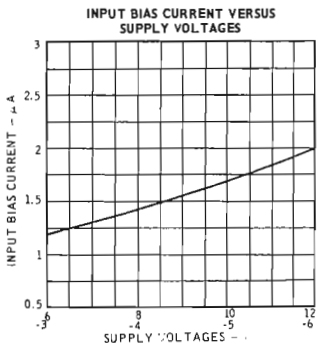
OUTPUT VOLTAGE SWING VERSUS LOAD RESISTANCE



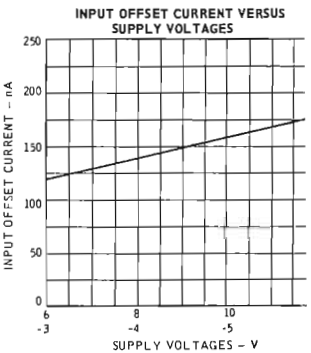
VOLTAGE GAIN VERSUS SUPPLY VOLTAGES



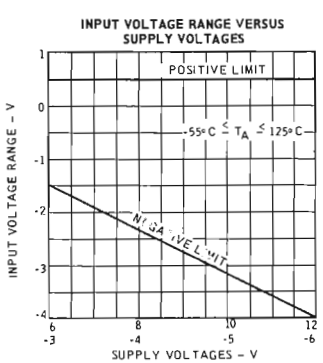
INPUT BIAS CURRENT VERSUS SUPPLY VOLTAGES



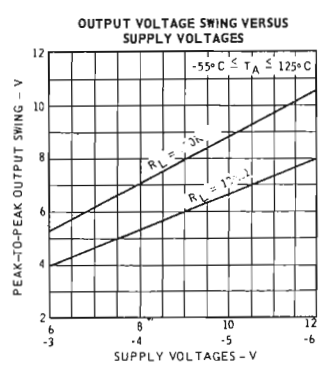
INPUT OFFSET CURRENT VERSUS SUPPLY VOLTAGES



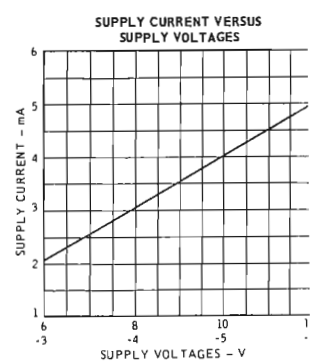
INPUT VOLTAGE RANGE VERSUS SUPPLY VOLTAGES



OUTPUT VOLTAGE SWING VERSUS SUPPLY VOLTAGES

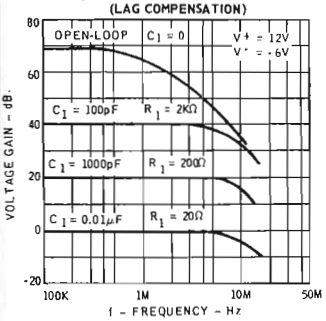


SUPPLY CURRENT VERSUS SUPPLY VOLTAGES

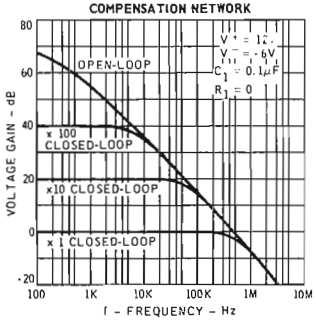


TYPICAL ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

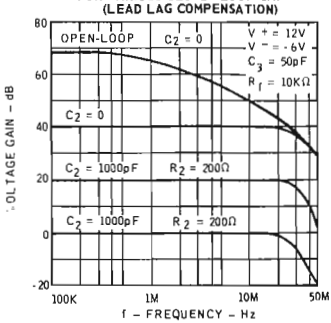
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LAG COMPENSATION)



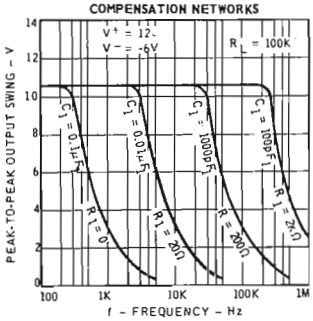
FREQUENCY RESPONSE WITH CONSERVATIVE COMPENSATION NETWORK



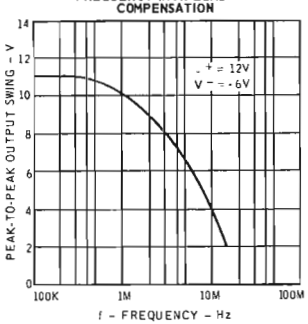
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LEAD LAG COMPENSATION)



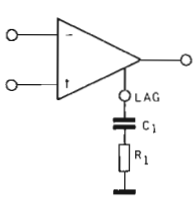
OUTPUT VOLTAGE SWING VERSUS FREQUENCY FOR VARIOUS LAG COMPENSATION NETWORKS



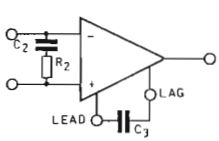
OUTPUT VOLTAGE SWING VERSUS FREQUENCY WITH LEAD-LAG COMPENSATION



FREQUENCY COMPENSATION CIRCUITS



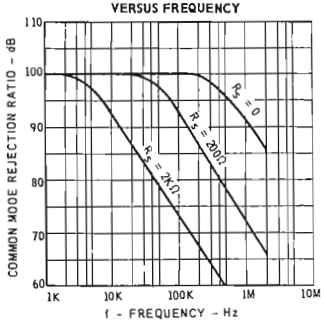
LAG COMPENSATION



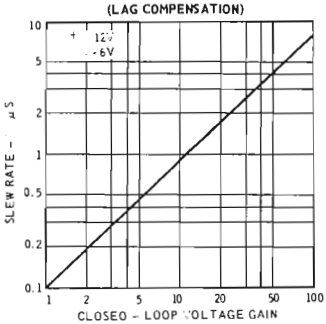
LEAD-LAG COMPENSATION

TYPICAL ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

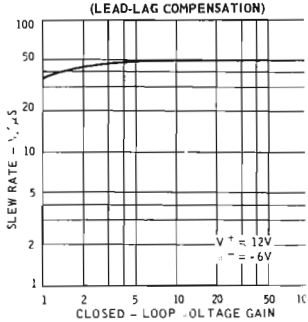
COMMON MODE REJECTION RATIO VERSUS FREQUENCY



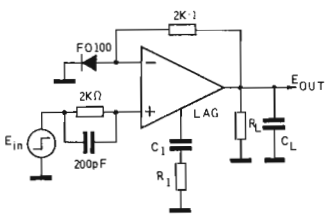
SLEW RATE VERSUS CLOSED-LOOP VOLTAGE GAIN (LAG COMPENSATION)



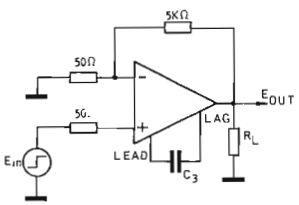
SLEW RATE VERSUS CLOSED-LOOP VOLTAGE GAIN (LEAD-LAG COMPENSATION)



TRANSIENT RESPONSE TEST CIRCUIT

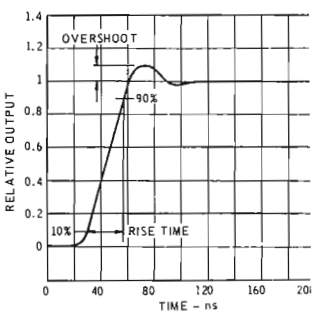


UNITY-GAIN AMPLIFIER
(LAG COMPENSATION)



X 100 AMPLIFIER
(LEAD COMPENSATION)

TRANSIENT RESPONSE



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE - That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT - The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE - The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT - The average of the two input currents.

INPUT VOLTAGE RANGE - The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly

INPUT COMMON MODE REJECTION RATIO - The ratio of the input voltage range to the maximum change in input offset voltage over this range

SUPPLY VOLTAGE REJECTION RATIO - The ratio of the change in input offset voltage to the change in supply voltage producing it.

LARGE-SIGNAL VOLTAGE GAIN - The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING - The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE - The resistance seen looking into the output terminal with the output et null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

POWER CONSUMPTION - The DC power required to operate the amplifier with the output at zero and with no load current.

TRANSIENT RESPONCE - The closed - loop step - function response of the amplifier under small - signal conditions.

PEAK OUTPUT CURRENT - The maximum current that may flow in the output load without causing damage to the unit.

High gain, wideband dc amplifier

STANDARD TEMPERATURE RANGE, 0°C to 70°C

- HIGH GAIN
- WIDEBAND (DC to 30 MHz)

The μA702C is a complete DC amplifier constructed on a single silicon chip, using the planar epitaxial process. It is intended for use as an operational amplifier in high speed analogue computers, as a precision instrumentation amplifier, or in other applications requiring a feedback amplifier usable from DC to 30 MHz. For full temperature range operation (-55°C to 125°C) see μA702A data sheet.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

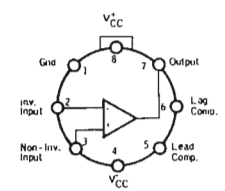
Total Supply Voltage Between V_{CC}^+ and V_{CC}^- Terminals	21 V
Peak Load Current	50 mA
Internal Power Dissipation (see note)	300 mW
Storage Temperature Range	-55°C to + 150°C
Operating Temperature Range	0°C to + 70°C
Differential Input Voltage	± 5 V
Input Voltage, Either Input	+ 1.5V to - 6 V
Lead Temperature	
(Soldering 60 sec. for package No. 1)	300°C
(Soldering 10 sec. for package No. 2)	260°C

Note : rating applies for ambient temperature to 70°C.

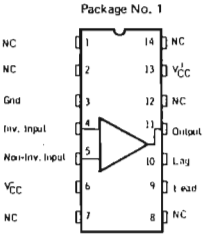
ORDERING NUMBERS

U5B771239X (for package No. 1)
U6E7712393 (for package No. 2)

CONNECTION DIAGRAMS
(top views)

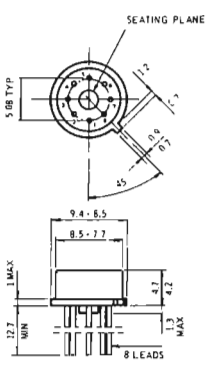


Package No. 1



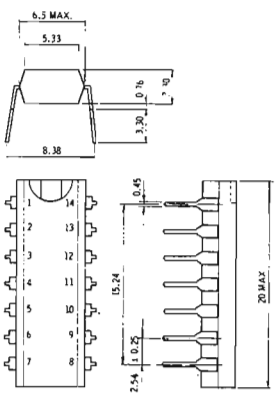
Package No. 2

PACKAGE No. 1
PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-99 outline



Note. all dimensions in mm.

PACKAGE No. 2
PHYSICAL DIMENSIONS
14-pin plastic DIP

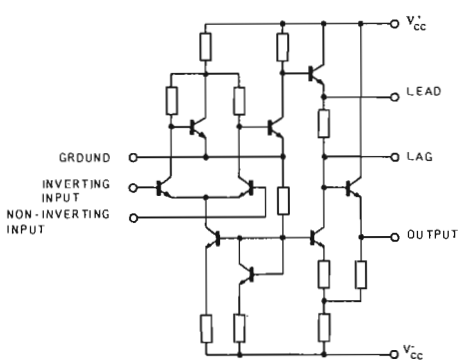


Note: all dimensions in mm.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

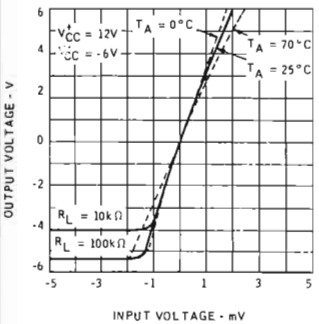
PARAMETER	CONDITIONS	V_{CC}^+=12V, V_{CC}^-=-6V			V_{CC}^+= 6V, V_{CC}^-= - 3V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage	$R_S \leq$ 2 kΩ		± 1.5	±5		± 1.7	± 6	mV
Input Offset Current			± 0.5	±2		± 0.3	± 2	μA
Input Bias Current			2.5	7.5		1.5	5	μA
Input Resistance		10	32		16	55		kΩ
Input Voltage Range		-4		+ 0.5	-1.5		+ 0.5	V
Common Mode Rejection Ratio	$R_S \leq$ 2 kΩ, f ≤ 1 kHz	70	92		70	92		dB
Large-Signal Voltage Gain	$R_L \geq$ 100 kΩ, V_{OUT}= ± 5V	2000	3400	6000				
	$R_L \geq$ 100 kΩ, V_{OUT}= ± 2.5V				500	800	1500	
Output Resistance			200	600		300	800	Ω
Supply Current	V_{OUT} = 0		5	6.7		2.1	3.3	mA
Power Consumption	V_{OUT} = 0		90	120		19	30	mW
Transient Response (unity gain):	$R_L \leq$ 100 kΩ, V_{IN}=20mV, $C_L \leq$100pF							
Rise Time	C_1= 0.01 μF, R_1 = 20 Ω		25	120				ns
Overshoot			10	50				%
Transient Response (x 100 gain):	C_3=50 pF, $R_L \geq$100kΩ, V_{IN}=1 mV							
Rise Time			10	30				ns
Overshoot			20	40				%
The following specifications apply for 0°C ≤ T_A ≤ 70°C :								
Input Offset Voltage	$R_S \leq$ 2 kΩ			±6.5			±7.5	mV
Average Temperature Coefficient of Input Offset Voltage	T_A=70°C to T_A= 0°C, R_S=50 Ω		5	20		7.5	25	μV/°C
Input Offset Current				2.5			2.5	μA
Average Temperature Coefficient of Input Offset Current	T_A=25°C to T_A= 70°C		4	10		3	8	nA/°C
	T_A=25°C to T_A= 0°C		6	20		5.5	18	nA/°C
Input Bias Current	T_A= 0°C		4	12		2.7	8	μA
Input Resistance		6	18		9	27		kΩ
Common Mode Rejection Ratio	$R_S \leq$ 2 kΩ, f ≤ 1 kHz	65	86		65	86		dB
Supply Voltage Rejection Ratio	V_{CC}^+=12V, V_{CC}^-=-6V, to V_{CC}^+=6V, V_{CC}^-=-3V, $R_S \leq$ 2 kΩ		90	300		90	300	μV/ V
Large-Signal Voltage Gain	$R_L \geq$100 kΩ, V_{OUT}= ± 5V	1500		7000				
	$R_L \geq$ 100 kΩ, V_{OUT}= ± 2.5V				400		1750	
Output Voltage Swing	$R_L \geq$ 100 kΩ	± 5	± 5.3		±2.5	±2.7		V
	$R_L \geq$ 10 kΩ	±3.5	± 4		±1.5	± 2		V
Supply Current	V_{OUT} = 0		5	7		2.1	3.9	mA
Power Consumption	V_{OUT} = 0		90	125		19	35	mW

EQUIVALENT CIRCUIT

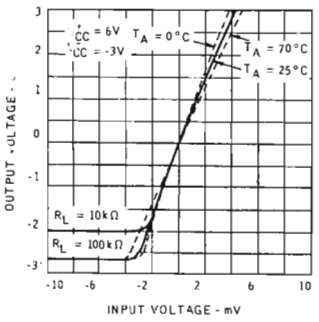


TYPICAL ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

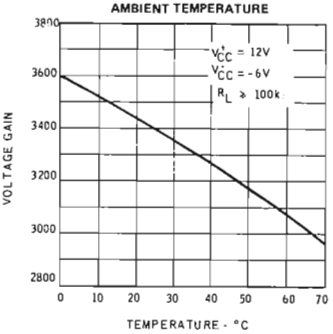
VOLTAGE TRANSFER CHARACTERISTIC



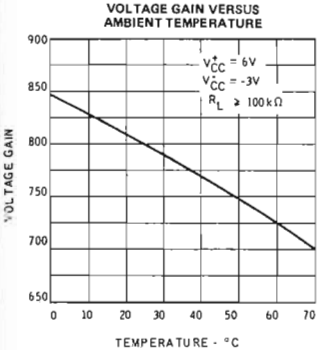
VOLTAGE TRANSFER CHARACTERISTIC



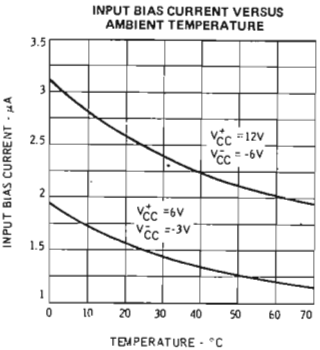
VOLTAGE GAIN VERSUS AMBIENT TEMPERATURE



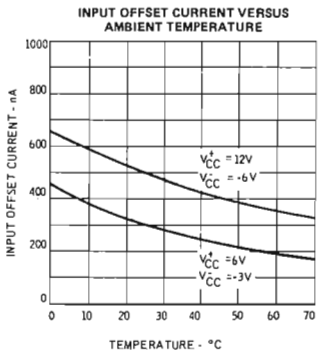
VOLTAGE GAIN VERSUS AMBIENT TEMPERATURE



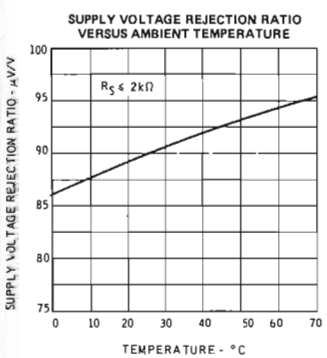
INPUT BIAS CURRENT VERSUS AMBIENT TEMPERATURE



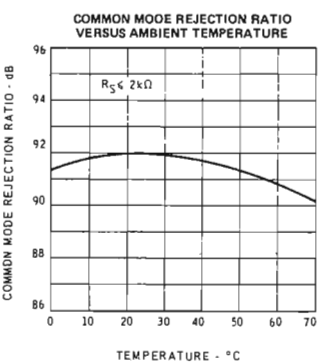
INPUT OFFSET CURRENT VERSUS AMBIENT TEMPERATURE



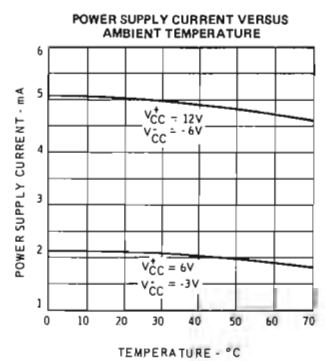
SUPPLY VOLTAGE REJECTION RATIO VERSUS AMBIENT TEMPERATURE



COMMON MODE REJECTION RATIO VERSUS AMBIENT TEMPERATURE

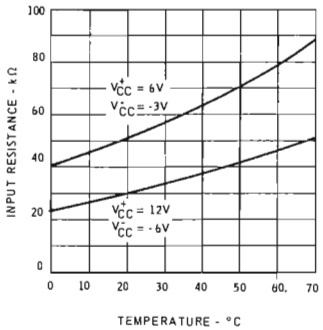


POWER SUPPLY CURRENT VERSUS AMBIENT TEMPERATURE

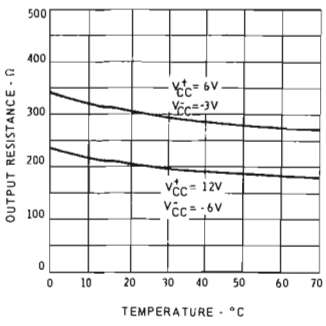


TYPICAL ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

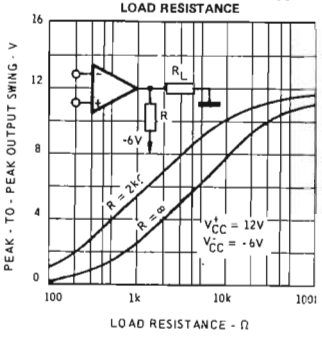
INPUT RESISTANCE VERSUS AMBIENT TEMPERATURE



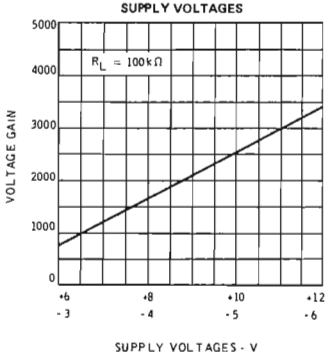
OUTPUT RESISTANCE VERSUS AMBIENT TEMPERATURE



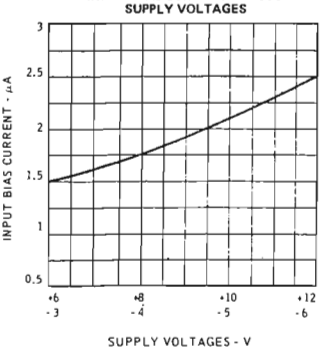
OUTPUT VOLTAGE SWING VERSUS LOAD RESISTANCE



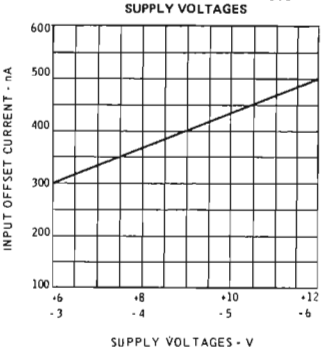
VOLTAGE GAIN VERSUS SUPPLY VOLTAGES



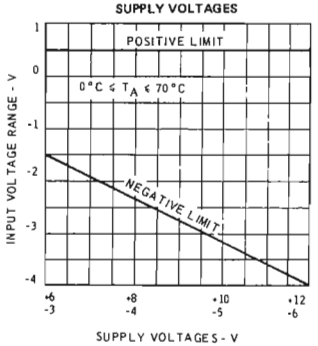
INPUT BIAS CURRENT VERSUS SUPPLY VOLTAGES



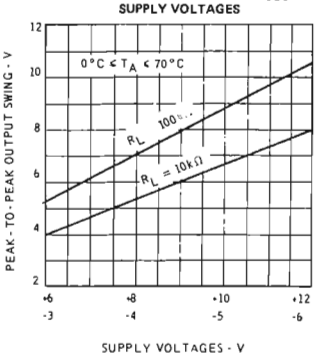
INPUT OFFSET CURRENT VERSUS SUPPLY VOLTAGES



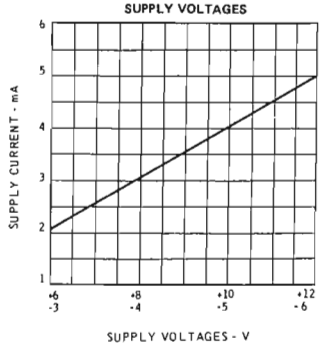
INPUT VOLTAGE RANGE VERSUS SUPPLY VOLTAGES



OUTPUT VOLTAGE SWING VERSUS SUPPLY VOLTAGES

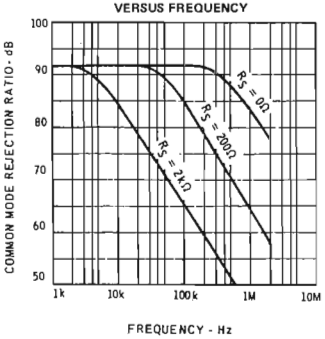


SUPPLY CURRENT VERSUS SUPPLY VOLTAGES

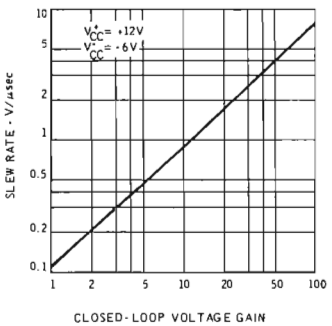


TYPICAL ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

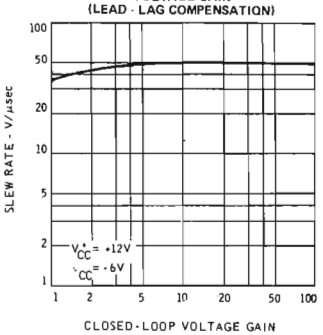
COMMON MODE REJECTION RATIO VERSUS FREQUENCY



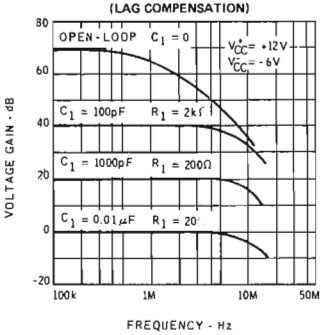
SLEW RATE VERSUS CLOSED-LOOP VOLTAGE GAIN (LAG COMPENSATION)



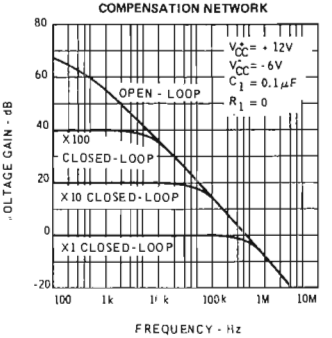
SLEW RATE VERSUS CLOSED-LOOP VOLTAGE GAIN (LEAD-LAG COMPENSATION)



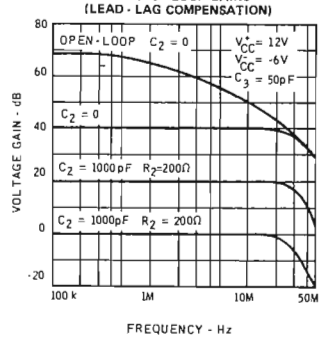
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LAG COMPENSATION)



FREQUENCY RESPONSE WITH CONSERVATIVE COMPENSATION NETWORK

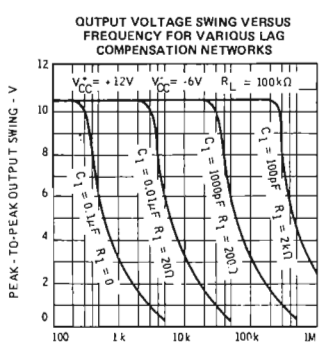


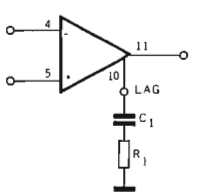
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LEAD-LAG COMPENSATION)



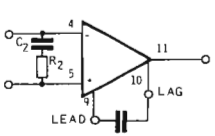
FREQUENCY COMPENSATION CIRCUITS

OUTPUT VOLTAGE SWING VERSUS FREQUENCY FOR VARIOUS LAG COMPENSATION NETWORKS



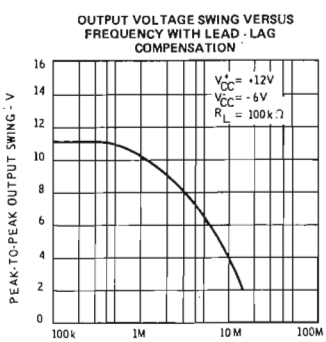


LAG COMPENSATION

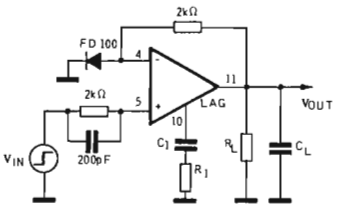


LEAD-LAG COMPENSATION

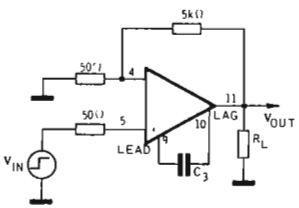
OUTPUT VOLTAGE SWING VERSUS FREQUENCY WITH LEAD-LAG COMPENSATION



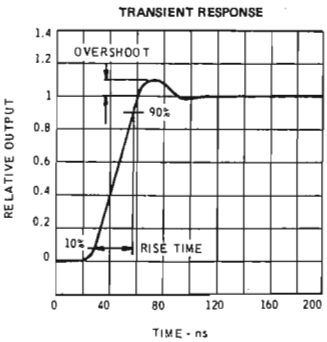
TRANSIENT RESPONSE TEST CIRCUITS



UNITY-GAIN AMPLIFIER
(LAG COMPENSATION)



X 100 AMPLIFIER
(LEAD COMPENSATION)



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE – That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT – The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE – The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT – The average of the two input currents.

INPUT VOLTAGE RANGE – The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO – The ratio of the input voltage range to the maximum change in input offset voltage over this range.

SUPPLY VOLTAGE REJECTION RATIO – The ratio of the change in input offset voltage to the change in supply voltage producing it.

LARGE-SIGNAL VOLTAGE GAIN – The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING – The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE – The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

POWER CONSUMPTION – The DC power required to operate the amplifier with the output at zero and with no load current.

TRANSIENT RESPONSE – The closed-loop step-function response of the amplifier under small-signal conditions.

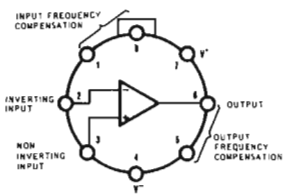
PEAK OUTPUT CURRENT – The maximum current that may flow in the output load without causing damage to the unit.

high performance operational amplifier

EXTENDED TEMPERATURE RANGE, – 55°C + 125°C

The μA709 is a High-Gain Operational amplifier constructed on a single silicon chip using the Planar epitaxial process. It features low offset, high input impedance, large input common mode range, high output swing under load and low power consumption. The device displays exceptional temperature stability and will operate over a wide range of supply voltages with little degradation of performance. The amplifier is intended for use in DC servo systems, high impedance analog computers, in low-level instrumentation applications and for the generation of special linear and nonlinear transfer functions.

CONNECTION DIAGRAM
(Top view)



Note : Pin 4 connected to case.

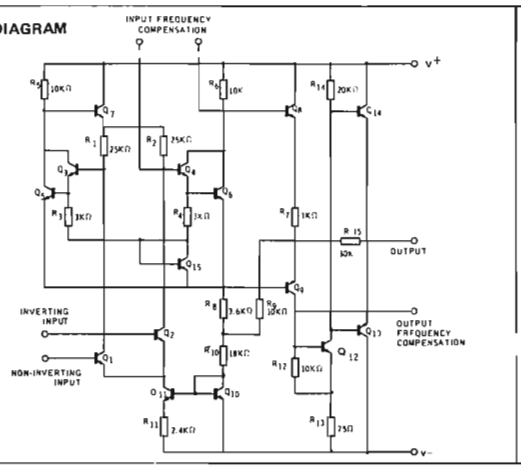
ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Supply Voltage	± 18 V
Internal Power Dissipation (Note 1)	300 mW
Differential Input Voltage	± 5 V
Input Voltage	± 10 V
Output Short-Circuit Duration ($T_A = 25°C$)	5 sec
Storage Temperature Range	-65°C to + 150°C
Operating Ambient Temperature Range	-55°C to + 125°C
Lead Temperature (Soldering, 60 sec)	300°C

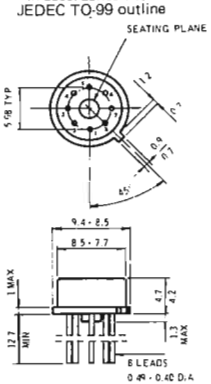
ORDERING NUMBER
U5B770931X

NOTE 1 : Rating applies for case temperatures to + 125°C; derate linearly at 5.5 mW/°C for ambient temperature above + 95°C.

SCHEMATIC DIAGRAM



PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-99 outline



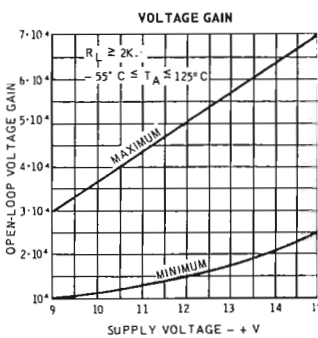
Note: all dimensions in mm.

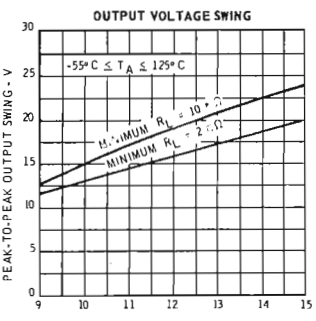
ELECTRICAL CHARACTERISTICS ($T_A = +25°C$, $\pm 9\ V \leq V_S \leq \pm 15\ V$ unless otherwise noted)

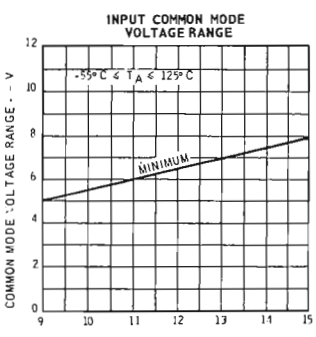
PARAMETER (see definitions)	CONDITIONS	Min.	Typ.	Max.	UNIT
Input Offset Voltage	$R_S \leq 10\ K\Omega$		1	5	mV
Input Offset Current			50	200	nA
Input Bias Current			200	500	nA
Input Resistance		150	400		KΩ
Output Resistance			150		Ω
Power Consumption	$V_S = \pm 15V$		80	165	mW
Transient Response	$V_{IN} = 20\ mV$, $R_L = 2\ K\Omega$,				
Risetime	$C_1 = 5000\ pF$, $R_1 = 1.5\ K\Omega$, $C_2 = 200\ pF$, $R_2 = 50\ \Omega$		0.3	1	μs
Overshoot	$C_L \leq 100\ pF$		10	30	%
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage	$R_S \leq 10\ K\Omega$			6	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\ \Omega$		3		μV/°C
	$R_S \leq 10\ K\Omega$		6		μV/°C
Large - Signal Voltage Gain	$V_S = \pm 15\ V$, $R_L \geq 2\ K\Omega$, $V_{OUT} = \pm 10\ V$	25,000	45,000	70,000	
Output Voltage Swing	$V_S = \pm 15V$, $R_L \geq 10\ K\Omega$	± 12	± 14		V
	$V_S = \pm 15V$, $R_L \geq 2\ K\Omega$	± 10	± 13		V
Input Voltage Range	$V_S = \pm 15\ V$	± 8	± 10		V
Common Mode Rejection Ratio	$R_S \leq 10\ K\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ K\Omega$		25	150	μV/C
Input Offset Current	$T_A = +125°C$		20	200	nA
	$T_A = -55°C$		100	500	nA
Input Bias Current	$T_A = -55°C$		0.5	1.5	μA
Input Resistance		40	100		KΩ

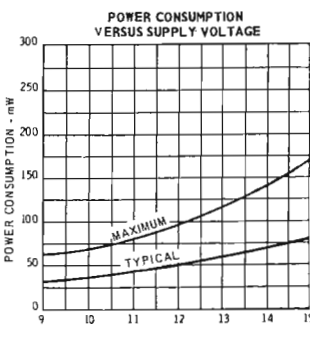
GUARANTEED ELECTRICAL CHARACTERISTICS

(25°C free air temperature unless otherwise noted)



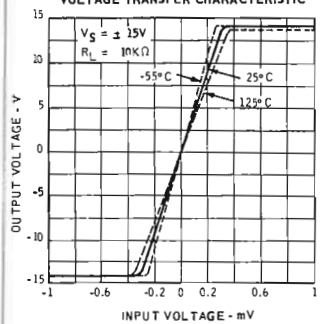




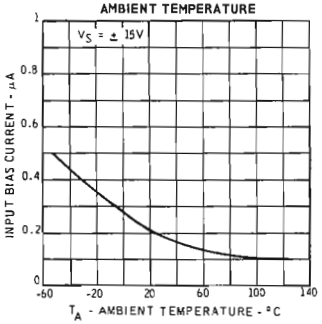


TYPICAL ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

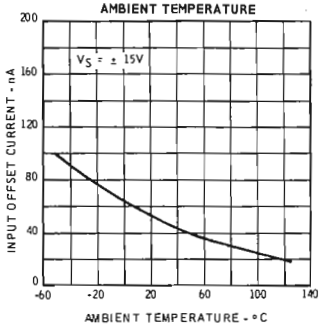
VOLTAGE TRANSFER CHARACTERISTIC



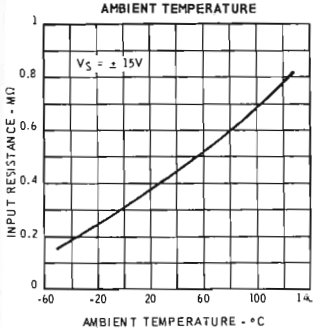
INPUT BIAS CURRENT VERSUS AMBIENT TEMPERATURE



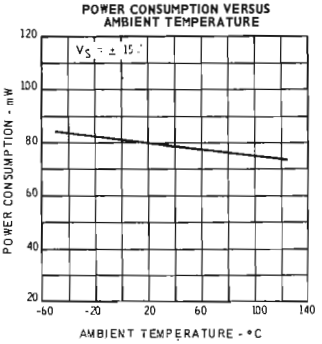
INPUT OFFSET CURRENT VERSUS AMBIENT TEMPERATURE



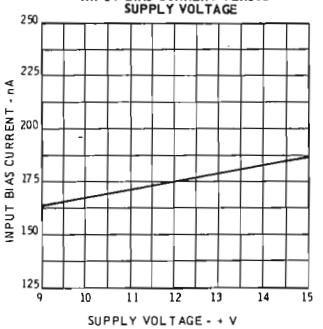
INPUT RESISTANCE VERSUS AMBIENT TEMPERATURE



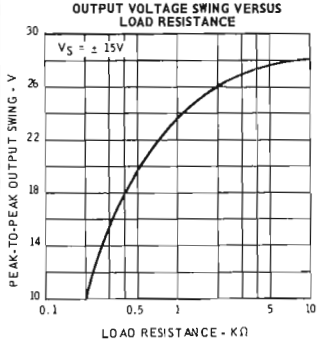
POWER CONSUMPTION VERSUS AMBIENT TEMPERATURE



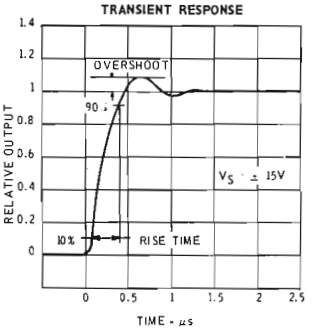
INPUT BIAS CURRENT VERSUS SUPPLY VOLTAGE



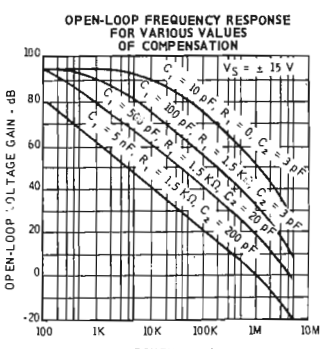
OUTPUT VOLTAGE SWING VERSUS LOAD RESISTANCE



TRANSIENT RESPONSE

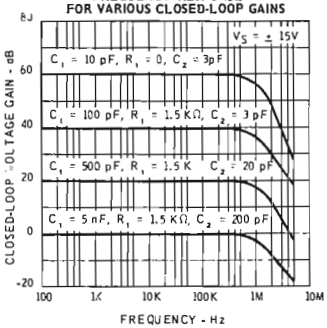


OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF COMPENSATION

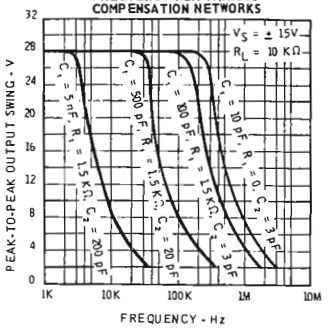


TYPICAL ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

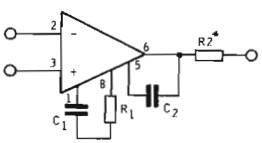
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS



OUTPUT VOLTAGE SWING VERSUS FREQUENCY FOR VARIOUS COMPENSATION NETWORKS

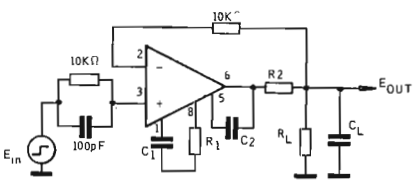


FREQUENCY COMPENSATION CIRCUIT



* Use R_2 = 50Ω when the amplifier is operated with capacitive loading

TRANSIENT RESPONSE TEST CIRCUIT



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE - That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT - The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE - The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT - The average of the two input currents.

INPUT VOLTAGE RANGE - A range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO - The ratio of the input voltage range to the maximum change in input offset voltage over this range.

LARGE-SIGNAL VOLTAGE GAIN - The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING - The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE - The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

POWER CONSUMPTION - The DC power required to operate the amplifier with the output at zero and with no load current.

SUPPLY VOLTAGE REJECTION RATIO - The ratio of the change in input offset voltage to the change in supply voltage producing it.

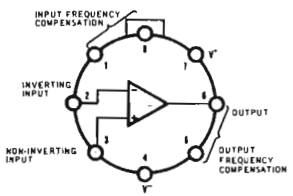
TRANSIENT RESPONSE - The closed - loop step function response of the amplifier under small - signal conditions.

high performance operational amplifier

EXTENDED TEMPERATURE RANGE, - 55°C + 125°C

The μA709A is a High-Gain Operational amplifier constructed on a single silicon chip using the Planar epitaxial process. It features low offset, high input impedance, large input common mode range, high output swing under load and low power consumption. The device displays exceptional temperature stability and will operate over a wide range of supply voltages with little degradation of performance. The amplifier is intended for use in DC servo systems, high impedance analog computers, in low-level instrumentation applications and for the generation of special linear and nonlinear transfer functions.

CONNECTION DIAGRAM
(Top view)



Note : Pin 4 connected to case.

ORDERING NUMBER

U5B 7709311

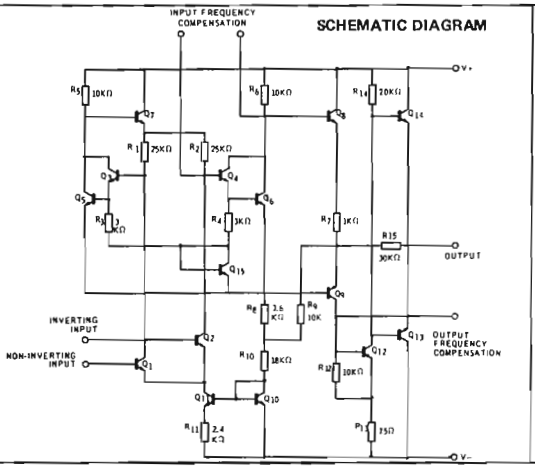
ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Supply Voltage	±18V
Internal Power Dissipation (Note 1)	300 mW
Differential Input Voltage	±5 V
Input Voltage	±10 V
Output Short - Circuit Duration ($T_A = 25°C$)	5 sec
Storage Temperature Range	- 65°C to 150°C
Operating Ambient Temperature Range	- 55°C to 125°C
Lead Temperature (Soldering, 60 sec)	300°C

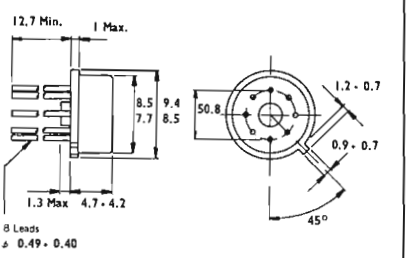
NOTE 1:

Rating applies for case temperatures to 125°C; derate linearly at 5.6 mW/°C for ambient temperatures above 95°C.

SCHEMATIC DIAGRAM



PHYSICAL DIMENSIONS
similar to
Jedec TO 99 outline



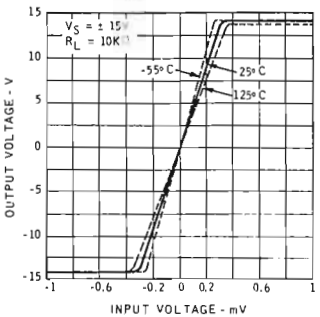
Notes All dimensions in mm.
Leads are gold-plated Kovar.

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $\pm 9\ V \leq V_S \leq \pm 15V$ unless otherwise specified)

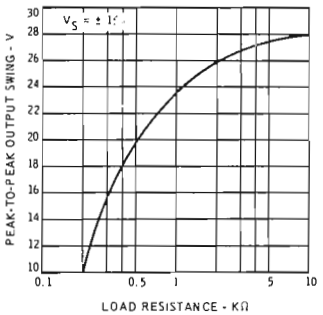
PARAMETER (see definitions)	CONDITIONS	Min.	Typ.	Max.	UNIT
Input Offset Voltage	$R_S \leq 10\ k\Omega$		0.6	2	mV
Input Offset Current			10	50	nA
Input Bias Current			100	200	nA
Input Resistance		350	700		kΩ
Output Resistance			150		Ω
Supply Current	$V_S = \pm 15\ V$		2.5	3.6	mA
Power Consumption	$V_S = \pm 15\ V$		75	108	mW
Transient Response	$V_S = \pm 15\ V$, $V_{IN} = 20\ mV$, $R_L = 2\ k\Omega$, $C_1 = 5\ nF$, $R_1 = 1.5\ k\Omega$, $C_2 = 200\ pF$, $R_2 = 50\ \Omega$				
Risetime				1.5	μsec
Overshoot	$C_L \leq 100\ pF$			30	%
The following specifications apply for $-55°C \leq T_A \leq 125°C$:					
Input Offset Voltage	$R_S \leq 10\ k\Omega$			3	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\ \Omega$, $T_A = 25°C$ to $T_A = 125°C$		1.8	10	μV/°C
	$R_S = 50\ \Omega$, $T_A = 25°C$ to $T_A = -55°C$		1.8	10	μV/°C
	$R_S = 10\ k\Omega$, $T_A = 25°C$ to $T_A = 125°C$		2	15	μV/°C
	$R_S = 10\ k\Omega$, $T_A = 25°C$ to $T_A = -55°C$		4.8	25	μV/°C
Input Offset Current	$T_A = 125°C$		3.5	50	nA
	$T_A = -55°C$		40	250	nA
Average Temperature Coefficient of Input Offset Current	$T_A = 25°C$ to $T_A = 125°C$		0.08	0.5	nA/°C
	$T_A = 25°C$ to $T_A = -55°C$		0.45	2.8	nA/°C
Input Bias Current	$T_A = -55°C$		300	600	nA
Input Resistance	$T_A = -55°C$	85	170		kΩ
Input Voltage Range	$V_S = \pm 15\ V$	± 8			V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	80	110		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$		40	100	μV/V
Large - Signal Voltage Gain	$V_S = \pm 15\ V$, $R_L \geq 2\ k\Omega$, $V_{OUT} = \pm 10V$	25,000		70,000	
Output Voltage Swing	$V_S = \pm 15V$, $R_L \geq 10\ k\Omega$	± 12	± 14		V
	$V_S = \pm 15\ V$, $R_L \geq 2\ k\Omega$	± 10	± 13		V
Supply Current	$T_A = 125°C$, $V_S = \pm 15\ V$		2.1	3	mA
	$T_A = -55°C$, $V_S = \pm 15\ V$		2.7	4.5	mA
Power Consumption	$T_A = 125°C$, $V_S = \pm 15\ V$		63	90	mW
	$T_A = -55°C$, $V_S = \pm 15\ V$		81	135	mW

TYPICAL ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

VOLTAGE TRANSFER CHARACTERISTIC

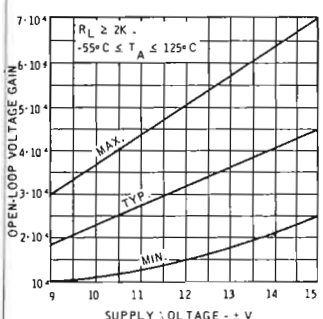


OUTPUT VOLTAGE SWING VERSUS LOAD RESISTANCE

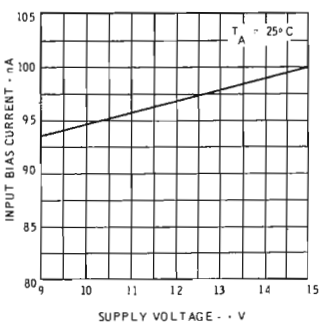


DC CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE

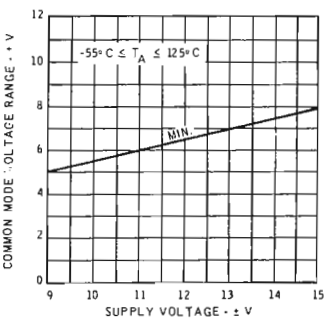
VOLTAGE GAIN



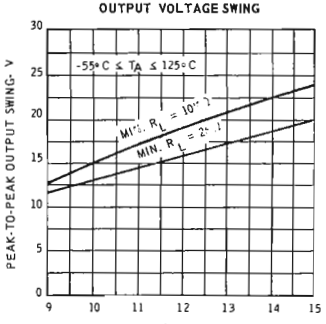
INPUT BIAS CURRENT VERSUS SUPPLY VOLTAGE



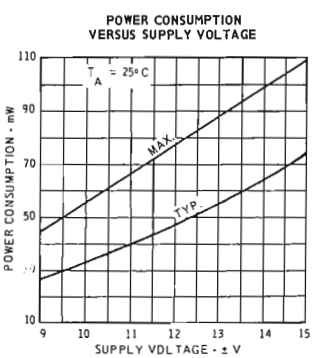
INPUT COMMON MODE VOLTAGE RANGE



OUTPUT VOLTAGE SWING

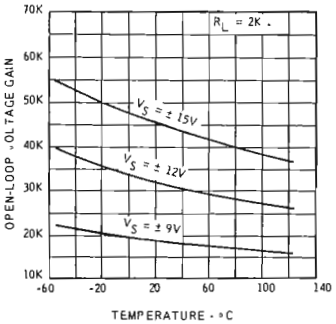


POWER CONSUMPTION VERSUS SUPPLY VOLTAGE

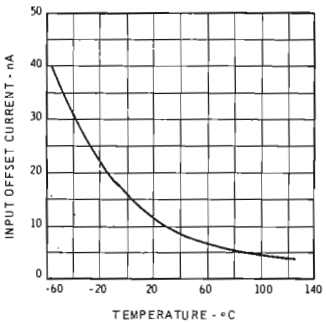


DC CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE

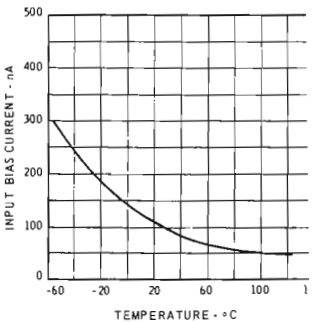
VOLTAGE GAIN VERSUS AMBIENT TEMPERATURE



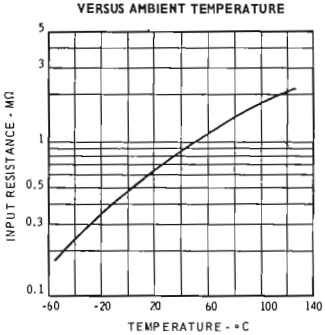
INPUT OFFSET CURRENT VERSUS AMBIENT TEMPERATURE



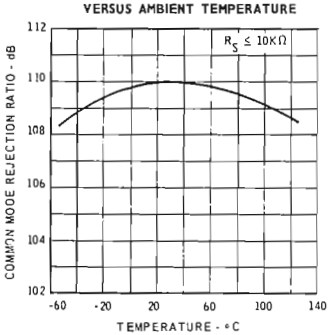
INPUT BIAS CURRENT VERSUS AMBIENT TEMPERATURE



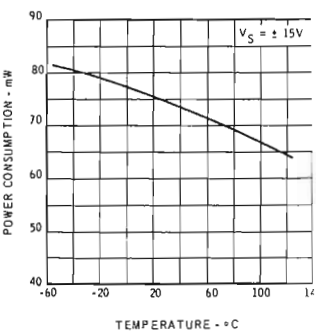
INPUT RESISTANCE VERSUS AMBIENT TEMPERATURE



COMMON MODE REJECTION RATIO VERSUS AMBIENT TEMPERATURE

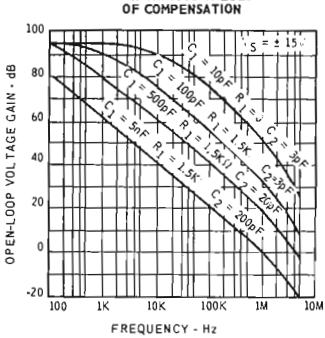


POWER CONSUMPTION VERSUS AMBIENT TEMPERATURE

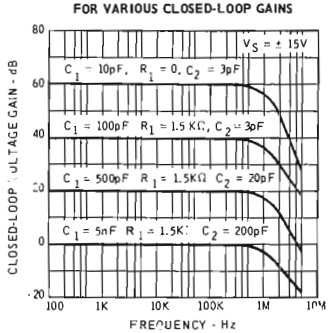


AC CHARACTERISTICS

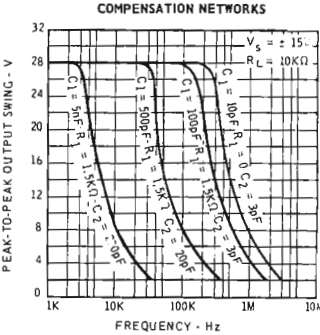
OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF COMPENSATION



FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS



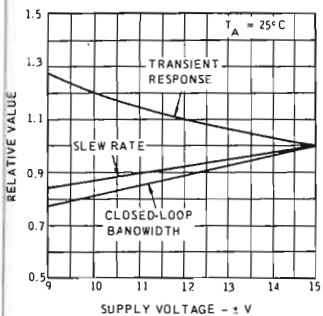
OUTPUT VOLTAGE SWING VERSUS FREQUENCY FOR VARIOUS COMPENSATION NETWORKS



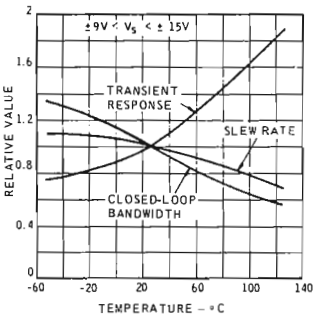
EXTENDED TEMPERATURE RANGE

AC CHARACTERISTICS

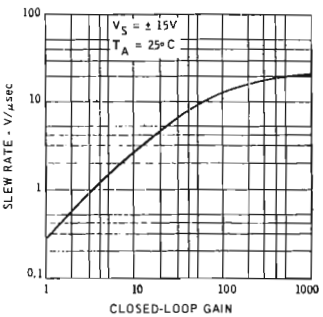
FREQUENCY CHARACTERISTICS VERSUS SUPPLY VOLTAGE



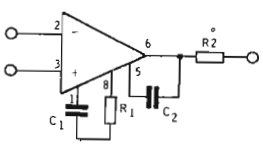
FREQUENCY CHARACTERISTICS VERSUS AMBIENT TEMPERATURE



SLEW RATE VERSUS CLOSED-LOOP GAIN USING RECOMMENDED COMPENSATION NETWORKS

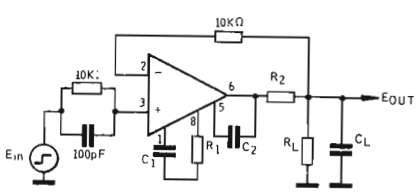


FREQUENCY COMPENSATION CIRCUIT

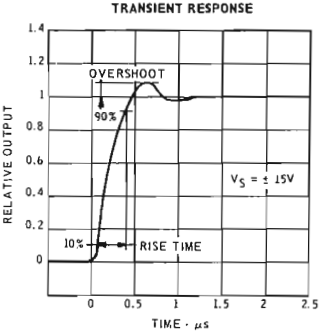


* Use R_2 = 50Ω when the amplifier is operated with capacitive loading

TRANSIENT RESPONSE TEST CIRCUIT



TRANSIENT RESPONSE



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE - That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT - The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE - The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT - The average of the two input currents.

INPUT VOLTAGE RANGE - A range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly

INPUT COMMON MODE REJECTION RATIO - The ratio of the input voltage range to the maximum change in input offset voltage over this range

LARGE-SIGNAL VOLTAGE GAIN - The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING - The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE - The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

POWER CONSUMPTION - The DC power required to operate the amplifier with the output at zero and with no load current.

SUPPLY VOLTAGE REJECTION RATIO - The ratio of the change in input offset voltage to the change in supply voltage producing it.

TRANSIENT RESPONSE - The closed - loop step function response of the amplifier under small - signal conditions.

High performance operational amplifier

STANDARD TEMPERATURE RANGE
0°C to 70°C

- LOW OFFSET
- HIGH INPUT IMPEDANCE
- LOW POWER CONSUMPTION

The μA709C is a high-gain operational amplifier constructed on a single silicon chip using the planar epitaxial process. It features low offset, high input impedance, large input common mode range, high output swing under load and low power consumption. The device displays exceptional temperature stability and will operate over a wide range of supply voltages with little degradation of performance. The amplifier is intended for use in DC servo systems, high impedance analogue computers, in low-level instrumentation applications and for the generation of special linear and nonlinear transfer functions. For full temperature range operation (-55°C to +125°C) see μa709 data sheet.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

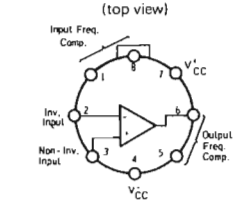
Supply Voltage	± 18 V
Internal Power Dissipation (see note)	300 mW
Differential Input Voltage	± 5 V
Input Voltage	± 10 V
Output Short-Circuit Duration (T_A=25°C)	5 sec
Storage Temperature Range	-55°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
(Soldering 60 sec for package No. 1)	300°C
(Soldering 10 sec for package No. 2)	260°C

Note : rating applies for ambient temperature to + 70°C

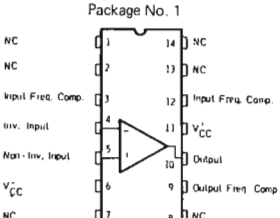
ORDERING NUMBERS

U5B770939X (for package No. 1)
U6E7709393 (for package No. 2)

CONNECTION DIAGRAMS
(top view)

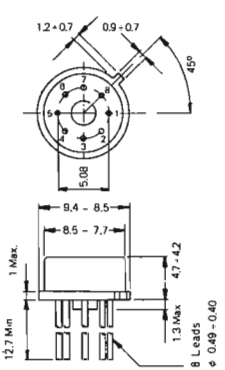


Package No. 1



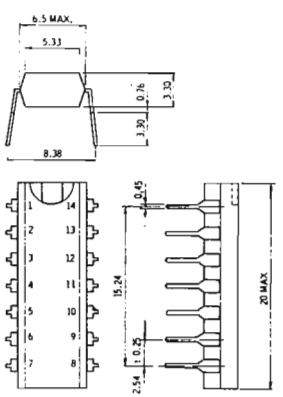
Package No. 2

PACKAGE No. 1
PHYSICAL DIMENSIONS
similar to
Jedec TO 99 outline



Note : All dimensions in mm.

PACKAGE No. 2
PHYSICAL DIMENSIONS
14-pin plastic DIP

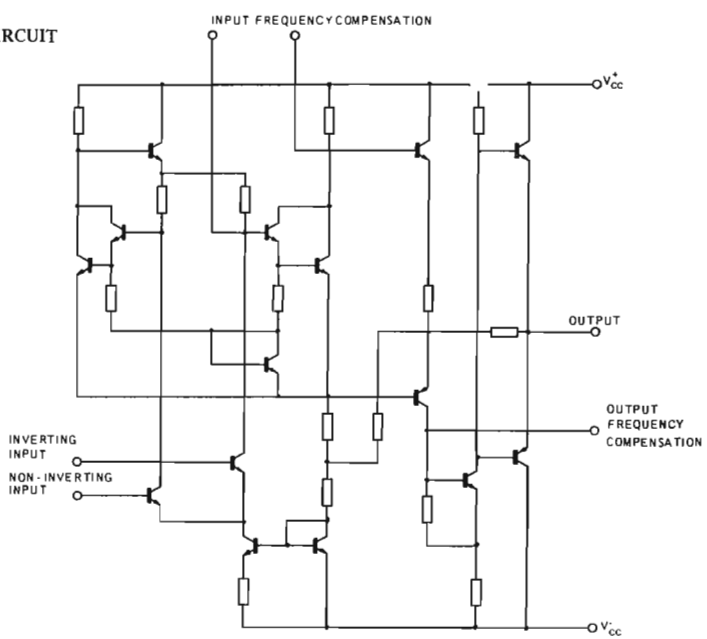


Note: all dimensions in mm.

ELECTRICAL CHARACTERISTICS (V_{CC}= ± 15V, T_A= 25°C unless otherwise specified)

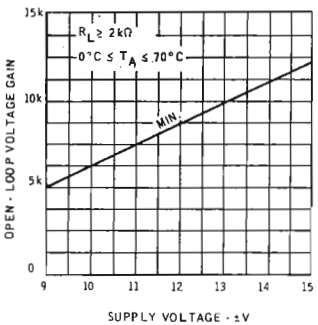
PARAMETER	CONDITIONS	Min.	Typ.	Max.	Unit
Input Offset Voltage	$R_S \leq 10\,k\Omega$, ± 9V ≤ $V_{CC} \leq$ ± 15V		± 2	± 7.5	mV
Input Offset Current			± 100	±500	nA
Input Bias Current			0.3	1.5	uA
Input Resistance		50	250		kΩ
Output Resistance			150		Ω
Large-Signal Voltage Gain	$R_L \geq 2\,k\Omega$, V_{OUT}= ±10V	15,000	45,000		
Output Voltage Swing	$R_L \geq 10\,k\Omega$	± 12	± 14		V
	$R_L \geq 2\,k\Omega$	± 10	± 13		V
Input Voltage Range		± 8	± 10		V
Common Mode Rejection Ratio	$R_S \leq 10\,k\Omega$	65	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\,k\Omega$		25	200	μV/V
Power Consumption	V_{OUT} = 0		80	200	mW
Transient Response (Unity Gain)	V_{IN}=20 mV, $R_L = 2\,k\Omega$, C_1 = 5000 pF				
Rise Time	R_1= 1.5 kΩ, C_2= 200 pF, R_2 = 50 Ω		0.3		μs
Overshoot	$C_L \leq 100$ pF		10		%
The following specifications apply for 0°C ≤ T_A ≤ + 70°C:					
Input Offset Voltage	$R_S \leq 10\,k\Omega$, ±9V ≤ $V_{CC} \leq$± 15V			± 10	mV
Input Offset Current				±750	nA
Input Bias Current				2	μA
Large-Signal Voltage Gain	$R_L \geq 2\,k\Omega$, V_{OUT}= ± 10V	12,000			
Input Resistance		35			kΩ

EQUIVALENT CIRCUIT

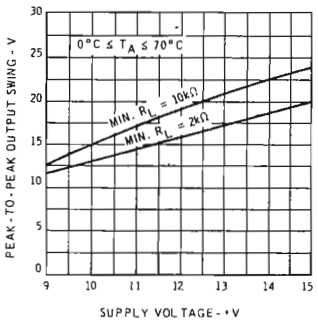


GUARANTEED ELECTRICAL CHARACTERISTICS

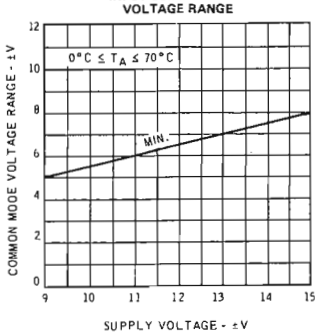
VOLTAGE GAIN



OUTPUT VOLTAGE SWING

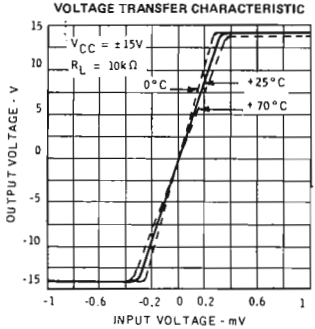


INPUT COMMON MODE VOLTAGE RANGE

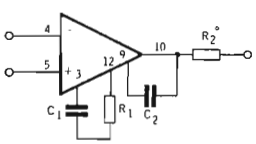


TYPICAL PERFORMANCE CURVES

VOLTAGE TRANSFER CHARACTERISTIC

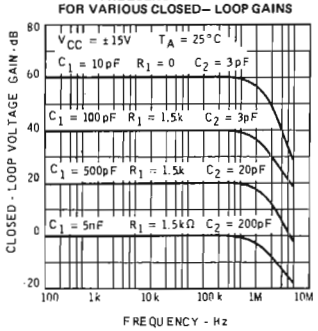


FREQUENCY COMPENSATION CIRCUIT



* Use R_2 = 50Ω when the amplifier is operated with capacitive loading

FREQUENCY RESPONSE FOR VARIOUS CLOSED– LOOP GAINS



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE - That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT - The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE - The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT - The average of the two input currents.

INPUT VOLTAGE RANGE - A range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO - The ratio of the input voltage range to the maximum change in input offset voltage over this range.

LARGE-SIGNAL VOLTAGE GAIN - The ratio of the maximum output voltage swing with load to change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING - The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE - The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

POWER CONSUMPTION - The DC power required to operate the amplifier with the output at zero and with no load current.

SUPPLY VOLTAGE REJECTION RATIO - The ratio of the change in input offset voltage to the change in supply voltage producing it.

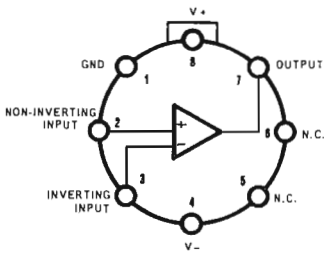
TRANSIENT RESPONSE - The closed-loop step function response of the amplifier under small-signal conditions.

high speed differential comparator

EXTENDED TEMPERATURE RANGE, –55°C ÷ 125°C

The μA 710 is a differential voltage comparator intended for applications requiring high accuracy and fast response times. It is constructed on a single silicon chip using the Planar epitaxial process. The device is useful as a variable threshold Schmitt trigger, a pulse height discriminator, a voltage comparator in high-speed A-D converters, a memory sense amplifier or a high-noise immunity line receiver. The output of the comparator is compatible with all integrated logic forms.

CONNECTION DIAGRAM
(Top View)



Note : Pin 4 connected to case.

ORDERING NUMBER

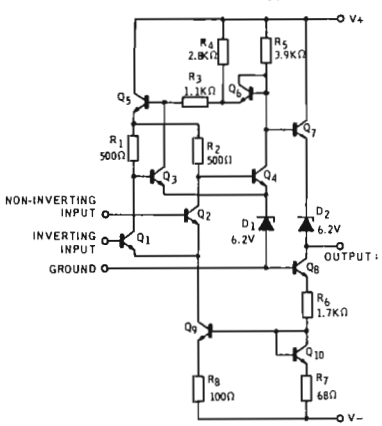
U5B771031X

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

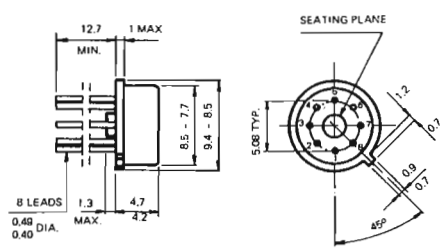
Positive Supply Voltage	14 V
Negative Supply Voltage	7 V
Peak Output Current	10 mA
Differential Input Voltage	± 5 V
Input Voltage	± 7 V
Internal Power Dissipation (Note 1)	300 mW
Operating Temperature Range	-55°C to 125°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 60 sec)	300°C

NOTES : on the following page.

SCHEMATIC DIAGRAM



PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-99 outline



Notes: All dimensions in mm.

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V^+ = 12V, V^- = -6V unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNIT.
Input Offset Voltage (Note 3)	$R_S \leq 200\,\Omega$		0.6	2	mV
Input Offset Current (Note 3)			0.75	3	μA
Input Bias Current			13	20	μA
Voltage Gain		1250	1700		
Output Resistance			200		Ω
Output Sink Current	$\Delta V_{in} \geq 5mV$, $V_{out} = 0$	2	2.5		mA
Response Time (Note 2)			40		ns
The following specifications apply for -55°C ≤ T_A ≤ +125°C:					
Input Offset Voltage (Note 3)	$R_S \leq 200\,\Omega$			3	mV
Average Temperature Coefficient of	$R_S = 50\,\Omega$				
Input Offset Voltage	T_A = 25°C to T_A = 125°C		3.5	10	μV/°C
	T_A = 25°C to T_A = -55°C		2.7	10	μV/°C
Input Offset Current (Note 3)	T_A = +125°C		0.25	3	μA
	T_A = -55°C		1.8	7	μA
Average Temperature Coefficient of	T_A = 25°C to T_A = +125°C		5	25	nA/°C
Input Offset Current	T_A = 25°C to T_A = -55°C		15	75	nA/°C
Input Bies Current	T_A = -55°C		27	45	μA
Input Voltage Range	V^- = -7V	±5			V
Common Mode Rejection Ratio	$R_S \leq 200\,\Omega$	80	100		dB
Differential Input Voltage Range		±5			V
Voltage Gain		1000			
Positive Output Level	$\Delta V_{in} \geq 5mV$, $0 \leq I_{out} \leq 5mA$	2.5	3.2	4	V
Negative Output Level	$\Delta V_{in} \geq 5mV$	-1	-0.5	0	V
Output Sink Current	$\Delta V_{in} \geq 5mV$, $V_{out} = 0$				
	T_A = +125°C	0.5	1.7		mA
	T_A = -55°C	1	2.3		mA
Positive Supply Current	$V_{out} \leq 0$		5.2	9	mA
Negative Supply Current			4.6	7	mA
Power Consumption			90	150	mW

NOTES:

(1) Rating applies for case temperatures to +125°C; derate linearly at 6.6 mW/°C for ambient temperatures above +105°C.

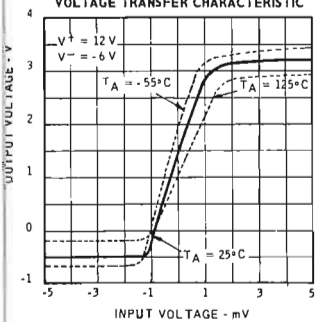
(2) The response time specified (see definitions) is for a 100 mV input step with 5mV overdrive.

(3) The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1.8V at -55°C, 1.4V at +25°C and 1V at +125°C.

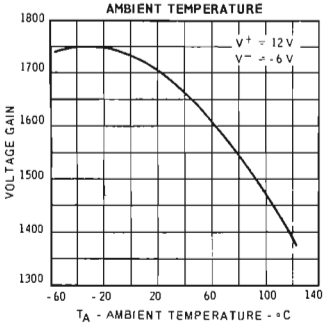
EXTENDED TEMPERATURE RANGE

TYPICAL ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

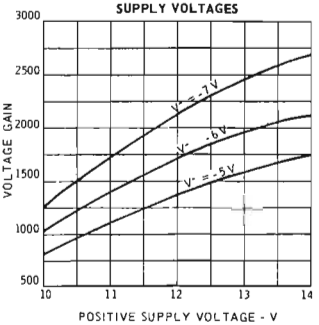
VOLTAGE TRANSFER CHARACTERISTIC



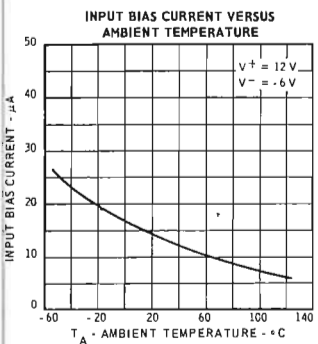
VOLTAGE GAIN VERSUS AMBIENT TEMPERATURE



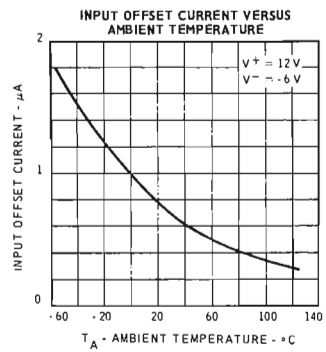
VOLTAGE GAIN VERSUS SUPPLY VOLTAGES



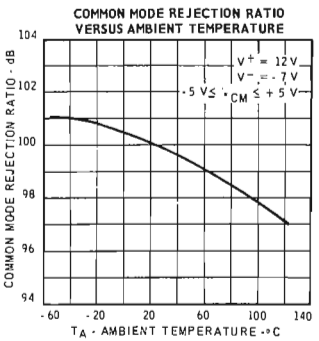
INPUT BIAS CURRENT VERSUS AMBIENT TEMPERATURE



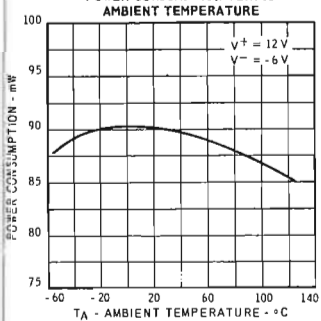
INPUT OFFSET CURRENT VERSUS AMBIENT TEMPERATURE



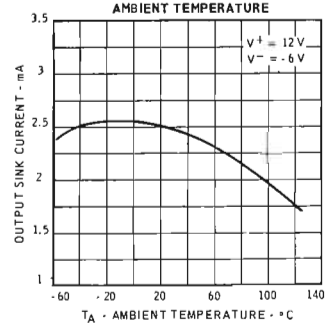
COMMON MODE REJECTION RATIO VERSUS AMBIENT TEMPERATURE



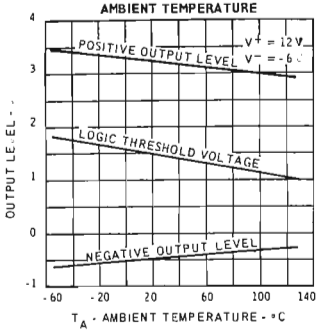
POWER CONSUMPTION VERSUS AMBIENT TEMPERATURE



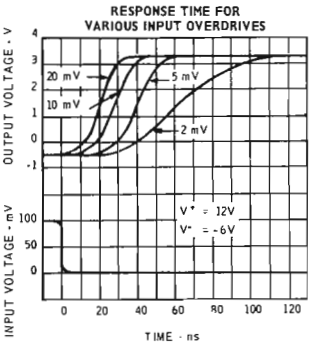
OUTPUT SINK CURRENT VERSUS AMBIENT TEMPERATURE

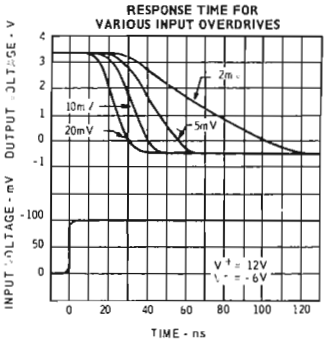


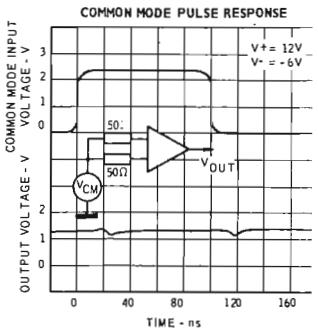
OUTPUT VOLTAGE LEVELS VERSUS AMBIENT TEMPERATURE



TYPICAL ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)







DEFINITION OF TERMS

LOGIC THRESHOLD VOLTAGE - The approximate voltage at the output of the comparator at which the loading logic circuitry changes its digi state. For the μA 710 this voltage has been fixed at +1.4V (see note 3).

INPUT OFFSET VOLTAGE - The voltage between the input terminals when the output is at the logic threshold voltage. The input offset volta may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT - The difference in the currents into the two input terminals with the output at the logic threshold voltage.

INPUT BIAS CURRENT - The average of the two input currents.

INPUT VOLTAGE RANGE - The range of voltage on the input terminals for which the comparator will operate within specifications.

INPUT COMMON MODE REJECTION RATIO - The ratio of the input voltage range to the maximum change in input offset voltage over this rang

DIFFERENTIAL INPUT VOLTAGE RANGE - The range of voltage between the input terminals for which operation within specifications is assure

VOLTAGE GAIN - The ratio of the change in output voltage to the change in voltage between the input terminals producing it with the DC outp level in the vicinity of the logic threshold voltage.

RESPONSE TIME - The interval between the application of an input step function and the time when the output crosses the logic threshold volta The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring t output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

POSITIVE OUTPUT LEVEL - The DC output voltage in the positive direction with the input voltage equal to or greater than a minimum specifi amount.

NEGATIVE OUTPUT LEVEL - The DC output voltage in the negative direction with the input voltage equal to or greater than a minimum specifi amount.

OUTPUT SINK CURRENT - The maximum negative current than can be delivered by the comparator.

PEAK OUTPUT CURRENT - The maximum current that may flow into the output load without causing damage to the comparator.

OUTPUT RESISTANCE - The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

POWER CONSUMPTION - The DC power into the amplifier with no output load. The DC power will vary with signal level, but is specified a maximum for the entire range of input - signal conditions.

High-speed differential comparator

STANDARD TEMPERATURE RANGE,
0°C to 70°C

- IMPROVED SPECIFICATIONS
- 5mV MAXIMUM OFFSET VOLTAGE
- 5 μA MAXIMUM OFFSET CURRENT
- 1000 MINIMUM VOLTAGE GAIN
- 20 μV/°C MAXIMUM OFFSET VOLTAGE DRIFT

The μA 710C is a differential voltage comparator intended for applications requiring high accuracy and fast response times. It is constructed on a single silicon chip using the planar epitaxial process. The device is useful as a variable threshold Schmidt trigger, a pulse height discriminator, a voltage comparator in high-speed A-D converters, a memory sense amplifier or a high-noise immunity line receiver. The output of the comparator is compatible with all integrated logic forms. For full temperature range operation (-55°C to +125°C) see μA 710 data sheet.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

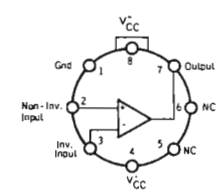
Positive Supply Voltage	14 V
Negative Supply Voltage	−7 V
Peak Output Current	10 mA
Differential Input Voltage	± 5 V
Input Voltage	± 7 V
Internal Power Dissipation (Note 1)	300 mW
Operating Temperature Range	0°C to + 70°C
Storage Temperature Range	-55°C to + 150°C
Lead Temperature	
(Soldering 60 sec for package No. 1)	300°C
(Soldering 10 sec for package No. 2)	260°C

ORDERING NUMBERS

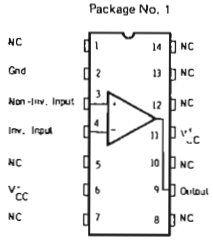
U5B771039X (for package No. 1)
U6E7710393 (for package No. 2)

Notes on the following page.

CONNECTION DIAGRAMS
(top view)

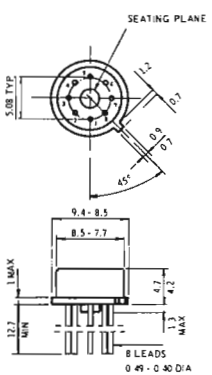


Package No. 1



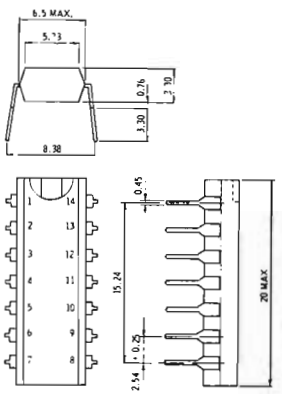
Package No. 2

PACKAGE No. 1
PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-99 outline



Note: all dimensions in mm.

PACKAGE No. 2
PHYSICAL DIMENSIONS
14-pin plastic DIP



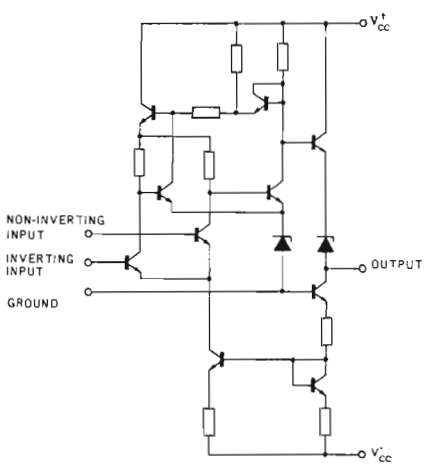
Note: all dimensions in mm.

STANDARD TEMPERATURE RANGE

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC}^+ = 12V, V_{CC}^- = -6V unless otherwise specified)

PARAMETER	CONDITIONS (Note 3)	Min.	Typ.	Max.	Unit
Input Offset Voltage (Note 3)	$R_S \leq 200\ \Omega$		± 1.6	± 5	mV
Input Offset Current (Note 3)			± 1.8	± 5	μA
Input Bias Current			16	25	μA
Voltage Gain		1000	1500		
Output Resistance			200		Ω
Output Sink Current	$\Delta V_{IN} \leq -5$ mV, $V_{OUT} = 0$	1.6	2.5		mA
Response Time (Note 2)			40		nsec
The following specifications apply for $0°C \leq T_A \leq +70°C$:					
Input Offset Voltage (Note 3)	$R_S \leq 200\ \Omega$			± 6.5	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\ \Omega$, $T_A = 0°C$ to $T_A = +70°C$		5	20	μV/°C
Input Offset Current (Note 3)				± 7.5	μA
Average Temperature Coefficient of Input Offset Current	$T_A = 25°C$ to $T_A = +70°C$		15	50	nA/°C
	$T_A = 25°C$ to $T_A = 0°C$		24	100	nA/°C
Input Bias Current	$T_A = 0°C$		25	40	μA
Input Voltage Range	$V_{CC} = -7V$	± 5			V
Common Mode Rejection Ratio	$R_S \leq 200\ \Omega$ $V_{CM} = \pm 5V$	70	98		dB
Differential Input Voltage Range		± 5			V
Voltage Gain		800			
Positive Output Level	$\Delta V_{IN} \geq 5$ mV, $0 \leq I_{OUT} \leq 5$ mA	2.5	3.2	4	V
Negative Output Level	$\Delta V_{IN} \geq 5$ mV	-1	-0.5	0	V
Output Sink Current	$\Delta V_{IN} \geq 5$ mV, $V_{OUT} = 0$	0.5			mA
Positive Supply Current	$V_{OUT} \leq 0$		5.2	9	mA
Negative Supply Current	$V_{OUT} \leq 0$		-4.6	- 7	mA
Power Consumption	$V_{OUT} \leq 0$		90	150	mW

EQUIVALENT CIRCUIT

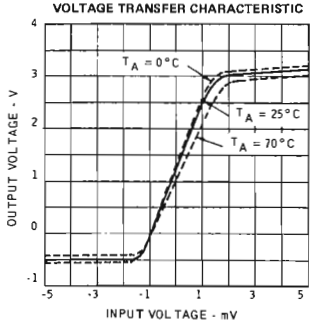


NOTES :

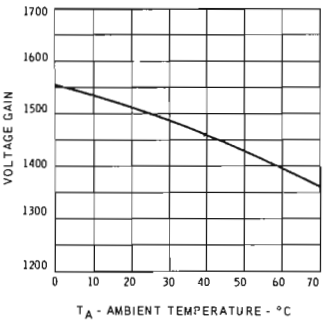
1) Ratings apply for ambient temperature to +70°C.
2) The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.
3) The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1.5V at 0°C, 1.4V at +25°C and 1.2V at +70°C.

TYPICAL ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC}^+ = 12 V, V_{CC}^- = -6 V unless otherwise specified)

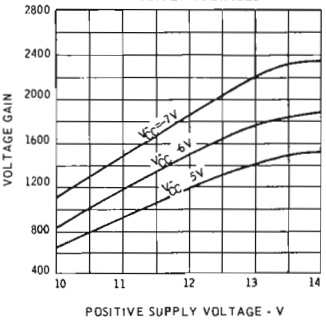
VOLTAGE TRANSFER CHARACTERISTIC



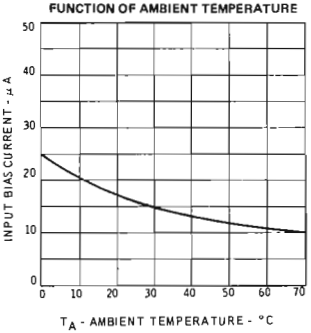
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



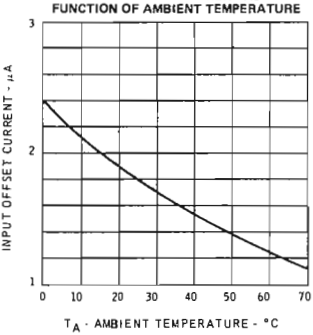
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



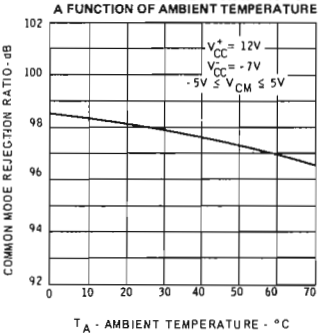
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



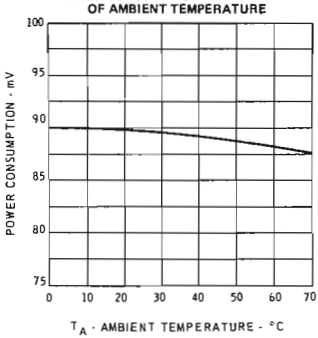
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



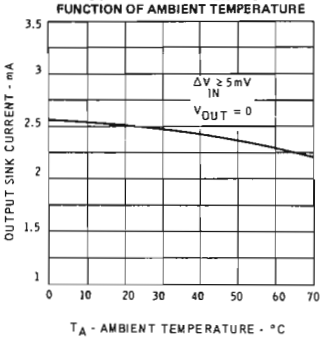
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



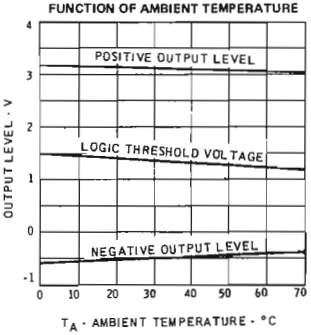
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



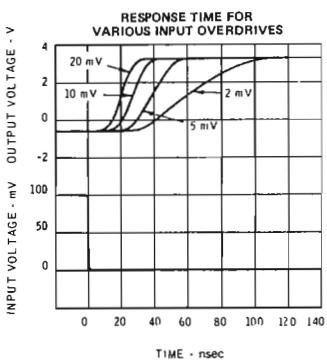
OUTPUT SINK CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

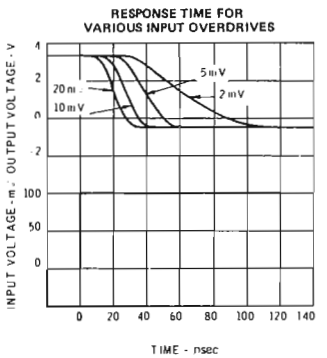


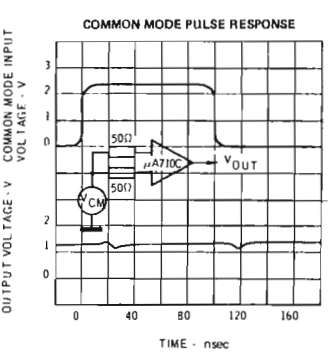
OUTPUT VOLTAGE LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



TYPICAL ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+_{CC} = 12V, V^-_{CC} = - 6V unless otherwise specified)







DEFINITION OF TERMS

LOGIC THRESHOLD VOLTAGE – The approximate voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

INPUT OFFSET VOLTAGE – The voltage between the input terminals when the output is at the logic threshold voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT – The difference in the currents into the two input terminals with the output at the logic threshold voltage.

INPUT BIAS CURRENT – The average of the two inputs currents.

INPUT VOLTAGE RANGE – The range of voltage on the input terminals for which the comparator will operate within specifications.

INPUT COMMON MODE REJECTION RATIO – The ratio of the input voltage range to the maximum change in input offset voltage over this range.

DIFFERENTIAL INPUT VOLTAGE RANGE – The range of voltage between the input terminals for which operation within specifications is assured.

VOLTAGE GAIN – The ratio of the change in output voltage to the change in voltage between the input terminals producing it with the DC output level in the vicinity of the logic threshold voltage.

RESPONSE TIME – The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

POSITIVE OUTPUT LEVEL – The DC output voltage in the positive direction with the input voltage equal to or greater than a minimum specified amount.

NEGATIVE OUTPUT LEVEL – The DC output voltage in the negative direction with the input voltage equal to or greater than a minimum specified amount.

OUTPUT SINK CURRENT – The maximum negative current that can be delivered by the comparator.

PEAK OUTPUT CURRENT – The maximum current that may flow into the output load without causing damage to the comparator.

OUTPUT RESISTANCE – The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

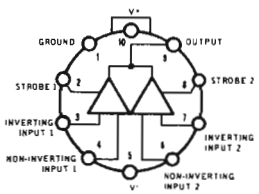
POWER CONSUMPTION – The DC power into the amplifier with no output load. The DC power will vary with signal level, but is specified as a maximum for the entire range of input-signal conditions.

dual comparator

EXTENDED TEMPERATURE RANGE, – 55°C ÷ + 125°C

The μA711 is a dual, differential voltage comparator intended primarily for core-memory sense amplifier applications. The device features high accuracy, fast response times, large input voltage range, low power consumption and compatibility with practically all integrated logic forms. When used as a sense amplifier, the threshold voltage can be adjusted over a wide range, almost independent of the integrated circuit characteristics. Independent strobing of each comparator channel is provided, and pulse stretching on the output is easily accomplished. Other applications of the dual comparator include a window discriminator in pulse height detectors and a double-ended limit detector for automatic go/no-go test equipment. The μA711, which is similar to the μA710 differential comparator, is constructed on a 40-mil square silicon chip using the Planar epitaxial process.

CONNECTION DIAGRAM
(Top view)



Note Pin 5 connected to case.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

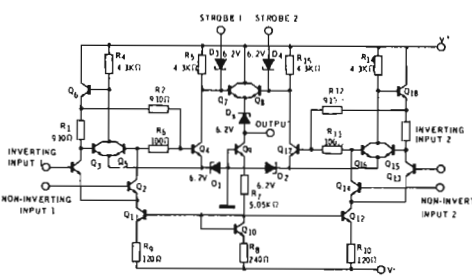
Positive Supply Voltage	14 V
Negative Supply Voltage	7 V
Peak Output Current	50 mA
Differential Input Voltage	± 5 V
Input Voltage	± 7 V
Strobe Voltage	0 to +6 V
Internal Power Dissipation (Note 1)	300 mW
Operating Temperature Range	-55°C to + 125°C
Storage Temperature Range	-65°C to + 150°C
Lead Temperature (Soldering, 60 sec)	+ 300°C

ORDERING NUMBER

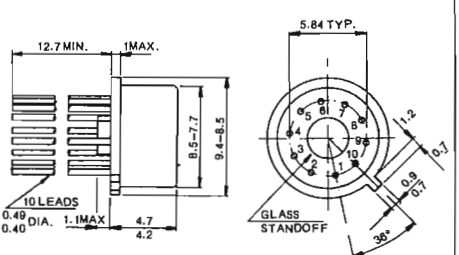
U5F771131X

NOTES : On the following page.

SCHEMATIC DIAGRAM



PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-100 outline



Note : all dimensions in mm.

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V^+ = 12$ V, $V^- = -6$ V unless otherwise noted)

PARAMETER (see definitions)	CONDITIONS	Min.	Typ.	Max.	UNIT
Input Offset Voltage	$V_{OUT} = +1.4$V, $R_S \leq 200\ \Omega$, $V_{CM} = 0$		1	3.5	mV
	$V_{OUT} = +1.4$ V, $R_S \leq 200\ \Omega$		1	5	mV
Input Offset Current	$V_{OUT} = +1.4$ V		0.5	10	μA
Input Bias Current			25	75	μA
Voltage Gain		750	1500		
Response Time (Note 2)			40		nsec
Strobe Release Time			12		nsec
Input Voltage Range	$V^- = -7$ V	±5			V
Differential Input Voltage Range		±5			V
Output Resistance			200		Ω
Positive Output Level	$V_{IN} \geq 10$ mV		4.5	5	V
Loaded Positive Output Level	$V_{IN} \geq 10$ mV, $I_O = 5$ mA	2.5	3.5		V
Negative Output Level	$V_{IN} \geq 10$ mV	-1	-0.5	0	V
Strobed Output Level	$V_{strobe} \leq 0.3$ V	-1		0	V
Output Sink Current	$V_{IN} \geq 10$ mV, $V_{OUT} \geq 0$	0.5	0.8		mA
Strobe Current	$V_{strobe} = 0$		1.2	2.5	mA
Positive Supply Current	$V_{OUT} \leq 0$		8.6		mA
Negative Supply Current			3.9		mA
Power Consumption			130	200	mW
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage (Note 3)	$R_S \leq 200\ \Omega$, $V_{CM} = 0$			4.5	mV
	$R_S \leq 200\ \Omega$			6	mV
Input Offset Current (Note 3)				20	μA
Input Bias Current				150	μA
Temperature Coefficient of Input Offset Voltage			5		μV/°C
Voltage Gain		500			

NOTES :

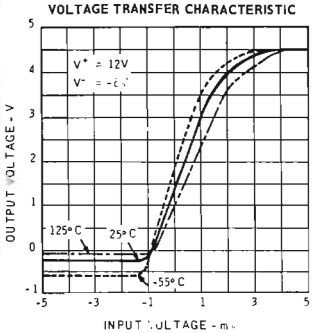
(1) Rating applies for case temperatures to +125°C; derate linearly at 6.6 mW/°C for ambient temperature above 105°C.

(2) The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

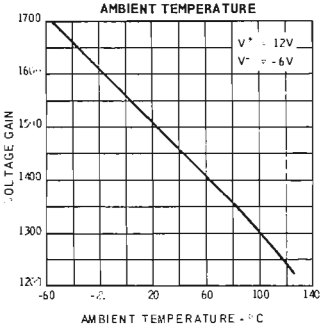
(3) The input offset voltage (see definitions) is specified for a logic threshold voltage of 1.8 V at -55°C, 1.4 V at +25°C and 1 V at +125°C.

TYPICAL ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

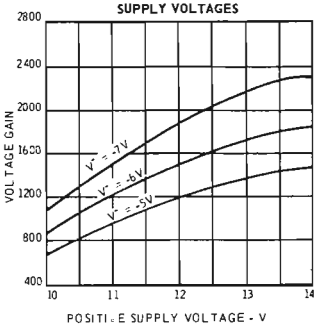
VOLTAGE TRANSFER CHARACTERISTIC



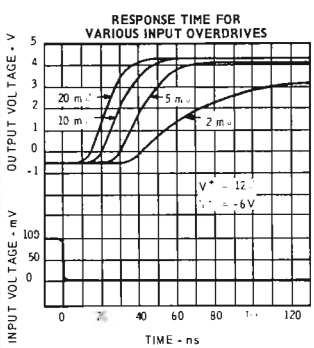
VOLTAGE GAIN VERSUS AMBIENT TEMPERATURE



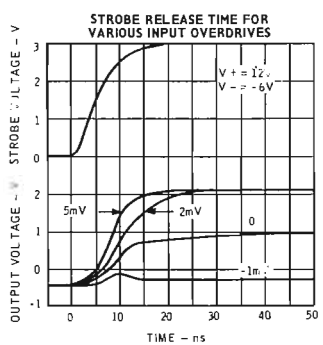
VOLTAGE GAIN VERSUS SUPPLY VOLTAGES



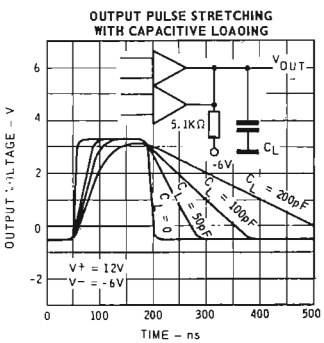
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



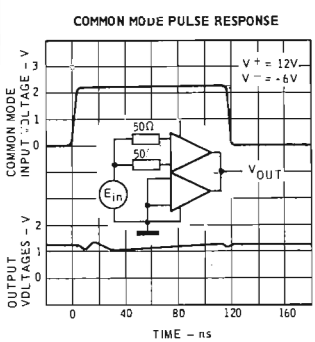
STROBE RELEASE TIME FOR VARIOUS INPUT OVERDRIVES



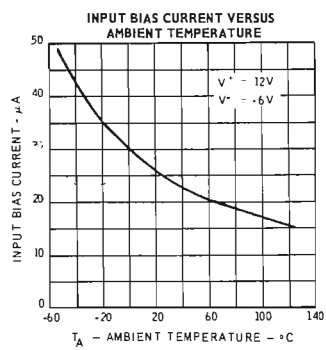
OUTPUT PULSE STRETCHING WITH CAPACITIVE LOADING



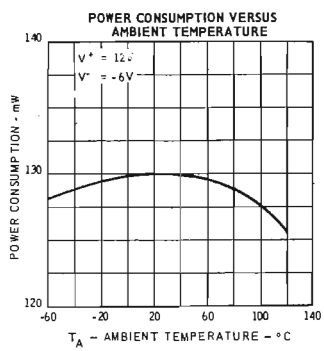
COMMON MODE PULSE RESPONSE



INPUT BIAS CURRENT VERSUS AMBIENT TEMPERATURE



POWER CONSUMPTION VERSUS AMBIENT TEMPERATURE



DEFINITION OF TERMS

LOGIC THRESHOLD VOLTAGE - The approximate voltage at the output of the comparator at which the loading logic circuitry changes its digital state. For the μA711 this voltage has been fixed at +1.4 V (see note 3).

INPUT OFFSET VOLTAGE* - The voltage between the input terminals when the output is at the logic threshold voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT* - The difference in the currents into the two input terminals with the output at the logic threshold voltage.

INPUT BIAS CURRENT* - The average of the two input currents.

INPUT VOLTAGE RANGE* - The range of voltage on the input terminals for which the comparator will operate within specifications.

DIFFERENTIAL INPUT VOLTAGE RANGE* - The range of voltage between the input terminals for which operation within specifications is assured

VOLTAGE GAIN* - The ratio of the change in output voltage to the change in voltage between the input terminals producing it with the DC output level in the vicinity of the logic threshold voltage.

RESPONSE TIME* - The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

STROBE RELEASE TIME* - The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from the zero to the one logic level. Appropriate input conditions are assumed.

POSITIVE OUTPUT LEVEL* - The DC output voltage in the positive direction with the input voltage equal to or greater than a minimum specified amount.

NEGATIVE OUTPUT LEVEL* - The DC output voltage in the negative direction with the input voltage equal to or greater than a minimum specified amount.

OUTPUT SINK CURRENT - The maximum negative current that can be delivered by the comparator.

PEAK OUTPUT CURRENT - The maximum current that may flow into the output load without causing damage to the comparator.

OUTPUT RESISTANCE* - The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

STROBED OUTPUT LEVEL* - The DC output voltage, independent of input voltage, with the voltage on the strobe terminal equal to or less than a minimum specified amount.

STROBE CURRENT - The maximum current drawn by the strobe terminal when it is at zero logic level.

POWER CONSUMPTION - The DC power into the amplifier with no output load. The DC power will vary with signal level, but is specified as a maximum for the entire range of input-signal conditions.

*These definitions apply for either side with the other disabled with the strobe.

Dual comparator

STANDARD TEMPERATURE RANGE,
0°C to 70°C

- FAST RESPONSE TIMES
- LOW POWER CONSUMPTION
- COMPATIBLE WITH LOGIC FAMILIES

The μA711C is a dual, differential voltage comparator intended primarily for core-memory sense amplifier applications. The device features high accuracy, fast response times, wide input voltage range, low power consumption and compatibility with pratically all integrated logic forms. When used as a sense amplifier, the threshold voltage can be adjusted over a wide range, almost independent of the integrated circuit characteristics. Independent strobing of each comparator channel is provided, and pulse stretching on the output is easily accomplished. Other applications of the dual comparator include as window discriminator in pulse height detectors and as double-ended limit detector for automatic go/no-go test equipment. The μA711C, which is similar to the μA710C differential comparator, is constructed on a silicon chip by means of the planar epitaxial process. For full temperature range operation (-55°C to + 125°C) see μA711 data sheet.

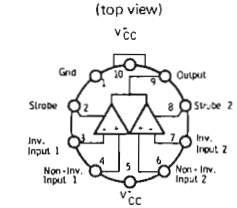
ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage	14 V
Negative Supply Voltage	-7 V
Peak Output Current	50 mA
Differential Input Voltage	± 5 V
Input Voltage	± 7 V
Strobe Voltage	0V to 6 V
Internal Power Dissipation (Note 1, over)	300 mW
Operating Temperature Range	0°C to + 70°C
Storage Temperature Range	-55°C to + 150°C
Lead Temperature	
(Soldering 60 sec. for package No. 1)	300°C
(Soldering 10 sec. for package No. 2)	260°C

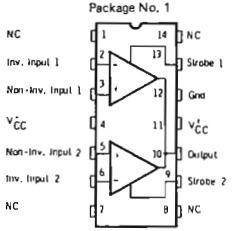
ORDERING NUMBERS

U5F771139X (for package No. 1)
U6E7711393 (for package No. 2)

CONNECTION DIAGRAMS
(top view)

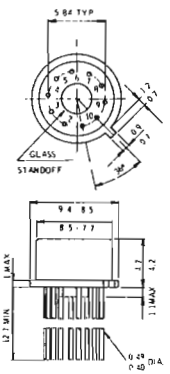


Package No. 1



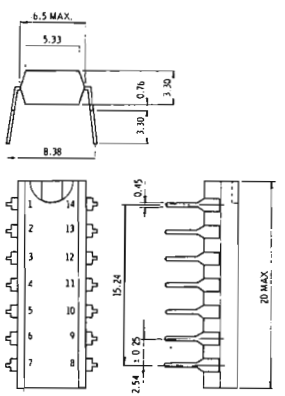
Package No. 2

PACKAGE No. 1
PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-100 outline



Note: all dimensions in mm.

PACKAGE No. 2
PHYSICAL DIMENSIONS
14-pin plastic DIP

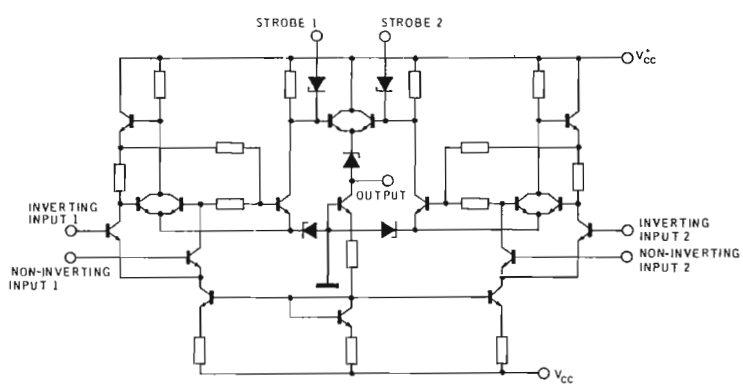


Note: all dimensions in mm.

ELECTRICAL CHARACTERISTICS (T_A= 25°C, V_{CC}^+= 12V, V_{CC}^-=-6V unless otherwise noted)

PARAMETER	CONDITIONS	Min.	Typ.	Max.	Unit
Input Offset Voltage	V_{OUT}= + 1.4V, $R_S \leq 200\ \Omega$		± 1	± 5	mV
	V_{OUT}= + 1.4V, $R_S \leq 200\ \Omega$, V_{CM}= ± 5V, V_{CC}^-= - 7V		± 1	± 7.5	mV
Input Offset Current	V_{OUT}= + 1.4V		± 0.5	± 15	μA
Input Bias Current	V_{CM}= + 5V		25	100	uA
Voltage Gain		700	1500		
Response Time (Note 2)			40		nsec
Strobe Release Time			12		nsec
Input Voltage Range	V_{CC}^-= -7V	± 5			V
Differential Input Voltage Range		± 5			V
Output Resistance			200		Ω
Positive Output Level	$V_{IN} \geq$ 10 mV		4.5	5	V
Loaded Positive Output Level	$V_{IN} \geq$ 10 mV, I_O = 5 mA	2.5	3.5		V
Negative Output Level	$V_{IN} \geq$ 10 mV	-1	-0.5	0	V
Strobed Output Level	$V_{strobe} \leq$ 0.3V	-1		0	V
Output Sink Current	$V_{IN} \geq$ 10 mV, $V_{OUT} \geq$ 0	0.5	0.8		mA
Strobe Current	V_{strobe} = 100mV		-1.2	-2.5	mA
Positive Supply Current	$V_{OUT} \leq$ 0		8.6		mA
Negative Supply Current	$V_{OUT} \leq$ 0		-3.9		mA
Power Consumption	$V_{OUT} \leq$ 0		130	230	mW
The following specifications apply for 0°C≤T_A≤ + 70°C:					
Input Offset Voltage (Note 3)	$R_S \leq 200\ \Omega$			± 6	mV
	$R_S \leq 200\ \Omega$, V_{CM}= ± 5V, V_{CC}^-= -7V			± 10	mV
Input Offset Current (Note 3)				± 25	μA
Input Bias Current	V_{CM}= + 5V			150	μA
Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 200\ \Omega$		5		μV/°C
Voltage Gain		500			

EQUIVALENT CIRCUIT

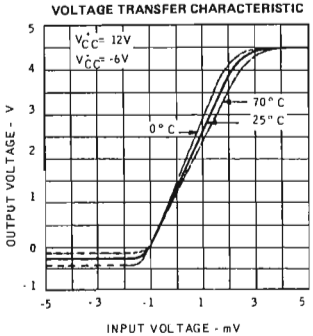


NOTES :

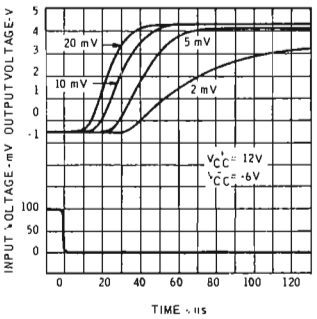
1) Rating applies for ambient temperature to + 70°C.
2) The response time specified is for a 100mV input step with 5mV overdrive.
3) The input offset voltage is specified for a logic threshold voltage of 1.5V at 0°C, 1.4V at + 25°C and 1.2V at + 70°C.

TYPICAL ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

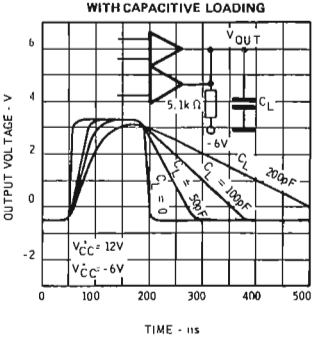
VOLTAGE TRANSFER CHARACTERISTIC



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



OUTPUT PULSE STRETCHING WITH CAPACITIVE LOADING



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STROBE CURRENT - The maximum current drawn by the strobe terminal when it is at zero logic level.

POWER CONSUMPTION - The DC power into the amplifier with no output load. The DC power will vary with signal level, but is specified as a maximum for the entire range of input-signal conditions.

* These definitions apply for either side with the other disabled with the strobe.

MOS INTEGRATED CIRCUITS

MOS INTEGRATED CIRCUITS

E. = Extended temperature range
S. = Standard temperature range

Multifunction gate

STANDARD TEMPERATURE RANGE 0° C TO 70° C

- INPUT GATE PROTECTION
- OUTPUT DRIVE VERSATILITY
- LOW POWER CONSUMPTION
- TWO DIFFERENT SUPPLY VOLTAGES ($-V_{DD}$; $-V_{GG}$)

The M001 is a monolithic integrated circuit utilizing channel enhancement mode MOS technology. The device can be used to gain familiarity with MOS integrated circuit logic versatility as a building block in a MOS system, or as a breadboarding gate in the design of complex custom integrated circuits.

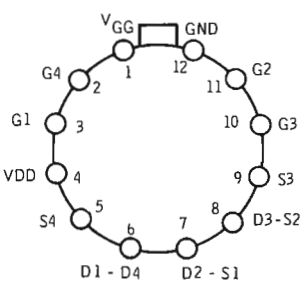
ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Voltage on any Pin ($V_{body} = 0$)	-30V to +0.3V
Storage Temperature	-55°C to +150°C
Operating Temperature	0°C to +70°C

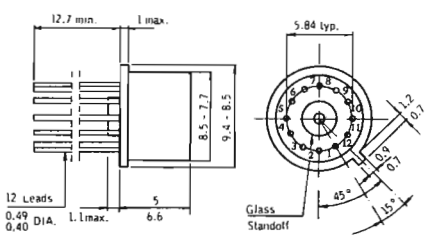
ORDERING NUMBER

M001 T1

CONNECTION DIAGRAM
(Top view)



PHYSICAL DIMENSIONS
In accordance with
JEDEC TO-73 outline



Notes : All dimensions in mm.
Lead No. 6 internally connected to case.

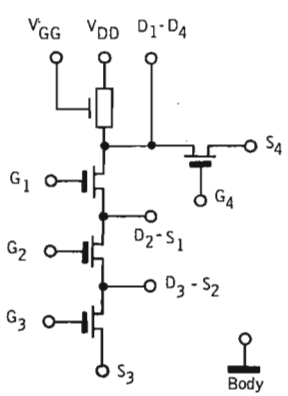
ELECTRICAL CHARACTERISTICS ($V_{body} = 0$; $T_A = 25°C$)

PARAMETER	CONDITIONS		Min.	Typ.	Max.	UNIT
Load Resistance	$V_{DD} = V_{GG} = -27 \pm 1V$	V_{D1-D4} = GND	23	32		K Ω
	$V_{DD} = -13V \pm 1V$	$V_{GG} = -27V \pm 1V$				
	V_{D1-D4} = GND		13	18		K Ω
On Resistance	$V_{in} = -19V$	$I_{Ron} = -100\ \mu A$		350	1000	Ω
	$V_{in} = -9V$	$I_{Ron} = -100\ \mu A$		500	1200	Ω
Input Leakage Current	$V_{in} = -20V$				1	μA
Threshold Voltage (VTH)	$V_{DD} = V_{GG}$ = GND	$I_D = -10\ \mu A$	3.3		5.7	V
Input High Voltage			-9			V
Input Low Voltage					-3	V
Power Consumption	$V_{DD} = -28V$			20		mW

TYPICAL RESISTANCE CHARACTERISTICS

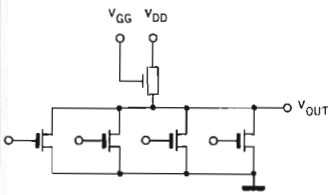
PARAMETER	CONDITIONS			VALUE
R_{Load}	$V_{DD} = -13V$	$V_{GG} = -27V$	$V_{D1} = 0V$	18 KΩ
	$V_{DD} = -27V$	$V_{GG} = -27V$	$V_{D1} = 0V$	32 KΩ
R_{on}	$V_{GS} = -19V$	$V_{DS} \leq -1V$	$V_{D2} = 0V$	350 Ω
	$V_{GS} = 9V$	$V_{DS} \leq -1V$	$V_{D2} = 0V$	500 Ω

SCHEMATIC DIAGRAM



BASIC APPLICATIONS :

NOR GATE CONFIGURATION



Pin 8 = Pin 6 = V_{out}
Pin 9 = Pin 7 = Pin 5 = GND
V_{DD} = V_{GG} = -27V

Logic Level	Voltage Level Min.	Max.
VOH (1)	-14V	
VOL (0)		-1.2V

Pin 8 = Pin 6 = V_{out}
Pin 9 = Pin 7 = Pin 5 = GND
V_{DD} = -13V V_{GG} = -27V

Logic Level	Voltage Level Min.	Max.
VOH (1)	-10V	
VOL (0)		- 1V

NAND GATE CONFIGURATION

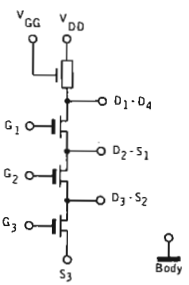
3-Input Gate

Pin 9 = GND
Pin 6 = Output
V_{GG} = V_{DD} = -27V

Logic Level	Voltage Level Min.	Max.
VOH (1)	-14V	
VOL (0)		-2.7V

Pin 9 = GND
Pin 6 = Output
V_{DD} = -13V
V_{GG} = -27V

Logic Level	Voltage Level Min.	Max.
VOH (1)	-10V	
VOL (0)		-2.5V



2-Input Gate

Pin 8 = GND
Pin 6 = Output
V_{GG} = V_{DD} = -27V

Logic Level	Voltage Level Min.	Max.
VOH (1)	-14V	
VOL (0)		-2V

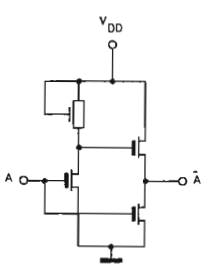
Pin 8 = GND
Pin 6 = Output
V_{DD} = -13V
V_{GG} = -27V

Logic Level	Voltage Level Min.	Max.
VOH (1)	-10V	
VOL (0)		-1.8V

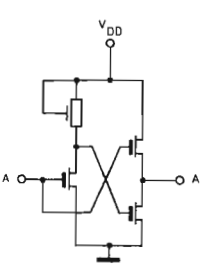
OTHER APPLICATIONS

MOS logic provides the versatility to build many different functions. The following circuits show how to build functions using one or two M001 packages. (V_{DD} = – 27V)

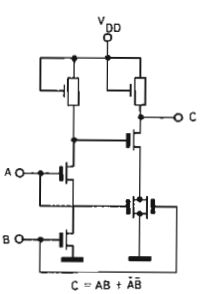
INVERTING BUFFER



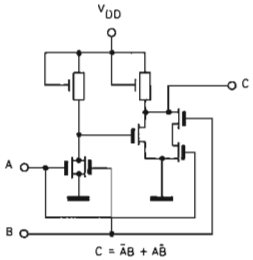
NON-INVERTING BUFFER



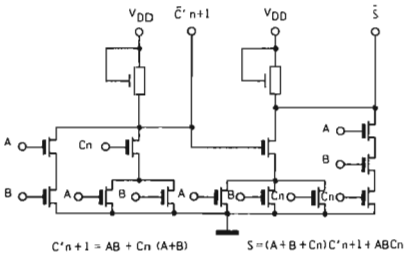
EXCLUSIVE NOR



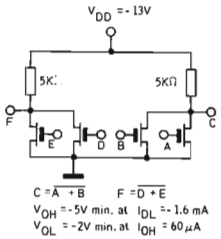
EXCLUSIVE OR



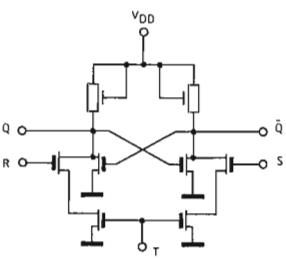
FULL ADDER



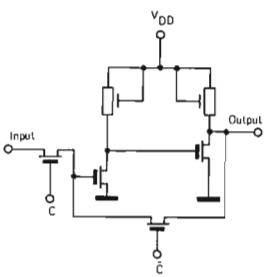
TTL INTERFACE



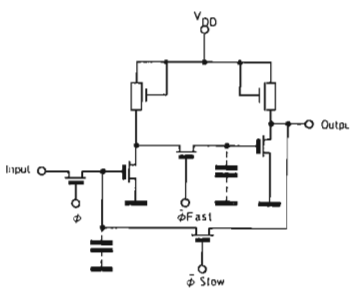
RST FLIP-FLOP



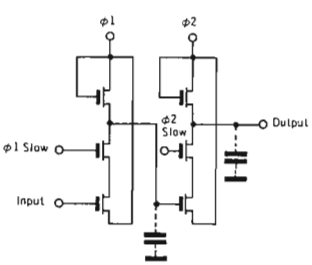
TYPE D FLIP-FLOP



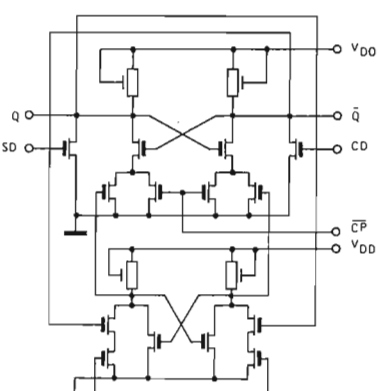
STATIC (DC) SHIFT REGISTER BIT



DYNAMIC 4-PHASE (4 Φ) SHIFT REGISTER BIT



FREQUENCY DIVIDER (Input = CP)



4-phase clock driver

STANDARD TEMPERATURE RANGE
0°C to 70°C

- HIGH OUTPUT VOLTAGE SWING
- ONLY ONE INPUT SIGNAL REQUIRED
- FOUR PHASES IN ONE TO-100 PACKAGE
- THREE DIFFERENT PHASE MODES
- BIPOLAR COMPATIBLE SYNCHRONIZING PULSE

The M002 is a P-channel enhancement mode monolithic MOS integrated circuit. The device generates four clock signals and is capable of directly driving dynamic, high threshold, MOS circuits or systems. It requires an external reference frequency and produces output clock signals at a rate equal to one-fourth the input clock frequency. The output states change after the positive transition of the input clock. The output clock signals are available in three different timing modes which satisfy the majority of all four-phase systems requirements. These modes are selectable by two external control lines (M, N) which can be grounded ("0") or left floating ("1"). Low output source impedance in the "0" and the "1" states is obtained by high efficiency push-pull drivers. The bipolar compatible sync. pulse is available via an open drain MOS transistor.

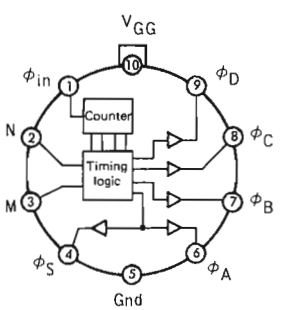
ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Input voltage (1)	-30V to +0.3V
Supply Voltage (1)	-30V to+ 0.3V
Storage Temperature	-55°C to +150°C
Power Dissipation (2)	500 mW at T_A = 70°C

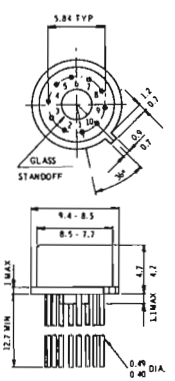
Note 1 : This voltage is with respect to the Gnd pin voltage
Note 2 : See following page

ORDERING NUMBER
M 002 T1

CONNECTION DIAGRAM
(Top view)



PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-100



Note : all dimensions in mm.

ELECTRICAL CHARACTERISTICS : (T_A = 0°C to 70°C, V_{GG} = -27V ± 1V unless otherwise noted)

SYMBOL	CHARACTERISTIC	Min.	Max.	Unit	TEST CONDITIONS
	INPUT CLOCK (ϕ_{in})				
f_{in}	Repetition Rate Range	4	2000	kHz	
V_{ILcp}	"0" Level Voltage		-2	V	
V_{IHcp}	"1" Level Voltage	-9		V	
V_{Ipw}	Pulse Width	200		nsec	
	PHASE OUTPUTS (ϕ_A-ϕ_B-ϕ_C-ϕ_D)				
f_{out}	Repetition Rate Range	1	500	kHz	
V_{OL}	"0" Level Voltage		-0.5	V	I_{OL} = 2 mA
V_{OH}	"1" Level Voltage	-25.5		V	I_{OH} = 2 mA
t_r	Rise Time		100	nsec	C_L = 200 pF, T_A = 25°C
t_f	Fall Time		200	nsec	see fig. 1
V_{OV}	Overlap Voltage		-5	V	see fig. 2
	SYNC. OUTPUT (ϕ_S)				
R_{on}	"On" resistance		900	Ω	V_{out} = 0 to -3V
I_L	Leakage Current (off)		1	μA	V_{out} = -5V

Note 2 : Power limits are:
500 mW at T_A = 70°C } without heat-sink
700 mW at T_A = 25°C }
800 mW at T_A = 70°C with a 50°C/W heat-sink

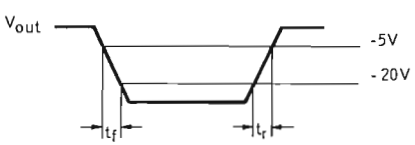


Fig. 1

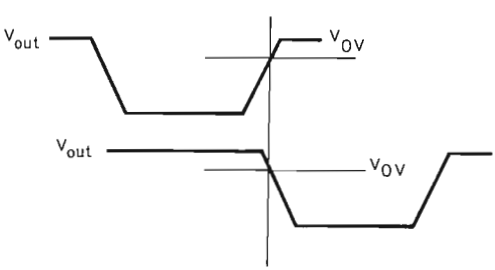
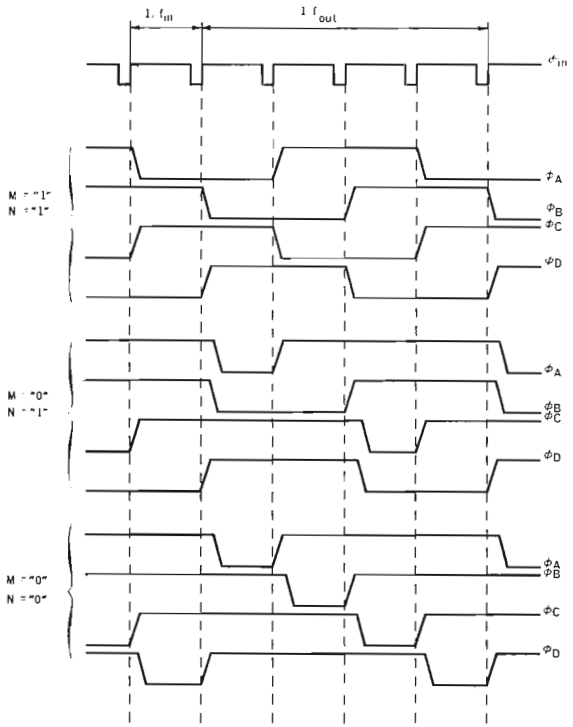
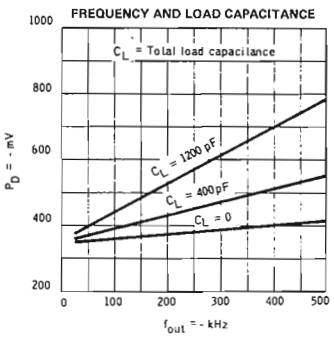


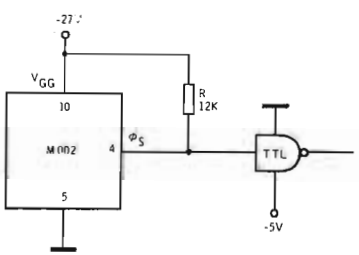
Fig. 2

TYPICAL TIMING DIAGRAM



POWER DISSIPATION VS OUTPUT FREQUENCY AND LOAD CAPACITANCE





Sync. out driving TTL

Quad up/down decade counter

The M003 is a quad up/down decade counter arranged as two subsystems of two decades each. Each subsystem has a single up/down control, zero and nine reset, and clock line. Common count enable input is provided for all decades, while synchronous carry-in inputs are available for each single counter. Constructed on a single monolithic chip using silicon nitride P-channel technology, the M003 has its reliability level enhanced by the use of the exclusive Planox process.

EXTENDED TEMPERATURE RANGE
-55°C to 125°C
STANDARD TEMPERATURE RANGE
0°C to 70°C

- FULLY TTL COMPATIBLE
- DC TO 1MHz OPERATION
- SINGLE PHASE CLOCK
- INPUT GATE PROTECTION

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Input Voltage (1)	-20V to 0.3V
Clock Voltage (1)	-20V to 0.3V
Supply Voltage (1)	-20V to 0.3V
Storage Temperature Range	-55°C to 150°C

ORDERING NUMBER

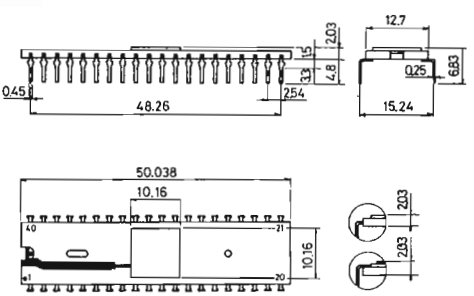
M003 T1 (for standard temperature range)
M003 T2 (for extended temperature range)

Note 1: This voltage is with respect to the V_{SS} pin voltage.

PIN CONNECTION

1	V_{SS}		21	VGG	
2	Carry OUT 3		22	Carry OUT 2	
3	CP (3-4)		23	Carry IN 2c	
4	Carry IN 3b		24	Carry IN 2b	
5	Carry IN 3a		25	Carry IN 2a	
6	Reset 0 (3-4)		26	Reset to 9 (1-2)	
7	A3 LSD	Third decade outputs	27	A2 LSD	Second decade outputs
8	B3		28	B2	
9	C3		29	C2	
10	D3 MSD		30	D2 MSD	
11	Up/Down (3-4)		31	Up/Down (1-2)	
12	D4 MSD	Fourth decade outputs	32	D1 MSD	First decade outputs
13	C4		33	C1	
14	B4		34	B1	
15	A4 LSD		35	A1 LSD	
16	VGI		36	Reset to 0 (1-2)	
17	Reset to 9 (3-4)		37	Carry IN 1a	
18	Carry IN 4		38	Carry IN 1b	
19	CP Enable		39	CP (1-2)	
20	Carry OUT 4		40	Carry OUT 1	

PHYSICAL DIMENSIONS
40 lead ceramic DIP

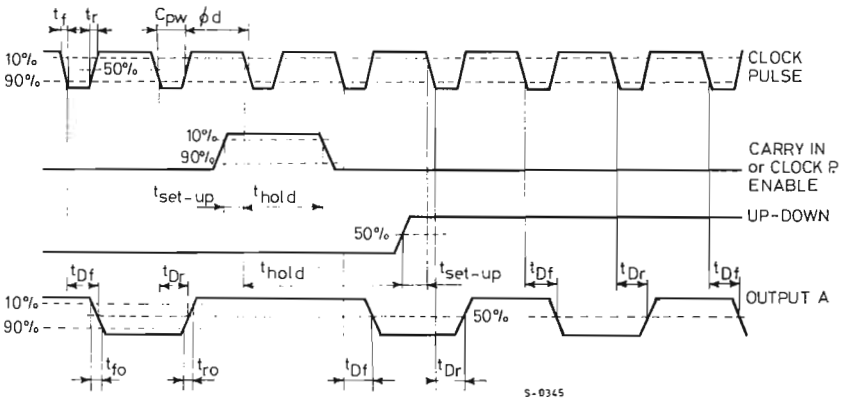


The package can be available in P044 SGS-ATES package.

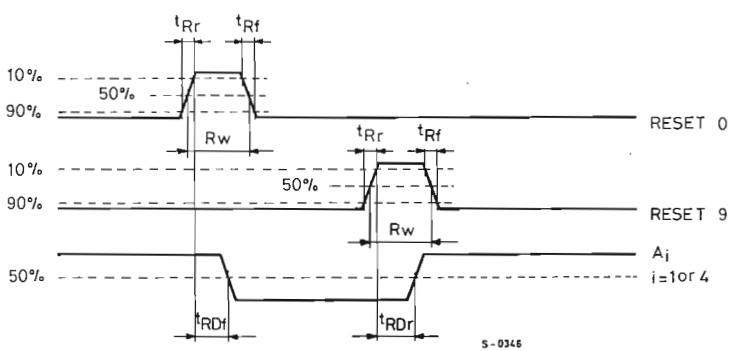
ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C; V_{GG} = -12V ± 1V; V_{GI} = -5V ± 0.25V; V_{SS} = +5V ± 0.25V, unless otherwise noted)

SYMBOL	CHARACTERISTICS	Min.	Typ.	Max.	Unit	TEST CONDITIONS	
	CLOCK PULSES						
f	Repetition Rate Range	0		1	MHz		
C_{pw}	Pulse Width	500			ns		
ϕd	Pulse Separation	500			ns		
tr, tf	Rise and Fall Time			1000	ns	T_A = 25°C	see waveforms
V_{ILcp}	"0" Level Voltage			V_{SS} -4.2	V		
V_{IHcp}	"1" Level Voltage	V_{SS} -1.5			V		
I_{Lcp}	Leakage Current			1	µA	V_{cp}=V_{SS} -15V	T_A=25°C
C_{cp}	Input Capacitance			10	pF	V_{cp}=V_{SS}	f = 1 MHz
	CONTROL INPUTS						
V_{IL}	"0" Level Voltage			V_{SS}-4.2	V		
V_{IH}	"1" Level Voltage	V_{SS} -1.5			V		
t_{set-up}	Set-up Time	200			ns		
t_{hold}	Hold Time	200			ns		
I_L	Leakage Current			1	µA	V_{cp}=V_{SS} -15V	T_A= 25°C
C_{in}	Input Capacitance			10	pF	V_{cp}=V_{SS}	f = 1 MHz
	RESET 0 and 9						
V_{IL}	"0" Level Voltage			V_{SS} -4.2	V		
V_{IH}	"1" Level Voltage	V_{SS} - 1.5			V		
R_W	Reset Pulse Width	300			ns		
t_{Rf}, t_{Rr}	Reset Rise and Fall Time			1000	ns		
	DATA OUTPUTS						
V_{OL}	"0" Level Voltage			0.4	V	load = 10pF	I_{sink} = 1.6mA
V_{OH}	"1" Level Voltage	V_{SS} - 1			V	I_{OL} = 100µA	
t_{ro}	Rise Time		120		ns	see waveforms	
t_{fo}	Fall Time		200		ns	see waveforms	
	SWITCHING TIMES						
t_{Df}	Delay Time to Fall		300		ns	see waveforms	
t_{Dr}	Delay Time to Rise		250		ns	see waveforms	
t_{RDf}	Reset Delay Time to Fall		280		ns	see waveforms	
t_{RDr}	Reset Delay Time to Rise		280		ns	see waveforms	
	POWER CONSUMPTION						
I_{GG}	Gate Supply Current		6		mA		
I_{GI}	Buffer Supply Current		10		mA	T_A = 25°C	f = 1 MHz

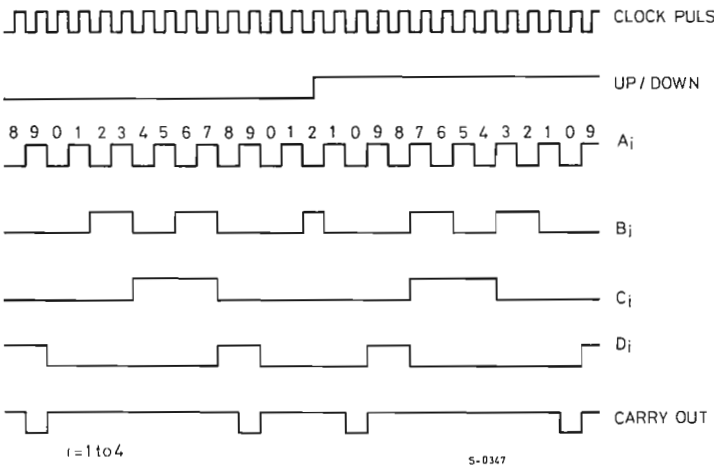
WAVEFORMS (SYNCHRONOUS INPUTS)



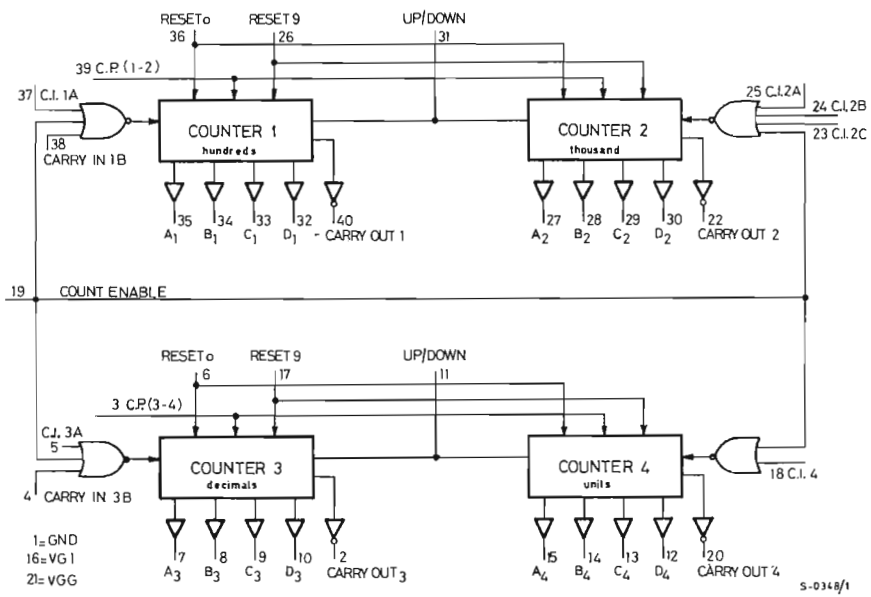
WAVEFORMS (ASYNCHRONOUS INPUTS)



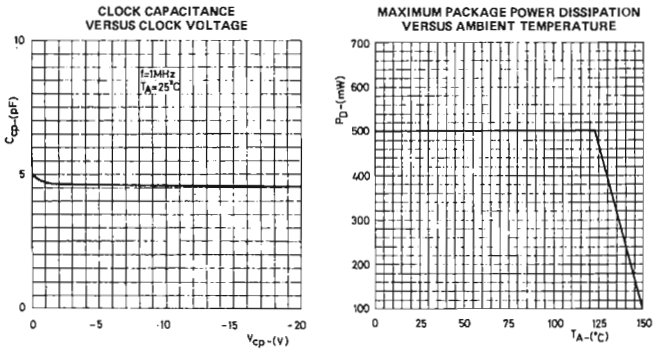
TYPICAL TIMING DIAGRAMS



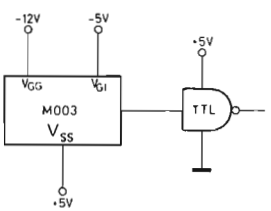
BLOCK DIAGRAM (FIG. 1)



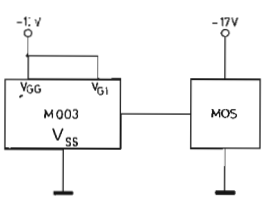
TYPICAL ELECTRICAL CHARACTERISTICS (contd.)



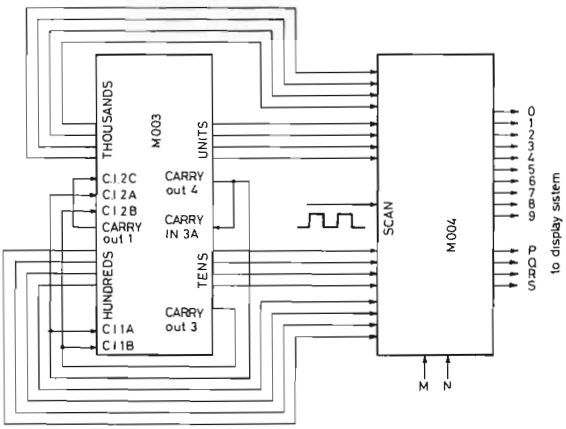
POWER CONNECTION FOR M003 DRIVING TTL (FIG. 2)



POWER CONNECTION FOR M003 DRIVING MOS (FIG. 3)



TYPICAL APPLICATION FOR a 4 DIGIT COUNTER (FIG. 4)



M004 Brief Description

The contents of 4 decades are memorized on 16 latch flip-flops. The content of one decade is shifted towards the decoder by means of the multiplexer; the selection is performed by control signals P, Q, R, S, which also appear at the output so as to select one display at a time.

Multiplexer scanning takes place at external "scan" signal frequency.

It is also possible to read the content of 2, 3 or 4 decades by means of the control signals M and N.

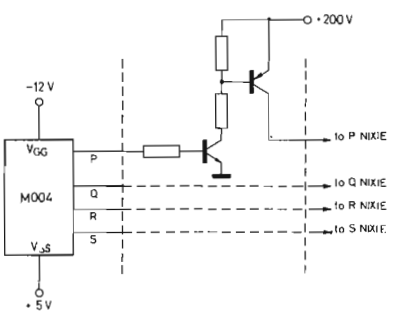
TYPICAL APPLICATION

The M 003 and M 004 devices find their typical application in all counting and display systems, such as digital instruments watches, etc.

It follows that we can realize a binary-decoder (able to count up to 9999) with only two packages. The circuitry related to this application is shown in fig. 4.

For driving displays such as nixie tubes, the interface circuit shown in fig. 5 should be used, so allowing the unselected display to be kept OFF, according to the signal logic level selected.

FIG. 5



4 - digit multiplexer/decoder

The contents of 4 decades are memorized by 16 latch flip-flops. The content of one decade is shifted towards the decoder by means of the multiplexer; selection is preformed by control signals P,Q,R,S, which also appear at the output so as to select only one display at a time. The M 004 also has a decoder with 10 decimal outputs. Two control signals M and N, allow the number of channels for scanning to be decided. Four outputs (P,Q,R,S,) indicate the channel selected and allow switch-on of one display and switch-off of the others. Display switch-off is also possible asynchronously by means of the blank signals. All the outputs are open-drain and the inputs are fully compatible with DTL/TTL. The device is realized on a single monolithic chip by means of the silicon-nitride Planox technology.

EXTENDED TEMPERATURE RANGE
-55°C to 125°C

STANDARD TEMPERATURE RANGE
0°C to 70°C

- FULLY TTL COMPATIBLE
- D.C. TO 1MHz OPERATION
- SINGLE PHASE CLOCK
- INPUT GATE PROTECTION

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Input Voltage (1)	-20 to 0.3V
Clock Voltage (1)	-20 to 0.3V
Supply Voltage (1)	-20 to 0.3V
Storage temperature range	-55°C to + 150°C

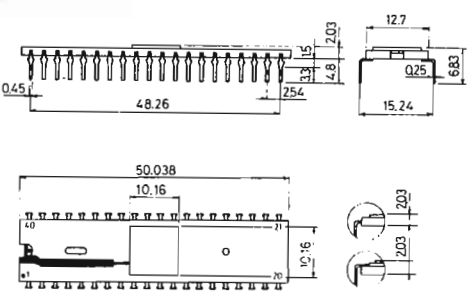
ORDERING NUMBER
M 004 T1 (for standard temperature range)
M 004 T2 (for extended temperature range)

1) Note: This voltage is with respect to the V_{SS} pin voltage

PIN CONNECTION

1	V_{SS}	21	B4
2	"9"	22	B3
3	"8"	23	B2
4	"7"	24	B1
5	"6"	25	A4 (LSD)
6	"5"	26	A3 (LSD)
7	"4"	27	A2 (LSD)
8	"3"	28	A1 (LSD)
9	"2"	29	V_{GG}
10	"1"	30	M
11	"0"	31	N
12	SAMPLE	32	P
13	D4 (MSD)	33	Q
14	D3 (MSD)	34	R
15	D2 (MSD)	35	S
16	D1 (MSD)	36	BLANK S
17	C4	37	BLANK R
18	C3	38	BLANK Q
19	C2	39	BLANK P
20	C1	40	SCAN

PHYSICAL DIMENSIONS
40 lead ceramic DIP

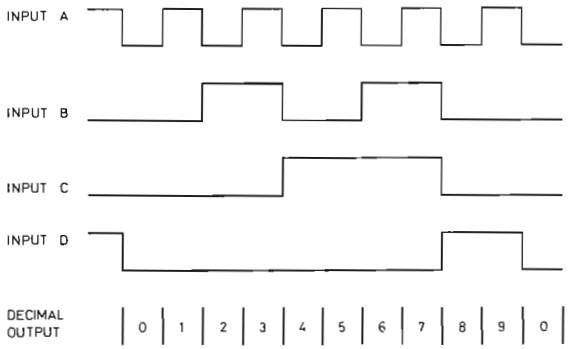


The package can be available in P044 SGS-ATES package.

ELECTRICAL CHARACTERISTICS (V_{GG}= -12V ± 1V; V_{SS}= +5V ± 0.5V unless otherwise noted)

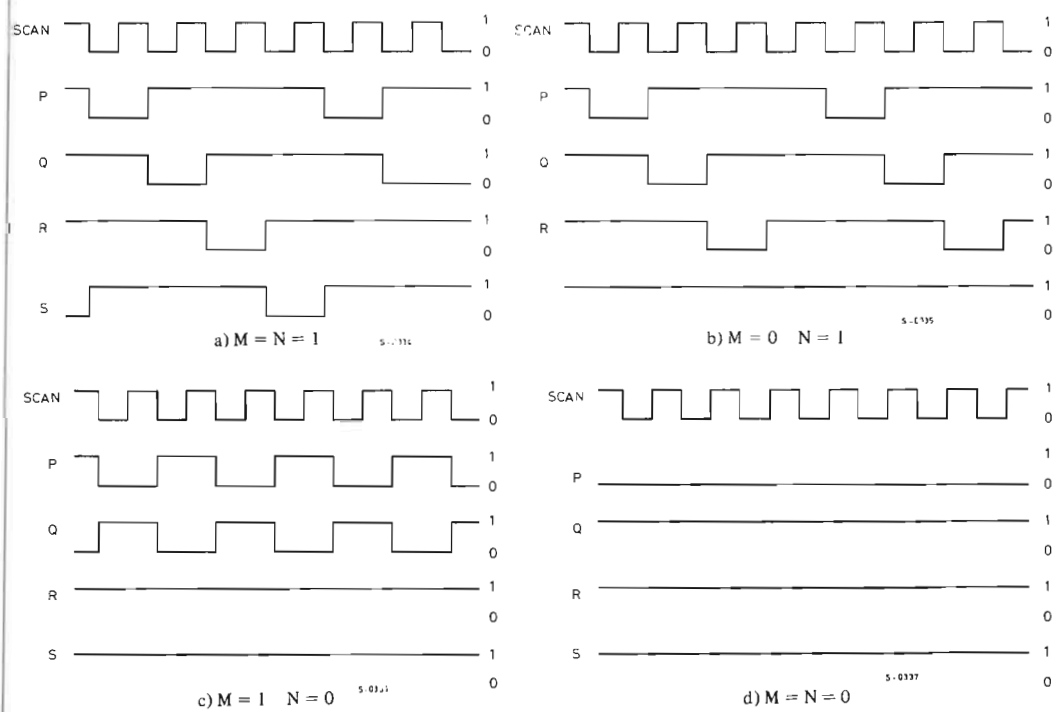
SYMBOL	CHARACTERISTICS	Min.	Typ.	Max.	UNIT	TEST CONDITIONS	
	CLOCK INPUTS (SAMPLE, SCAN)						
f	Repetition Rate Range	0		1	MHz		
C_{pw}	Pulse Width	400			ns		
ϕd	Pulse Separation	400			ns		
tr, tf	Rise and Fall Time			1	μs	T_A=25°C	
V_{ILcp}	"0" Level Voltage			V_{SS}-4.2	V		
V_{IHcp}	"1" Level Voltage	V_{SS}-1.5			V		
t set-up	Sample Set-up Time	200			ns	see waveforms	
t hold	Sample Hold Time	200			ns	see waveforms	
I_{Lcp}	Leakage Current			1	μA	V_{cp}=V_{SS}-15V	T_A = 25°C
C_{cp}	Input Capacitance			10	pF	V_{cp}=V_{SS}	f = 1 MHz
	DATA AND CONTROL INPUTS						
V_{IL}	"0" Level Voltage			V_{SS}-4.2	V		
V_{IH}	"1" Level Voltage	V_{SS}-1.5			V		
I_L	Leakage Current			1	μA	V_{in}=V_{SS}-15V	T_A = 25°C
C_{in}	Input Capacitance			10	pF	V_{in}=V_{SS}	f = 1 MHz
	DATA OUTPUTS						
R_{on}	Output ON Resistance			3.5	kΩ	I_{source} = 1mA	
R_{off}	Output OFF Resistance	100			MΩ		
	POWER CONSUMPTION						
I_{GG}	Gate Supply Current		18		mA		
P_d	Total Power Consumption		300		mW		

DECADE INPUTS/DECIMAL OUTPUT WAVEFORMS (Note 1)



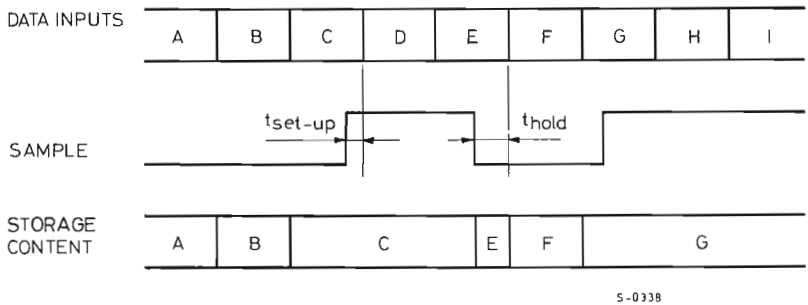
Note 1 : with sample at "1" level

MULTIPLEXER WAVEFORMS (Note 2)

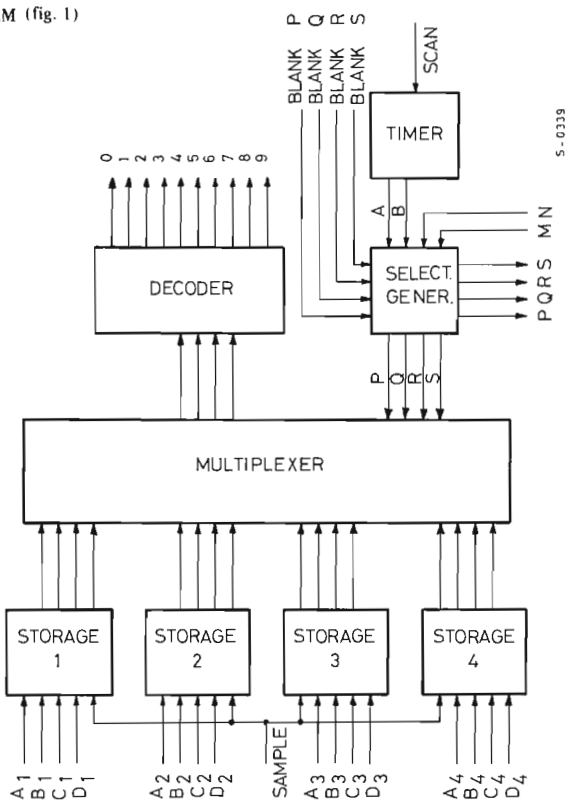


Note 2 : a V_{IH} level on a blank input forces the corresponding output transistor in the OFF state

SAMPLE FUNCTION

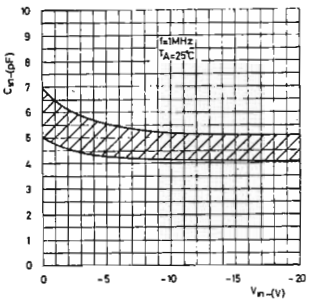


BLOCK DIAGRAM (fig. 1)

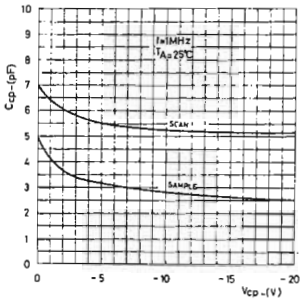


TYPICAL ELECTRICAL CHARACTERISTICS

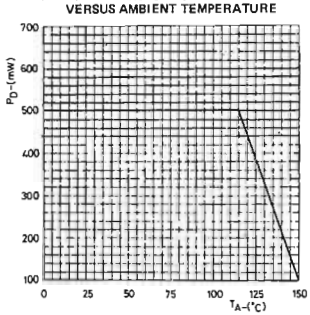
INPUT CAPACITANCE
VERSUS INPUT VOLTAGE



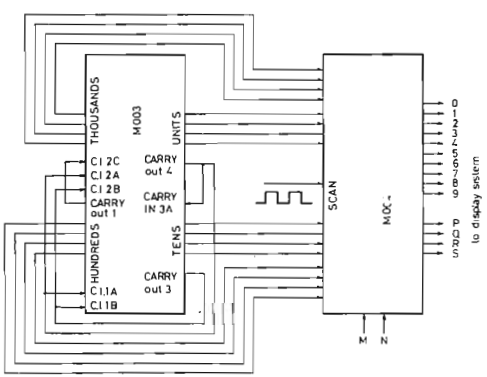
CLOCK CAPACITANCE
VERSUS CLOCK VOLTAGE



MAXIMUM PACKAGE POWER DISSIPATION
VERSUS AMBIENT TEMPERATURE



TYPICAL APPLICATION FOR a 4-DIGIT COUNTER (fig. 2)

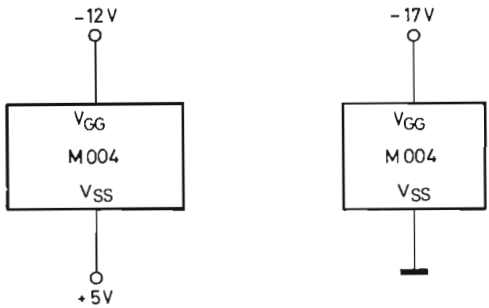


The M 003 and M 004 devices find their typical application in all counting and display systems, such as digital instruments, watches, etc.. It follows that we can realize a binary-decoder (able to count up to 9999) with only two packages (chips). The circuitry related to this application is shown in fig. 2.
For driving displays such as nixie tubes, the interface circuits shown in figs. 3, 4 should be used, so allowing the unselected displays to be kept OFF, according to the select signal logic level.

Brief description of the M 003.

The M 003 is a quad up/down decade counter arranged as two subsystems of two decades each.
Each subsystem has a single up/down control zero and nine reset clock line. Common count enable input is provided for all decades, while synchronous carry-in inputs are available for each single counter.

POWER CONNECTION OF M004 (fig. 3).

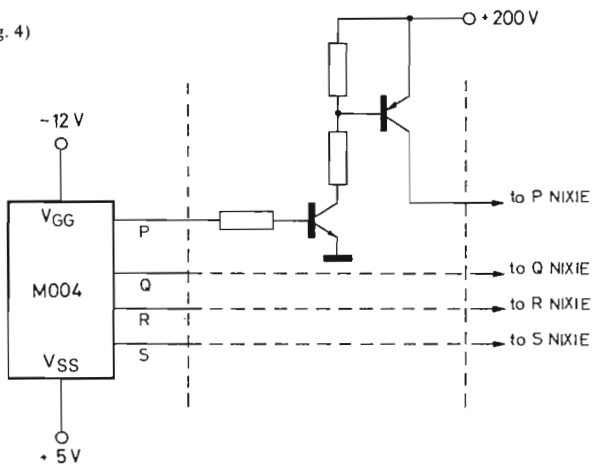


M004 used with TTL only

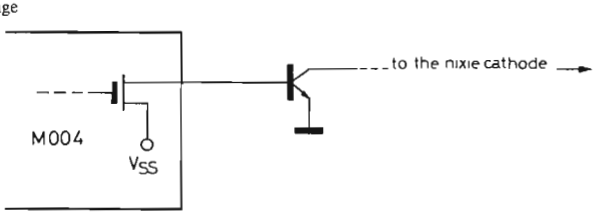
M004 used with MOS only

DISPLAY INTERFACES (fig. 4)

to drive nixie anode voltage



to drive nixie cathode voltage



MOS INTEGRATED CIRCUIT

M 005

PRELIMINARY DATA

4 CHANNEL MULTIPLEXER

The M 005 is a 4 channel multiplexer constructed on a single monolithic chip using P-channel low threshold silicon gate technology. The device is available in 10-lead metal case similar to Jedec TO-100.

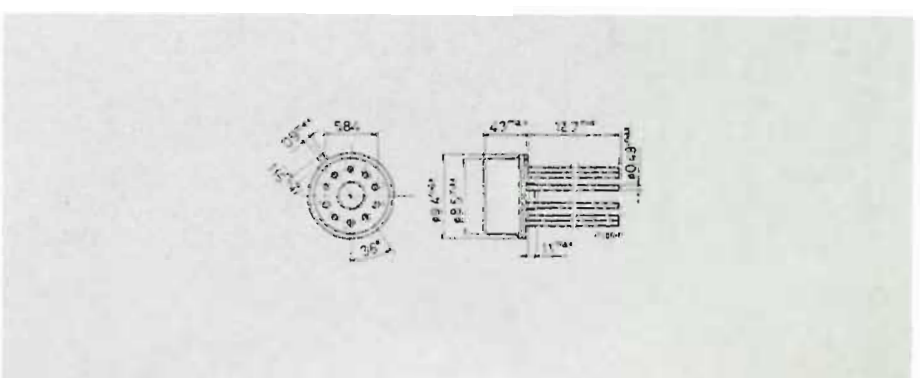
ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain to source voltage	-10 to 0.3	V
V_{GS}	Gate to source voltage	-35 to 0.3	V
V_{GD}	Gate to drain voltage	-25 to 0.3	V
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	0 to 70	°C

ORDERING NUMBER: M 005 T1

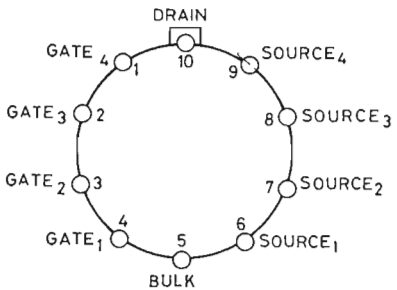
MECHANICAL DATA

Dimensions in mm

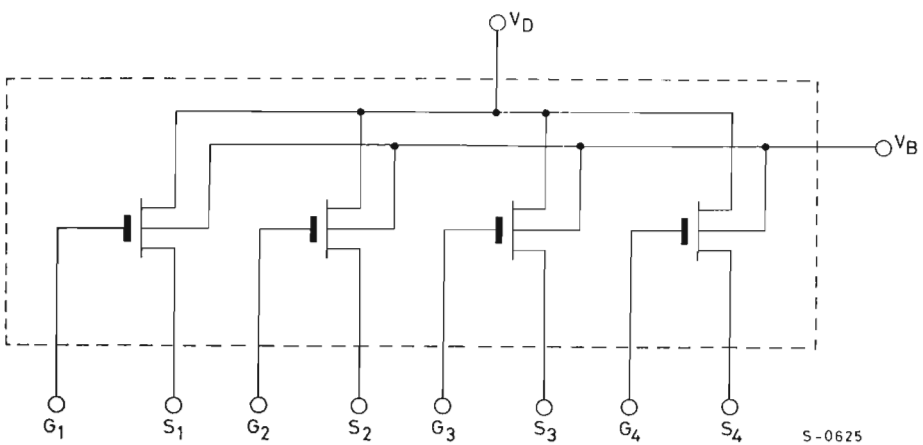


M 005

CONNECTION DIAGRAM (top view)



SCHEMATIC DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_i	Analog input voltage	V_{GS} = -20V V_{BULK} = 10V			±10	V
V_{THO}	Threshold voltage	$V_{DS} = V_{GS}$ I_{DS} = 100 μA V_{BS} = 0	-1		-2.5	V
R_{DS}	Drain to source on resistance	V_{GS} = -10V I_{DS} = 10 mA V_{BS} = 0		20	50	Ω
		V_{GS} = -20V I_{DS} = 10 mA V_{BS} = 0		13	20	Ω
I_{GL}	Gate leakage current	V_{GS} = -10V V_{DS} = 0 V_{BS} = 0			-1	nA
I_{DL}	Drain leakage current	V_{DS} = -5V V_{GS} = 0 V_{BS} = 0			-20	nA
I_D	Drain current	V_{GS} = V_{DS} = -5V V_{BS} = 0	-60			mA

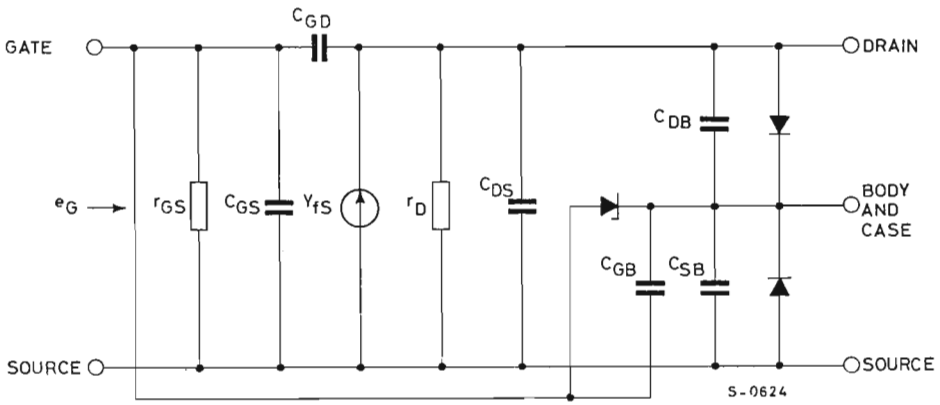
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
Y_{fs}	Forward transadmittance	V_{DS} = -3V V_{GS} = -10V V_{BS} = 0V		12.000		μmho
C_{DS}*	Drain to source capacitance	V_{DS} = 0 f = 1 MHz V_{iPP} = 15 mV		0.15	0.20	pF
C_{GD}*	Gate to drain capacitance	V_{GD} = 0 f = 1 MHz V_{iPP} = 15 mV		2	3	pF
C_{GS}*	Gate to source capacitance	V_{GS} = 0 f = 1 MHz V_{iPP} = 15 mV		2	3	pF
C_{SB}*	Source to body capacitance	V_{SB} = 0 f = 1 MHz V_{iPP} = 15 mV		8	10	pF
C_{DB}*	Drain to body capacitance	V_{DB} = 0 f = 1 MHz V_{iPP} = 15 mV		32	40	pF
C_{GB}*	Gate to body capacitance	V_{GB} = 0 f = 1 MHz V_{iPP} = 15 mV		4	6	pF

*This parameter is periodically sampled and not 100% tested

SMALL SIGNAL EQUIVALENT CIRCUIT

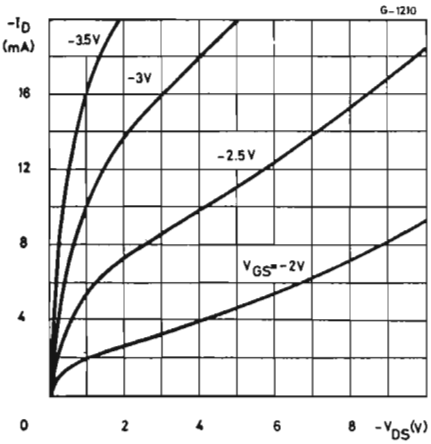
(conditions : $V_{GS} = -10V$, $V_{DS} = -3V$, $V_{BS} = 0$) $I \simeq 150$ mA



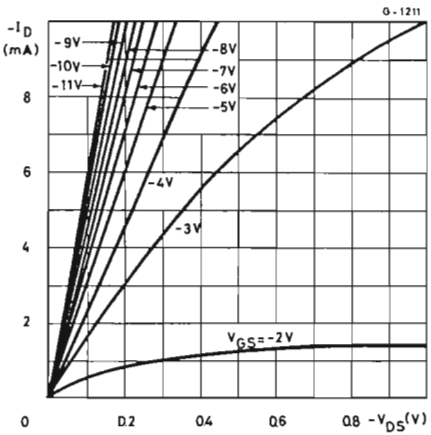
Symbol	Characteristics	Typical value	Unit
Diodes	All diodes are to be considered perfect diodes		
r_{GS}	Gate to source leakage resistance and diode leakage resistance	10^{10}	Ω
r_D	Dynamic drain resistance	0.5	kΩ
C_{GS}	Gate to source capacitance	2	pF
C_{GD}	Gate to drain capacitance	2	pF
C_{DS}	Drain to source capacitance	0.15	pF
C_{GB}	Gate to body capacitance	6	pF
C_{DB}	Drain to body capacitance	40	pF
C_{SB}	Source to body capacitance	10	pF
Y_{fs}	Forward transadmittance	12.000	μmho

M 005

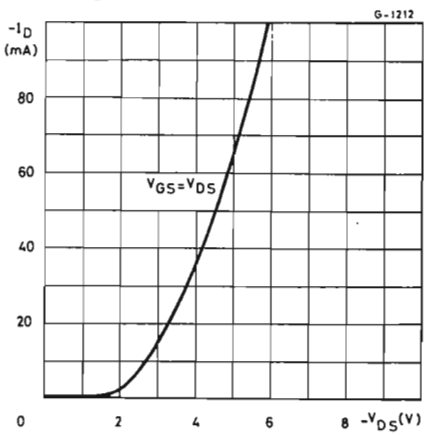
Drain current vs. drain to source voltage



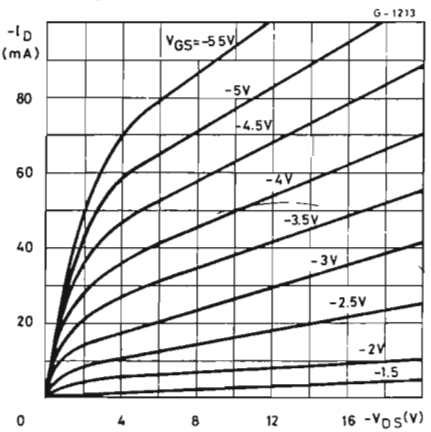
Drain current vs. drain to source voltage



Drain current vs. drain to source voltage

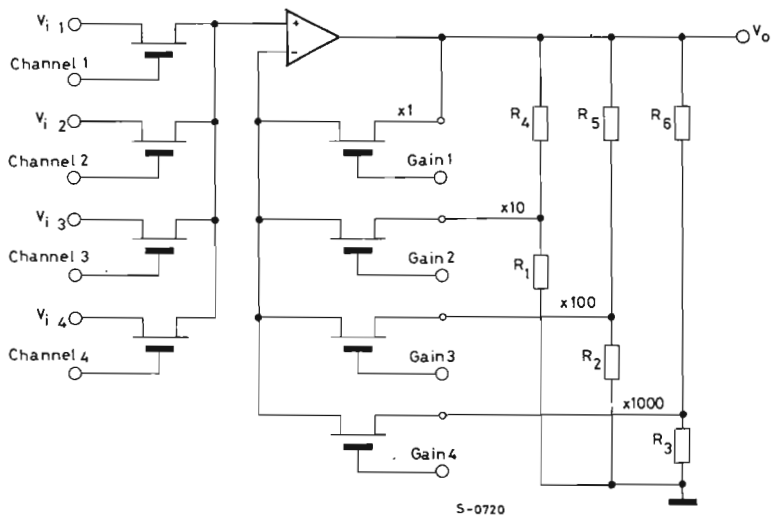


Drain current vs. drain to source voltage

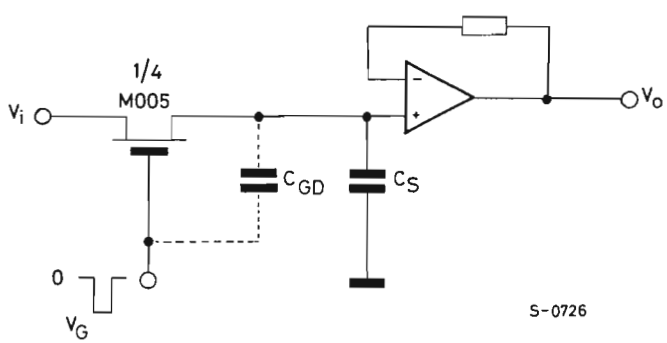


TYPICAL APPLICATIONS

Variable gain amplifier with multiplexed inputs



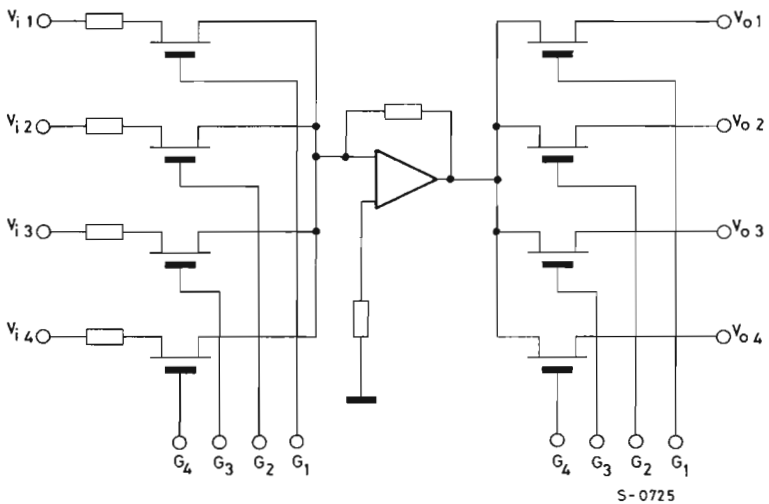
Sample and hold



M 005

TYPICAL APPLICATIONS (continued)

Multiplexing - demultiplexing



MOS INTEGRATED CIRCUIT

M 009

PRELIMINARY DATA

2 CHANNEL MULTIPLEXER

The **M 009** is a 2 channel multiplexer constructed on a single monolithic chip using P-channel low threshold silicon gate technology. The device is available in 8-lead metal case similar to Jedec TO-99.

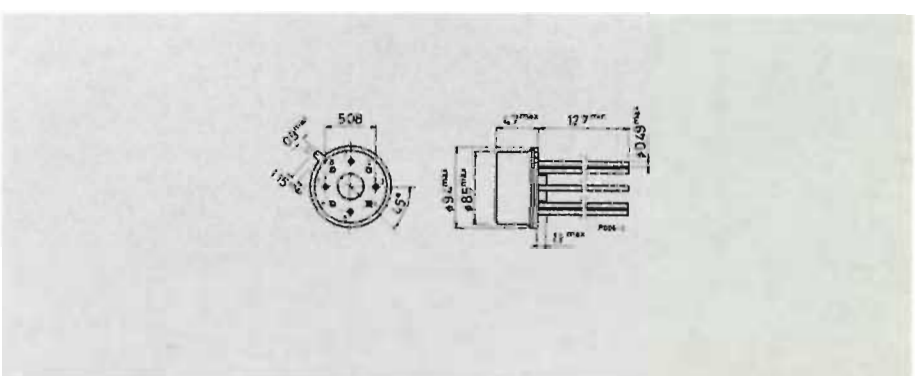
ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain to source voltage	-10 to 0.3	V
V_{GS}	Gate to source voltage	-35 to 0.3	V
V_{GD}	Gate to drain voltage	-25 to 0.3	V
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	0 to 70	°C

ORDERING NUMBER: M 009 T1

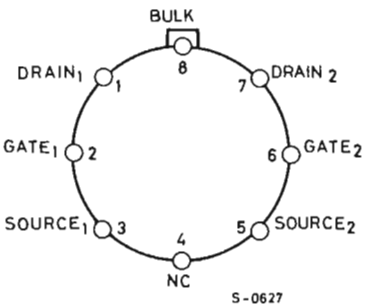
MECHANICAL DATA

Dimensions in mm

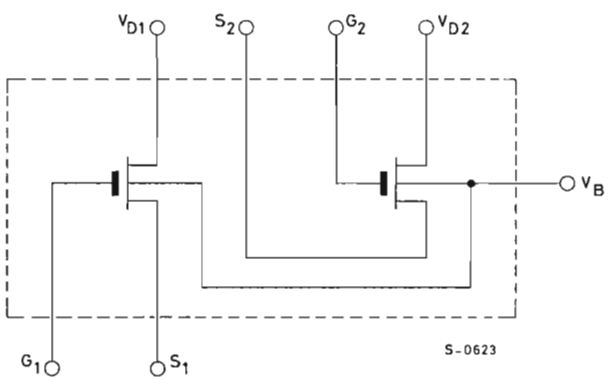


M 009

CONNECTION DIAGRAM (top view)



SCHEMATIC DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_i	Analog input voltage	V_{GS} = -20V V_{BULK} = 10V			±10	V
V_{THO}	Threshold voltage	$V_{DS} = V_{GS}$ I_{DS} = 100 μA V_{BS} = 0	-1		-2.5	V
R_{DS}	Drain to source on resistance	V_{GS} = -10V I_{DS} = 10 mA V_{BS} = 0		20	50	Ω
		V_{GS} = -20V I_{DS} = 10 mA V_{BS} = 0		13	30	Ω
I_{GL}	Gate leakage current	V_{GS} = -10V V_{DS} = 0 V_{BS} = 0			-1	nA
I_{DL}	Drain leakage current	V_{DS} = -5V V_{GS} = 0 V_{BS} = 0			-20	nA
I_D	Drain current	$V_{GS} = V_{DS}$ = -5V V_{BS} = 0	-60			mA

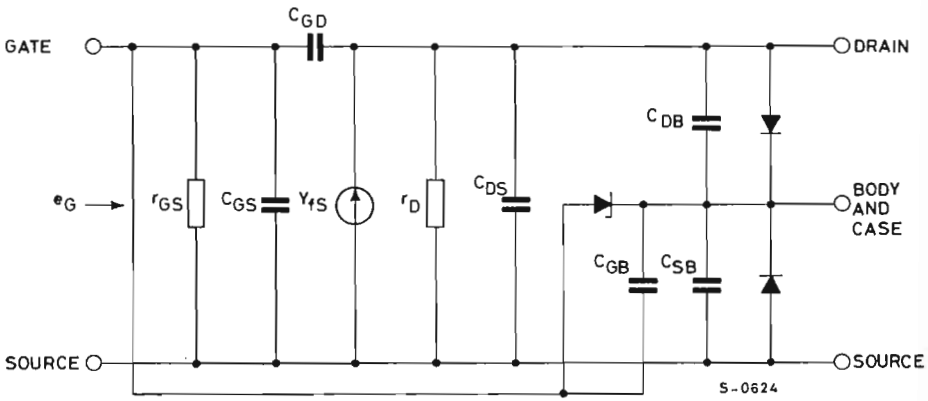
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 0 to 70°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
Y_{fs}	Forward transadmittance	V_{DS} = -3V V_{GS}= -10V V_{BS} = 0V		12.000		μmho
C_{DS}*	Drain to source capacitance	V_{DS} = 0 f = 1 MHz V_{iPP} = 15 mV		0.15	0.20	pF
C_{GD}*	Gate to drain capacitance	V_{GD} = 0 f = 1 MHz V_{iPP} = 15 mV		2	3	pF
C_{GS}*	Gate to source capacitance	V_{GS} = 0 f = 1 MHz V_{iPP} = 15 mV		2	3	pF
C_{SB}*	Source to body capacitance	V_{SB} = 0 f = 1 MHz V_{iPP} = 15 mV		8	10	pF
C_{DB}*	Drain to body capacitance	V_{DB} = 0 f = 1 MHz V_{iPP} = 15 mV		8	10	pF
C_{GB}*	Gate to body capacitance	V_{GB} = 0 f = 1 MHz V_{iPP} = 15 mV		4	6	pF

*This parameter is periodically sampled and not 100% tested

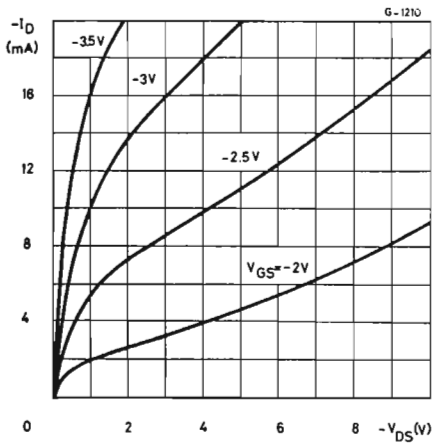
SMALL SIGNAL EQUIVALENT CIRCUIT

(conditions : $V_{GS} = -10V$, $V_{DS} = -3V$, $V_{BS} = 0$) $I \simeq 150$ mA)

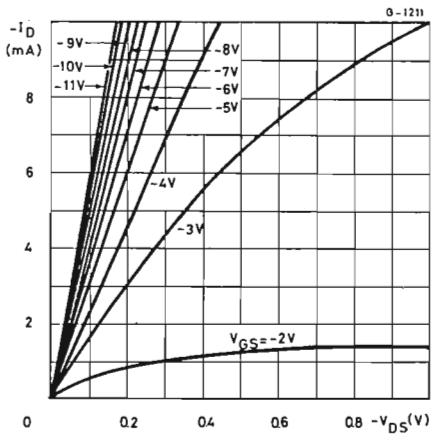


Symbol	Characteristics	Typical value	Unit
Diodes	All diodes are to be considered perfect diodes		
r_{GS}	Gate to source leakage resistance and diode leakage resistance	10^{10}	Ω
r_D	Dynamic drain resistance	0.5	kΩ
C_{GS}	Gate to source capacitance	2	pF
C_{GD}	Gate to drain capacitance	2	pF
C_{DS}	Drain to source capacitance	0.15	pF
C_{GB}	Gate to body capacitance	6	pF
C_{DB}	Drain to body capacitance	40	pF
C_{SB}	Source to body capacitance	10	pF
Y_{fs}	Forward transadmittance	12.000	μmho

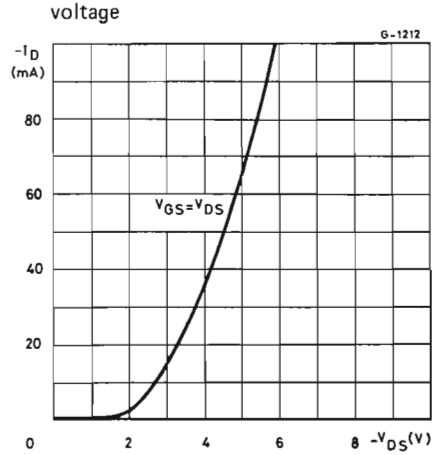
Drain current vs. drain to source voltage



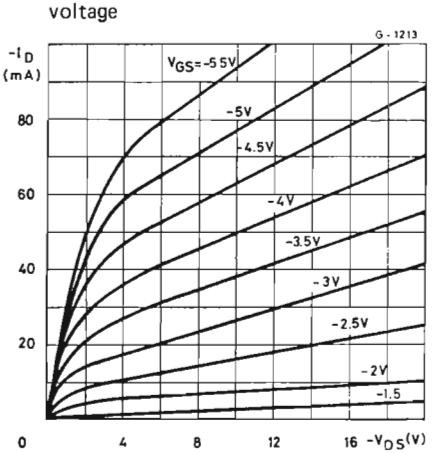
Drain current vs. drain to source voltage



Drain current vs. drain to source voltage

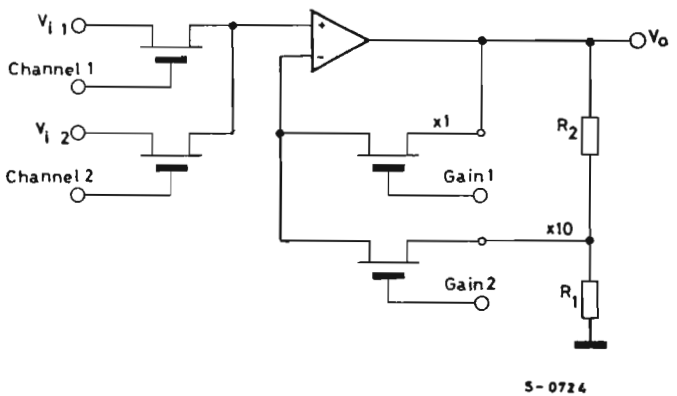


Drain current vs. drain to source voltage

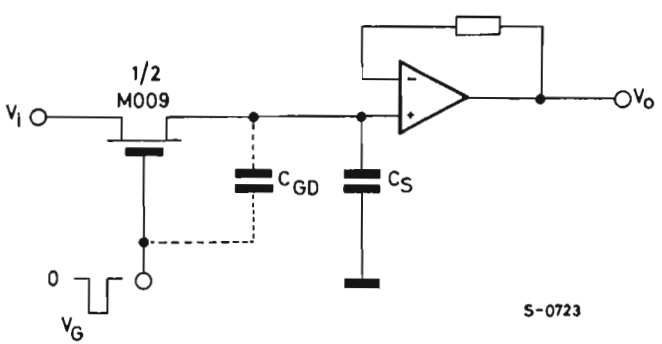


TYPICAL APPLICATIONS

Variable gain amplifier with multiplexed inputs

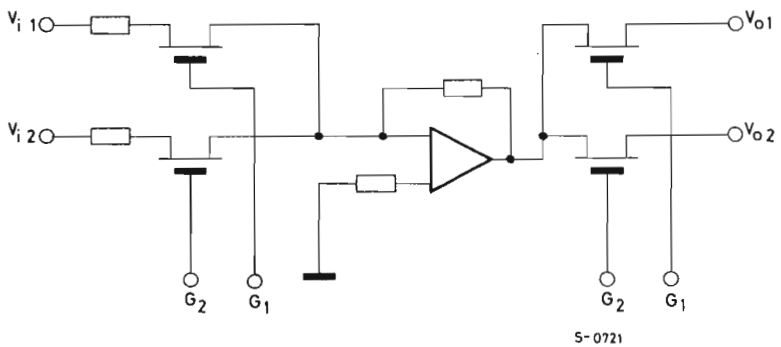


Sample and hold

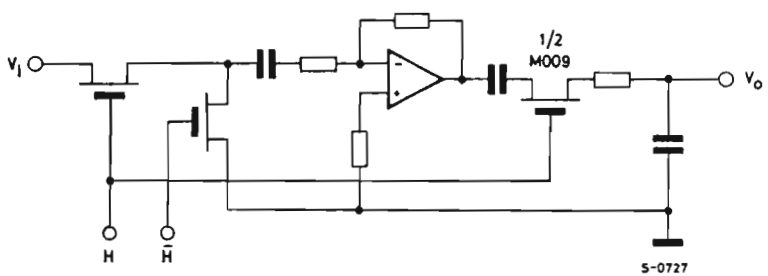


TYPICAL APPLICATIONS (continued)

Multiplexing - demultiplexing



Series parallel chopper (low direct voltage amplification)



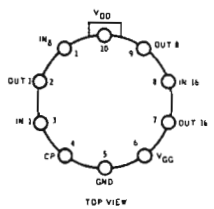
25 bit static shift register

EXTENDED TEMPERATURE RANGE, - 55°C + 85°C
STANDARD TEMPERATURE RANGE, 0°C + 70°C

The M 120 is a 25 bit Static Shift Register. It is a monolithic integrated circuit utilizing P-channel enhancement mode MOS technology. Input and output access is made available in 16,8 and 1 bit increments. This device is designed for use in single phase clock sequential digital systems as a delay line or memory element.

- **Input gate protection**
- **Low power 2 mW/bit**
- **Single phase clock**
- **Good capacitive driving capability**

CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

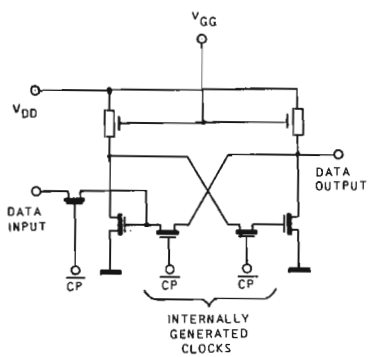
(above which the useful life may be impaired)

Storage Temperature	-55°C to + 150°C
Voltage on Clock, Inputs and Supply Pins	-30°V to + 0,3 V

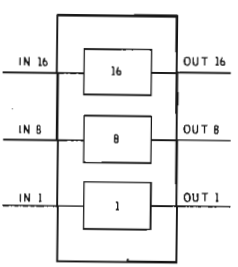
OPERATING LIMITS

Supply Voltages	$V_{GG} = -27\ V \pm 1V$ $V_{DD} = -13\ V \pm 1V$

SCHEMATIC DIAGRAM (ONE BIT)

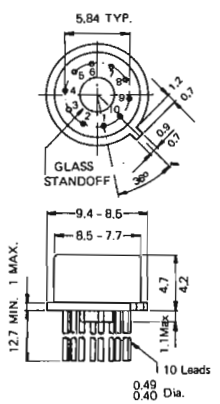


BLOCK DIAGRAM



PHYSICAL DIMENSIONS

similar to Jedec TO 100 outline



Notes All dimensions in mm.
Leads are gold-plated Kovar.

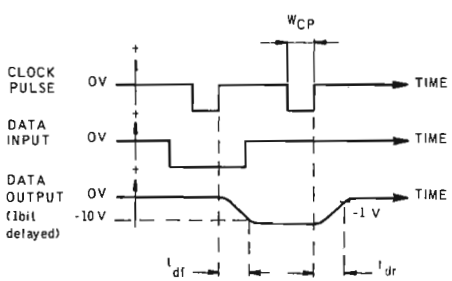
ORDERING NUMBER

M120 T1 (for standard temperature range)
M120 T8 (for extended temperature range)

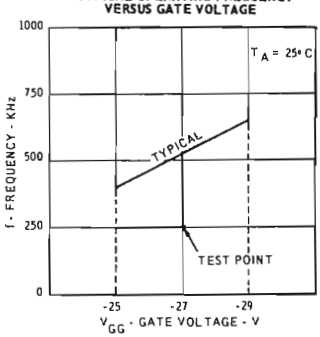
ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{GG} (Pin 6) = - 27 ± 1V, V_{DD} (Pin 10) = - 13 ± 1V, Load 10 Mohm 10 pF, unless otherwise specified)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	CONDITIONS
	Power Consumption		50		mW	V_{clock} = 0 V
	Operating Frequency	0		250	kHz	V_{GG} = - 27 V
V_{CP}	Clock Pulse Amplitude "0" level			- 2	V	
	"1" level	-9			V	
W_{CP}	Clock Pulse Width	1		100	µs	
	Clock Pulse Rise and Fall Time			10	µs	
	Clock Capacitance		3		pF	V_{CP} = 0 V
I_{CL}	Clock Leakage Current			- 1	µA	V_{CP} = - 20 V
V_{IL}	Input Amplitude "0" level			- 2	V	
V_{IH}	"1" level	-9			V	
C_{in}	Input Capacitance		2.5		pF	V_{in} = 0 V
I_{IL}	Input Leakage Current			- 1	µA	V_{in} = - 20 V
V_{OL}	Output Levels "0" level			- 1	V	I_{OUT} = - 10 µA
V_{OH}	"1" level	-10			V	I_{OUT} = - 10 µA
t_{df}	Time Delay-Fall		1		µs	
t_{dr}	Time Delay-Rise		1.2		µs	

TIMING DIAGRAM



TYPICAL OPERATING FREQUENCY VERSUS GATE VOLTAGE

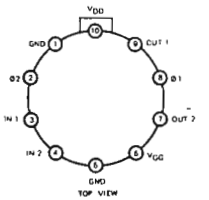


dual 16-bit static shift register

EXTENDED TEMPERATURE RANGE - 55 °C ÷ 85°C
STANDARD TEMPERATURE RANGE 0 ÷ 70° C

The M 122 is a Dual 16-Bit Static Shift Register. It is a monolithic integrated circuit utilizing P-Channel Enhancement Mode MOS technology. It is designed to operate on a two phase clock in delay line or in serial binary or BCD data storage applications. For DC storage conditions, it is important that $\emptyset_1$ is a logic "0" and $\emptyset_2$ is a logic 1.

CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(above which the useful life may be impaired)

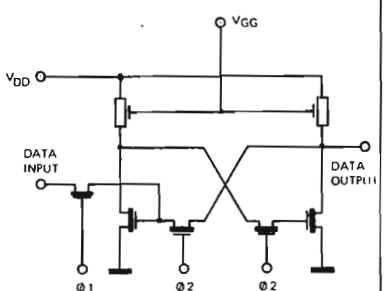
Drain Voltage (V_{DD})	- 30V to + 0.3V
Gate Voltage (V_{GG})	- 30V to + 0.3V
Clock and Data Input Voltages	- 30V to + 0.3V
Storage Temperature	- 55° C to + 150°C

OPERATING CONDITIONS

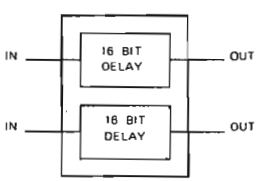
Temperature range (Extended)	- 55 ÷ 85° C
Temperature range (Standard)	0 ÷ 70° C
Supply Voltage	V_{DD} = -13V ± 1V V_{GG} = -27V ± 1V

SCHEMATIC DIAGRAM

(one bit)

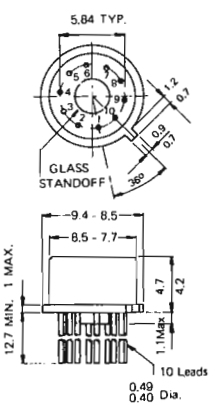


BLOCK DIAGRAM



PHYSICAL DIMENSIONS

similar to JEDEC to 100 outline



Notes All dimensions in mm.

ORDERING NUMBER

M 122 T1 (for standard temperature range)
M 122 T8 (for extended temperature range)

ELECTRICAL CHARACTERISTICS

V_{DD} = - 13 V ± 1V, V_{GG} = - 27 ± 1 V, Load = 10 MΩ and 10pF, T_A = - 55°C to 85°C or 0°C to 70°C according to the type No., unless otherwise specified.

CHARACTERISTICS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Clock Repetition Rate	D.C.		1	MHz	
Clock Pulse widths					
ϕ_1 pw	0.4		10	μs	See Figure 1
ϕ_2 pw	0.4		10	μs	See Figure 1
Clock Delay (d d)	0.01			μs	See Figure 1
Clock Pulse Rise and Fall Time (10% to 90%)			5	μs	See Figure 1
Clock Pulse Logic Levels (ϕ_1 & ϕ_2)					
Logic "0"			- 2	V	
Logic "1"	-26		-28	V	
Clock Pulse Input Capacitance (ϕ_1 & ϕ_2)		4		pF	$\phi_1 = \phi_2 = 0V$
Data Pulse Width (Dpw)	0.4			μs	
Data Input Capacitance		2		pF	V_{IN} = 0 Volt
Data Input Logic Levels					
Logic "0"			- 2	V	
Logic "1"	- 9			V	
Data Input Leakage Current			1	μA	V_{IN} = - 20V
Clock Input Leakage Current			100	μA	V_{IN} = - 26V
Clock (ϕ_2) Input Impedance	60			KΩ	ϕ_1 = - 26V ϕ_2 = 0V
Output Logic Levels					
Logic "0"		- 0.5	- 1	V	
Logic "1"	- 10	- 11		V	
Output Impedance to Ground		2	3	KΩ	Output at Logic "0"
Output Drive Capability	- 5			V	R_L = 4 kΩ to Ground
Power Supply Current Drain V_{DD}			10	mA	V_{DD} = - 13V
Power Supply Current Drain V_{GG}			2	mA	V_{GG} = - 27V

TIMING DIAGRAMS

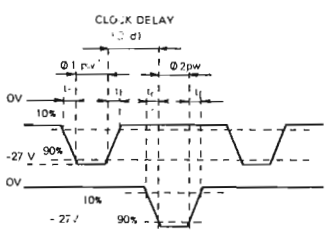


Figure 1

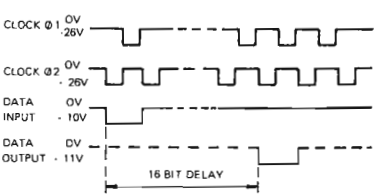


Figure 2

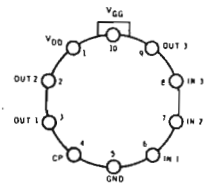
64 bit 1 ø static shift register

EXTENDED TEMPERATURE RANGE, -55°C ÷ 85°C
STANDARD TEMPERATURE RANGE, 0°C ÷ 70°C

- **Single phase clock**
- **Low power consumption - less than 3 mW/bit**
- **High speed operation – DC to 1 MHz**

The M 124 is a 64-bit 1 Ø static shift register arranged as a Dual 16, Single 32 in a TO-100 package. It is a monolithic integrated circuit utilizing P-channel Enhancement Mode Technology. Its main applications as delay line or bit storing device are in computer, data acquisition and data control systems, telemetry and peripheral equipments.

CONNECTION DIAGRAM
(Top view)



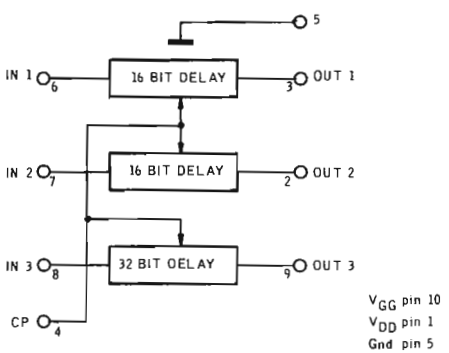
ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Drain Voltage (V_{DD})	- 30V to + 0.3 V
Gate Voltage (V_{GG})	- 30V to + 0.3 V
Clock and Data Input Voltages	- 30V to + 0.3 V
Storage Temperature	- 55°C to +150°C

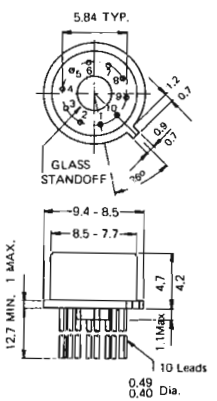
OPERATING CONDITIONS

Supply Voltage	$V_{DD} = -13V \pm 1V$ $V_{GG} = -27V \pm 1\%$
Temperature Range (extended)	-55°C to 85°C
Temperature Range (standard)	0°C to 70°C

BLOCK DIAGRAM



PHYSICAL DIMENSIONS
similar to
Jedec TO 100 outline



Notes All dimensions in mm.

ORDERING NUMBER

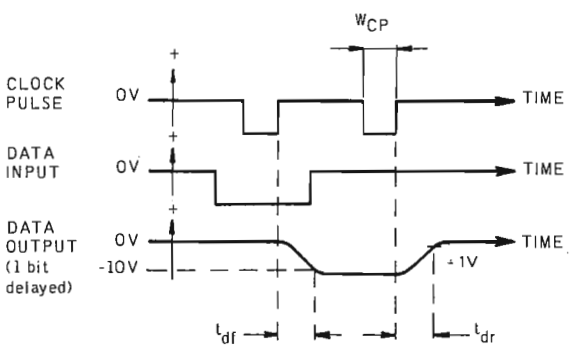
M 124 T8 (for extended temperature range)
M 124 T1 (for standard temperature range)

EXTENDED TEMPERATURE RANGE

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{GG} = - 27 ± 1V, V_{DD} = - 13 ± 1V, unless otherwise specified)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
	Power Consumption		200		mW	
	Operating Frequency	DC		1	MHz	V_{GG} = - 27 V
V_{CP}	Clock Pulse Amplitude "0" level			- 2	V	
	"1" level	- 9			V	
W_{CP}	Clock Pulse Width	0.3		100	µs	
	Clock Pulse Rise and Fall Time			10	µs	
	Clock Capacitance		8		pF	V_{CP} = 0 V
I_{CL}	Clock Leakage Current			- 1	µA	V_{CP} = - 20 V
V_{IL}	Input Amplitude "0" level			- 2	V	
V_{IH}	"1" level	- 9			V	
C_{in}	Input Capacitance		2.5		pF	V_{in} = 0 V
I_{IL}	Input Leakage Current			- 1	µA	V_{in} = - 20 V
V_{OL}	Output Levels "0" level			- 1	V	I_{OUT} = - 10 µA
V_{OH}	"1" level	-10			V	I_{OUT} = - 10 µA
t_{df}	Time Delay Fall		0.4	0.5	µs	V_{GG} = - 27 V
t_{dr}	Time Delay-Rise		0.4	0.5	µs	V_{GG} = - 27 V

TIMING DIAGRAM



Dual 256-bit dynamic shift register

STANDARD TEMPERATURE RANGE
0°C to 70°C

- INPUT GATE PROTECTION
- TTL DRIVE CAPABILITY
- ON-CHIP RECIRCULATING LOGIC

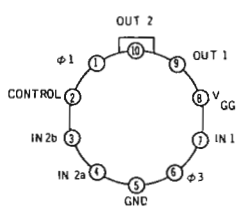
M125 consists of two separate 256-bit dynamic shift registers with independent input and output terminals, while clocks, power and ground are common. One power supply and two external clocks are required for operation with two further clocks generated internally. The entire device is constructed on a single monolithic chip using MOS P-channel technology. One section incorporates recirculating logic for application as an accumulator. The two sections could be cascaded to have a 512-bit serial accumulator. Input data should be stable from the leading edge of ϕ 1 to the leading edge of ϕ 3; while output data starts changing with the leading edge of ϕ 3. The control input allows the device to accept data from either the 2a or 2b inputs.

ORDERING NUMBER
M125 T1

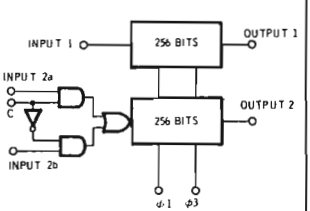
ABSOLUTE MAXIMUM RATINGS

Input Voltage	-30V to +0.3V
Clock Voltage	-30V to +0.3V
Supply Voltage	-30V to +0.3V
Storage Temperature Range	-55°C to 150°C

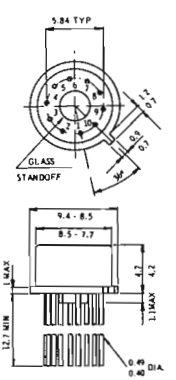
CONNECTION DIAGRAM
(top view)



LOGIC DIAGRAM



PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-100



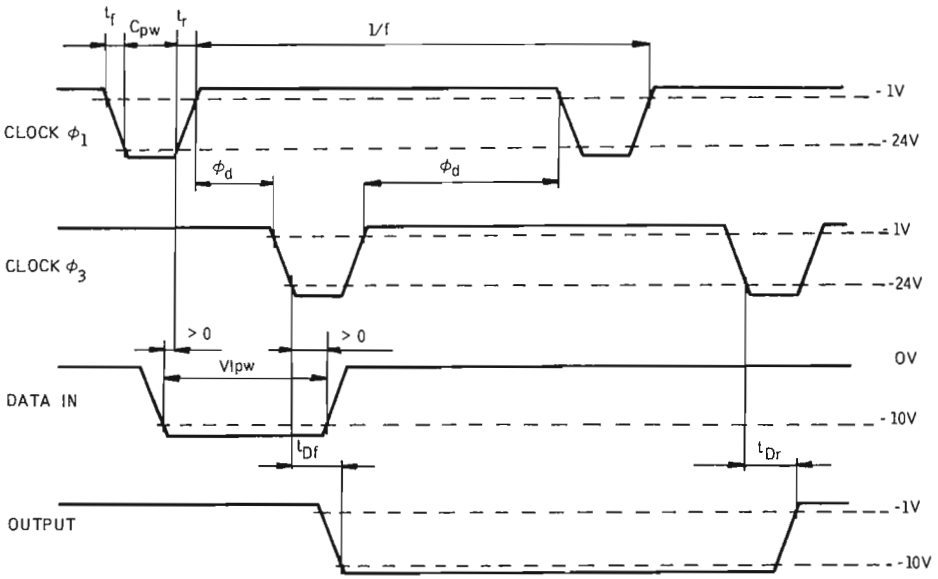
Note : all dimensions in mm.

ELECTRICAL CHARACTERISTICS

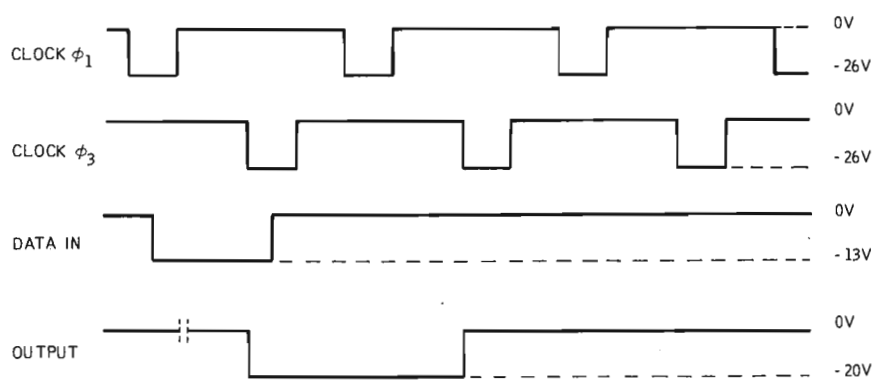
(T_A = 25°C; V_{GG} = - 27V ± 1V; load = 10M Ω and 10 pF unless otherwise noted)

SYMBOL	CHARACTERISTIC	Min.	Typ.	Max.	Unit	TEST CONDITIONS
	CLOCK PULSES					
f	Repetition Rate Range	10		1000	kHz	
C_{pw}	Pulse Width	0.15			µsec	See Fig. 1
Ø d	Pulse Separation	0.2			µsec	See Fig. 1
V_{ILcp}	"O" Level Voltage			- 1	V	
V_{IHcp}	"1" Level Voltage	-25			V	
C_{cp}	Input Capacitance		120		pF	V = 0 f = 1 MHz
$I_{L\,cp}$	Leakage Current			1	µA	V_{cp} = - 27V
	DATA INPUT AND CONTROL INPUT					
V_{IL}	"O" Level Voltage			- 2	V	
V_{IH}	"1" Level Voltage	-10			V	
C_{in}	Input Capacitance		3		pF	V = 0 f = 1 MHz
I_L	Leakage Current			1	µA	V_{in} =-20V
	DATA OUTPUT					
V_{OL}	"O" Level Voltage		-0.5	- 1	V	I_{OL} =-10 µA
V_{OH}	"1" Level Voltage	-11			V	I_{OH} = -10 µA
R_{on}	"O" Level On Resistance			6	k Ω	
R_{on}	"1" Level On Resistance			6	k Ω	
	POWER CONSUMPTION					
I_{GG}	Gate Current		3.5	6	mA	V_{GG}= -27V f = 1 MHz
	RESPONSE TIME					
t_{Df}	Delay Time to Fall		100	150	nsec	See Fig. 1
t_{Df}	Delay Time to Rise		300	350	nsec	See Fig. 1

WAVEFORMS (Fig. 1)

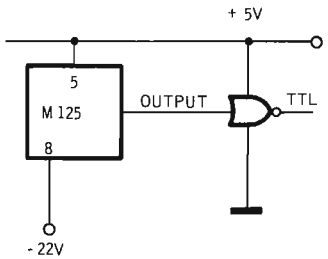


TYPICAL TIMING DIAGRAM

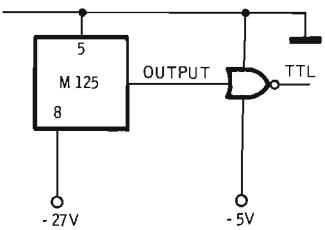


TYPICAL INTERFACE CIRCUITS

TTL DRIVE

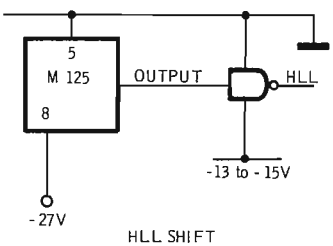


MOS SHIFT

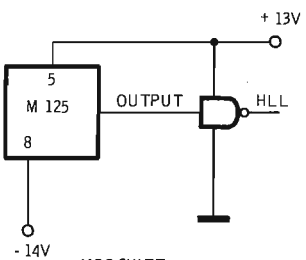


TTL SHIFT

HLL DRIVE

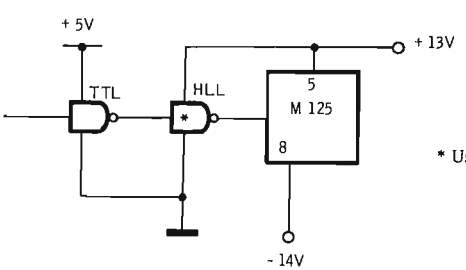


HLL SHIFT



MOS SHIFT

MOS DRIVE



* Use H114 HLL device for TTL interface

STANDARD TEMPERATURE RANGE
0°C to 70°C

Dual 100-bit static shift register

- INPUT GATE PROTECTION
- TTL DRIVE CAPABILITY
- HIGH SPEED (1 MHz)
- STATIC OPERATION

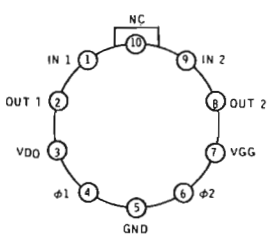
The M 127 consists of two separate 100-bit static shift registers with independent input and output terminals, and common clocks, power, and ground. Two power supplies and two external clocks are required for operation with a third clock generated internally. The entire device is constructed on a single monolithic chip using MOS P-channel technology. Transferring data into the register is accomplished when the Φ 1 clock is at a logical 1. Shifting the data occurs when the Φ 1 clock is momentarily pulsed to logical 1 and the Φ 2 clock to logical 0. For long term data storage, the Φ 1 clock must be held at logical 0 and Φ 2 clock must be held at logic "1". Output data appears on the negative-going edge of the Φ 2 clock pulse. Output low impedance allows direct drive of TTL gates.

ORDERING NUMBER
M 127 T1

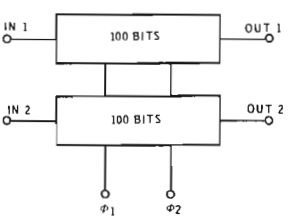
ABSOLUTE MAXIMUM RATINGS

Input Voltage	-30V to 0.3V
Clock Voltage	-30V to 0.3V
Supply Voltage	-30V to 0.3V
Storage Temperature Range	-55°C to 150°C

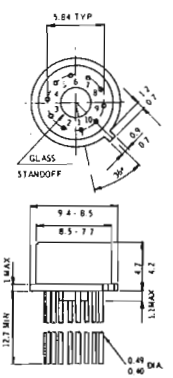
CONNECTION DIAGRAM
(Top view)



LOGIC DIAGRAM



PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-100



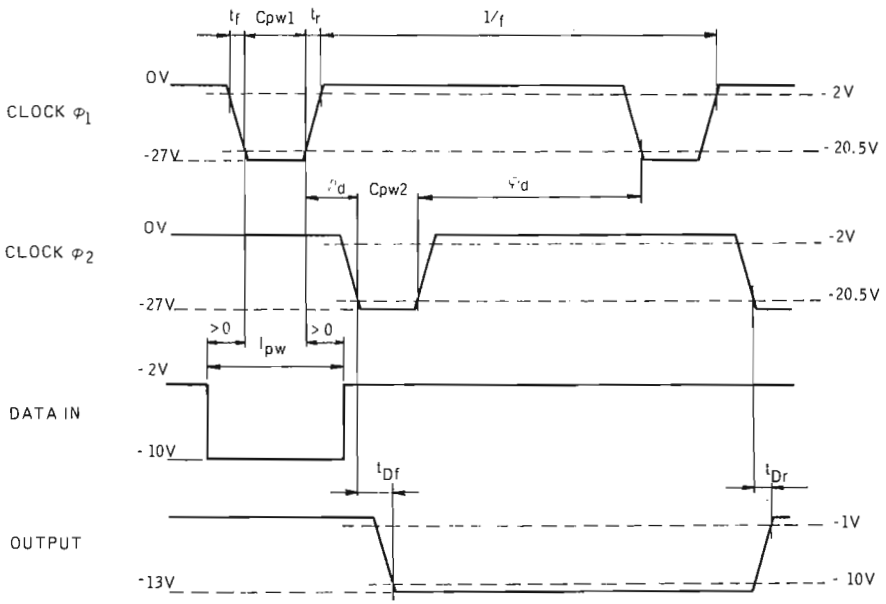
Note : all dimensions in mm.

ELECTRICAL CHARACTERISTICS :

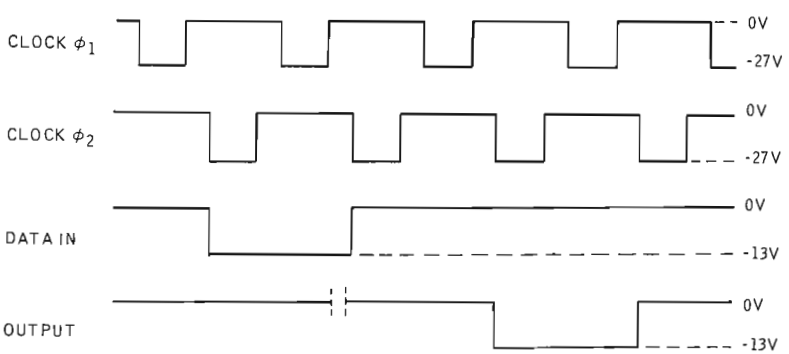
(T_A = 0°C to 70°C; V_{DD} = -13V ± 1V; V_{GG} = -27V ± 1V; Load = 10MΩ and 10pF unless otherwise noted)

SYMBOL	CHARACTERISTIC	Min.	Typ.	Max.	Unit	TEST CONDITIONS
	CLOCK PULSES					
f	Repetition Rate Range	0		1	MHz	
C_{pw1}	Pulse Width Ø 1	0.4		10	µsec	T_A = 25°C see waveforms
C_{pw2}	Pulse Width Ø 2	0.4			µsec	
Ø d	Pulse Separation	0.01		10	µsec	
t_r , tf	Rise and Fall Time			5	µsec	
V_{ILcp}	"0" Level Voltage			-2	V	
V_{IHcp}	"1" Level Voltage	- 26			V	
I_{Lcp}	Leakage Current			-50	µA	V = -28V
C_{cp}	Input Capacitance		28	33	pF	V = 0 T_A= 25°C f=1MHz
	DATA INPUT					
V_{IL}	"0" Level Voltage			- 2	V	
V_{IH}	"1" Level Voltage	- 9			V	
V_{Ipw}	Pulse Width	0.4			µsec	see waveforms
I_L	Leakage Current			- 1	µA	V = - 20V
C_{in}	Input Capacitance		3	5	pF	V=0 T_A=25°C f=1MHz
	DATA OUTPUT					
V_{OL}	"0" Level Voltage		-0.3	- 1	V	
V_{OL1}	"0" Level Voltage		-1	- 2	V	I_{OL1} = - 60µA
V_{OH}	"1" Level Voltage	- 10	-12		V	
V_{OH1}	"1" Level Voltage		-10.5		V	I_{OH} = 400 µA
V_{OH2}	"1" Level Voltage	-4.8			V	I_{OH} = 1.6 mA
	RESPONSE TIME					
t_{Dr}	Delay Time to Rise		300	400	nsec	T_A = 25°C see waveforms
t_{Df}	Delay Time to Fall		300	400	nsec	
	POWER CONSUMPTION					
I_{DD}	Drain Current		-18	-25	mA	V_{DD}=-14V V_{GG}=-28V
I_{GG}	Gate Current		-1.5	-2.9	mA	V_{DD}=-14V V_{GG}=-28V

WAVEFORMS

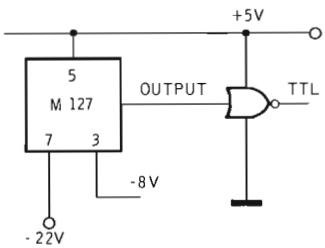


TYPICAL TIMING DIAGRAM

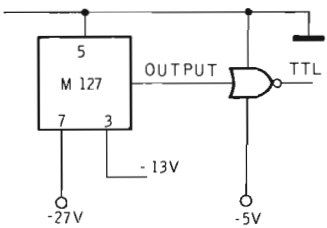


TYPICAL INTERFACE CIRCUITS

TTL DRIVE

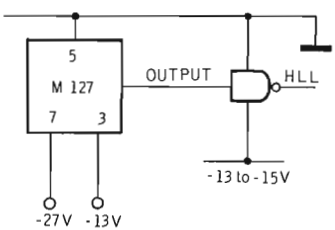


MOS SHIFT

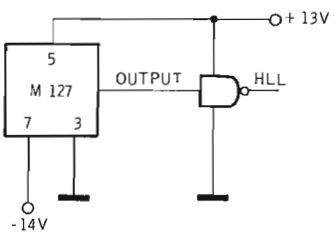


TTL SHIFT

HLL DRIVE

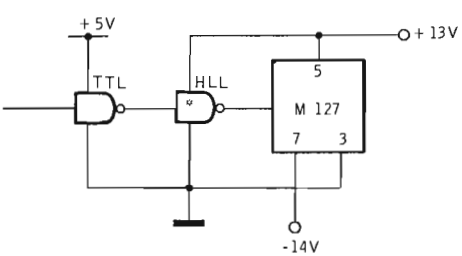


HLL SHIFT



MOS SHIFT

MOS DRIVE



* Use H 114 HLL device for TTL interface

MOS INTEGRATED CIRCUIT

M 130

1024 - BIT DYNAMIC SHIFT REGISTER

- LOW POWER DISSIPATION : 60 μW/BIT at 1 MHz
- HIGH FREQUENCY OPERATION : 10 MHz
- DTL-TTL COMPATIBLE
- INPUTS GATE PROTECTION

The M 130 is a 1024-bit dynamic shift register using low threshold silicon gate technology, which allows high speed (5 MHz guaranteed) while reducing power dissipation compared to conventional technologies. The registers can be driven directly by standard integrated circuits (TTL, DTL. etc.) or by MOS circuits. The circuit design makes the M 130 very popular in applications such as low cost memory and delay line.
The device is available in 8-lead metal case package similar to Jedec TO-99.

ABSOLUTE MAXIMUM RATINGS

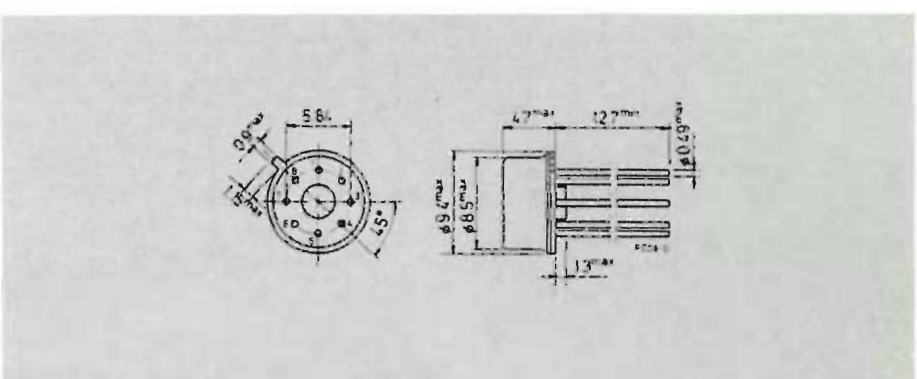
V_I*	Input voltage	-20 to 0.3	V
$V\phi$*	Clock voltage	-20 to 0.3	V
V_{DD}*	Drain supply voltage	-20 to 0.3	V
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	0 to 70	°C

* This voltage is with respect to V_{SS} pin voltage

ORDERING NUMBER : M 130 T1

MECHANICAL DATA

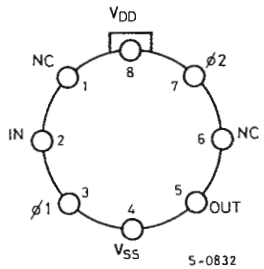
Dimensions in mm



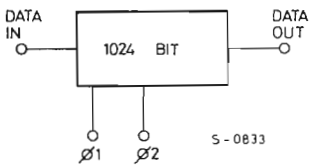
M 130

CONNECTION DIAGRAM

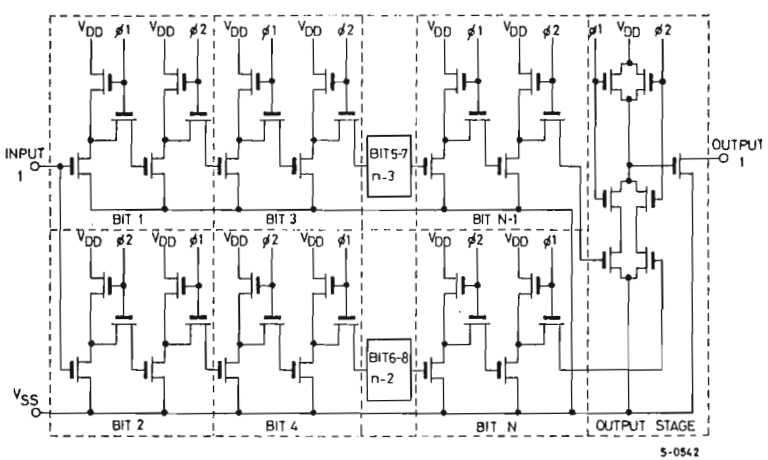
(top view)



LOGIC DIAGRAM



SCHEMATIC DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS (V_{SS} = 4.75 to 5.25V, V_{DD}= -4.75 to -5.25V, T_{amb}= 0 to 70°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
CLOCK PULSES						
$V_{\phi H}$	Clock high voltage		V_{SS}-1		V_{SS}	V
$V_{\phi L}$	Clock low voltage		V_{SS}-17		V_{SS}-15	V
$I_{L\phi}$	Clock leakage current	$V_{\phi L}$=V_{SS}-14V* T_{amb}=25°C		0.1	1	μA
DATA INPUT						
V_{IH}	Input high voltage		V_{SS}-1.7		V_{SS}	V
V_{IL}	Input low voltage		V_{SS}-10		V_{SS}-4.2	V
I_{LI}	Input leakage current	V_I =V_{SS}-14V* T_{amb}=25°C		0.01	500	nA
DATA OUTPUT						
V_{OH1}	Output high voltage driving MOS	R_L=4.7kΩ±5% C_L = 10 pF	V_{SS}-1.6			V
V_{OH2}	Output high voltage driving TTL	R_L=3kΩ ± 5% I_{OH}= 100μA	2.4			V
V_{OL}	Output low voltage	R_L=3kΩ ± 5% I_{OL}=1.6mA			0.5	V
I_{LO}	Output leakage current	V_o =V_{SS}-10V T_{amb}= 25°C V_{DD} =V_{SS} V_ϕ =V_{SS}-15V		0.01	1000	nA
POWER CONSUMPTION						
I_{DD}	Drain supply current	Output at logic "0" Duty cycle = 35%** Data rate = 25kHz R_L = 3kΩ $V_{\phi L}$= V_{SS} -14V T_{amb} = 25°C		25	35	mA

* All unspecified pins are tied to V_{SS}

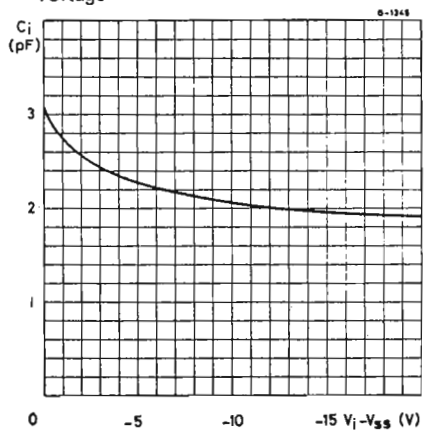
** The cycle is understood as measured half way between high and low level

DYNAMIC ELECTRICAL CHARACTERISTICS (V_{SS} = 4.75 to 5.25V, V_{DD} = -4.75 to -5.25V, load = 1 TTL gate, T_{amb} = 0 to 70°C, unless otherwise specified)

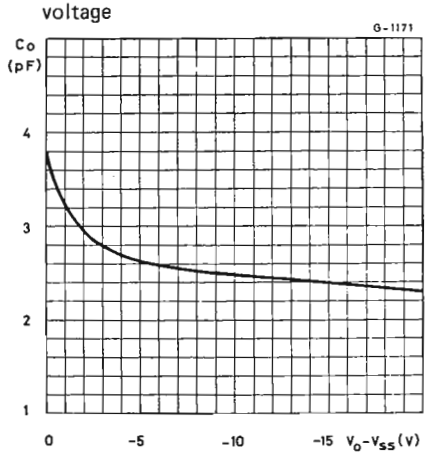
Parameter		Test conditions	Min.	Typ.	Max.	Unit
$t_{\phi pw}$	Clock pulse width	See timing diagram	150	90		ns
$t_{\phi d}$	Clock pulse delay		10			ns
t_r, t_f	Clock rise and fall time				1000	ns
f_{min}	Min. input date rate	$t_{\phi pw}$ = 130 ns R_L = 3kΩ T_{amb} = 25°C		100		Hz
f_{max}	Max. input data rate	$t_{\phi pw}$ = 50ns R_L = 3kΩ	5	10		MHz
t_{Dr}, t_{Df}	Delay time to rise and to fall			60	80	ns
t_s	Set-up time		70	50		ns
t_h	Input hold time		20			ns
C_ϕ*	Clock capacitance	$V_\phi = V_{SS}$ at 1 MHz		140		pF
$C_{\phi\phi}$*	Clock to clock capacitance			6.5		pF
C_i*	Input capacitance	$V_i = V_{SS}$ at 1 MHz		3		pF
C_o*	Output capacitance	$V_o = V_{SS}$ at 1 MHz		3	4	pF

*This parameter is periodically sampled and is not 100% tested

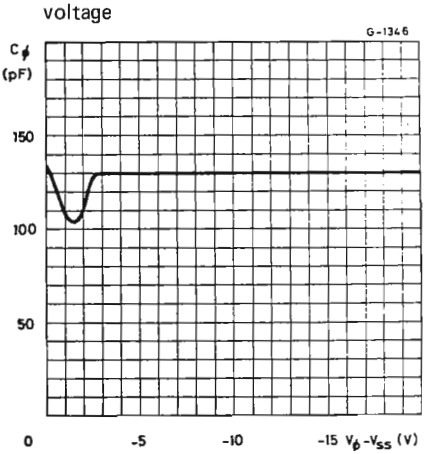
Typical input capacitance vs. input voltage



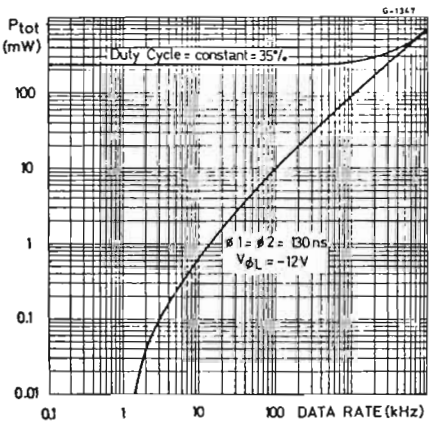
Typical output capacitance vs. output voltage

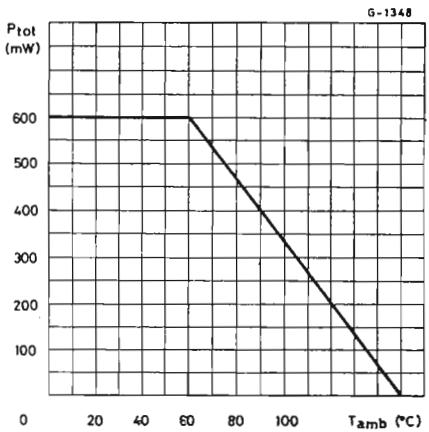


Typical clock capacitance vs. clock voltage



Power dissipation vs. data rate

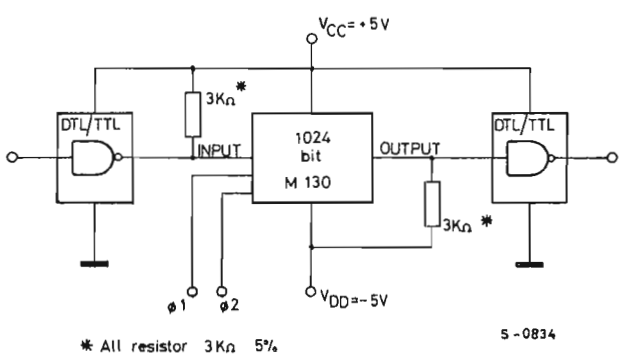




Maximum power dissipation vs. ambient temperature

SWITCHING TIMES

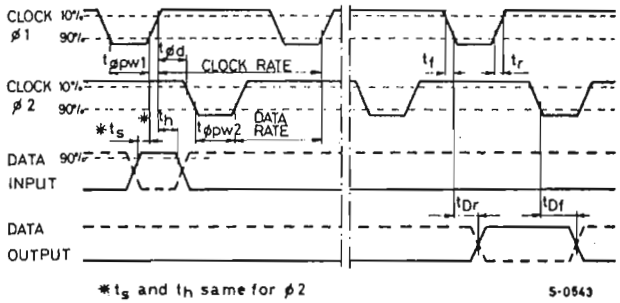
DTL-TTL - MOS interface



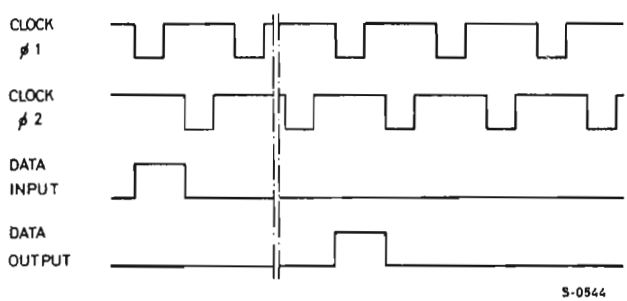
* All resistor 3KΩ 5%

SWITCHING TIMES (continued)

Waveforms



Timing diagram



DUAL 512 BIT DYNAMIC SHIFT REGISTER M 136
QUAD 256 BIT DYNAMIC SHIFT REGISTER M 141

- LOW POWER DISSIPATION : 60 μW/BIT at 1 MHz
- HIGH FREQUENCY OPERATION : 10 MHz
- DTL-TTL COMPATIBLE
- INPUTS PROTECTED AGAINST STATIC CHARGE

The **M 136** and **M 141** are dynamic shift registers using low threshold silicon gate technology, which allows high speed (5 MHz guaranteed) while reducing power dissipation compared to conventional technologies. The input of the shift registers can be driven directly by standard bipolar integrated circuits (TTL, DTL, etc.) or by MOS circuits. The design of the circuits makes the **M 136 - M 141** very popular in applications such as low cost memories and delay lines. The **M 136** is available in 8-lead metal case, while the **M 141** is available in 16- lead dual in-line ceramic package.

ABSOLUTE MAXIMUM RATINGS

V_i*	Input voltage	-20 to 0.3	V
V_ϕ*	Clock voltage	-20 to 0.3	V
V_{DD}*	Drain supply voltage	-20 to 0.3	V
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	0 to 70	°C

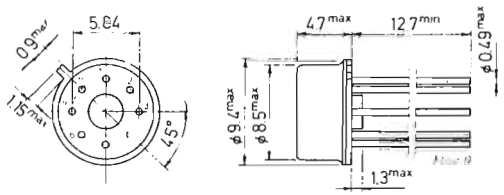
* This voltage is with respect to V_{SS} pin voltage

ORDERING NUMBERS: M 136 T1
M 141 D1

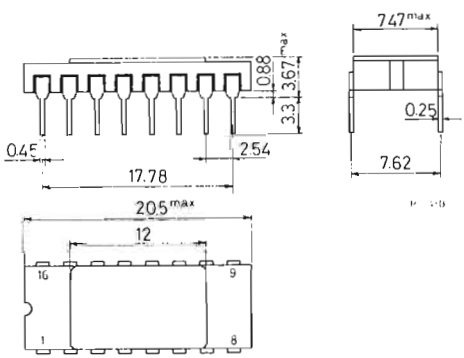
M 136
M 141

MECHANICAL DATA (dimensions in mm)

for **M 136** type

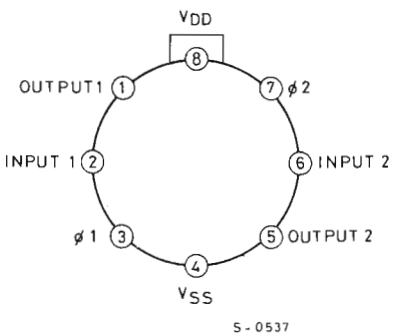


for **M 141** type



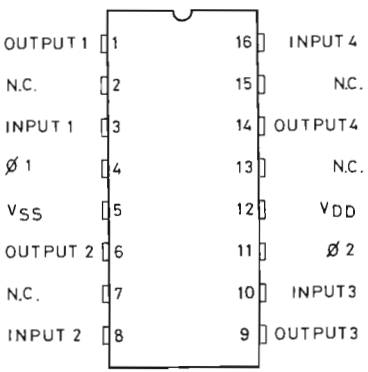
CONNECTION DIAGRAMS (top view)

for M 136 type



S-0537

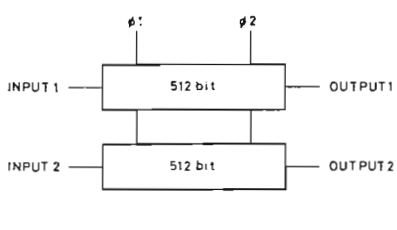
for M 141 type



S-0536

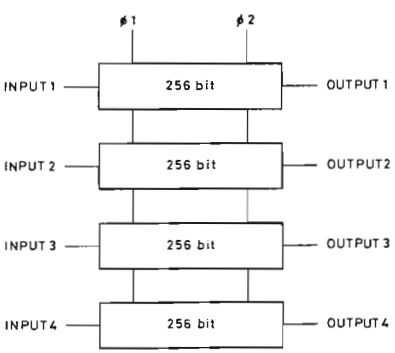
LOGIC DIAGRAMS

for M 136 type



S-0539

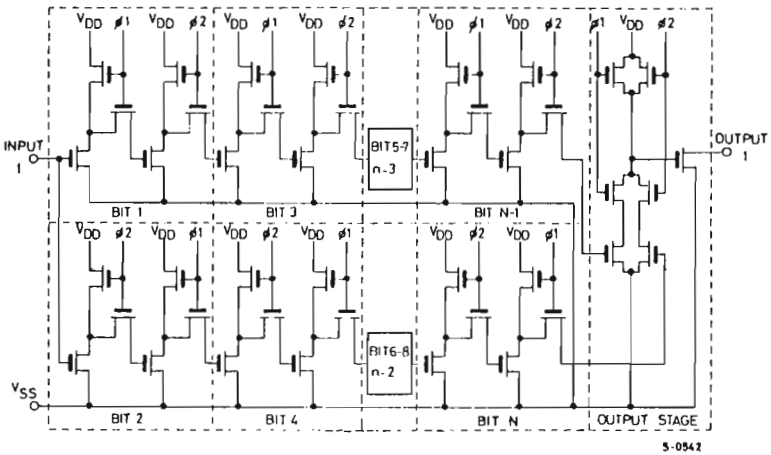
for M 141 type



S-538

M 136
M 141

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS (V_{SS} = 4.75 to 5.25 V, V_{DD} = - 4.75 to - 5.25 V, T_{amb} = 0 to 70°C unless otherwise specified)

	Parameter		Test conditions	Min.	Typ.	Max.	Unit
	CLOCK PULSES						
→	$V_{\phi H}$	Clock high voltage		V_{SS}-1		V_{SS}	V
	$V_{\phi L}$	Clock low voltage		V_{SS}-17		V_{SS}-15	V
→	$I_{L\phi}$	Clock leakage current	$V_{\phi L}$=V_{SS} -14V* T_{amb}=25°C		0.1	1	μA
	DATA INPUT						
→	V_{IH}	Input high voltage		V_{SS}-1.7		V_{SS}	V
	V_{IL}	Input low voltage		V_{SS}-10		V_{SS}-4.2	V
→	I_{LI}	Input leakage current	V_i =V_{SS} -14V* T_{amb} = 25°C		0.01	500	nA

ELECTRICAL CHARACTERISTICS (continued)

	Parameter		Test conditions	Min.	Typ.	Max.	Unit
	DATA OUTPUT						
→	V_{OH1}	Output high voltage driving MOS	R_L =4.7kΩ±5% C_L = 10 pF	V_{SS}-1.6			V
→	V_{OH2}	Output high voltage driving TTL	R_L =3kΩ±5% I_{OH} = 100 μA	2.4			V
→	V_{OL}	Output low voltage	R_L =3kΩ±5% I_{OL} = 1.6mA			0.5	V
	I_{LO}	Output leakage current	V_o=V_{SS}-10V T_{amb}= 25°C V_{DD}=V_{SS} V_ϕ=V_{SS}-15V		0.01	1000	nA
	POWER CONSUMPTION						
→	I_{DD}	Drain supply current	Output at logic "0" Duty cycle = 35%** Data rate = 25 kHz R_L = 3kΩ $V_{\phi L}$=V_{SS}-14V T_{amb} = 25°C		25	35	mA

* All unspecified pins are tied to V_{SS}

** The cycle is understood as measured half way between high and low level

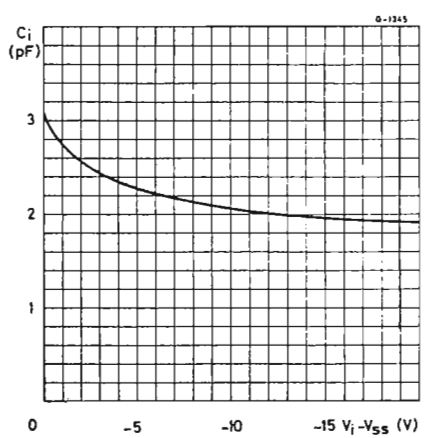
SWITCHING CHARACTERISTICS (V_{SS} = 4.75 to 5.25V, V_{DD} = -4.75 to -5.25V load = 1 TTL gate, T_{amb} = 0 to 70°C unless otherwise specified)

	Parameter		Test conditions	Min.	Typ.	Max.	Unit
→	$t_{\phi pw}$	Clock pulse width	See timing diagram	150	90		ns
	$t_{\phi d}$	Clock pulse delay		10			ns
	t_r, t_f	Clock rise and fall time				1000	ns

SWITCHING CHARACTERISTICS (continued)

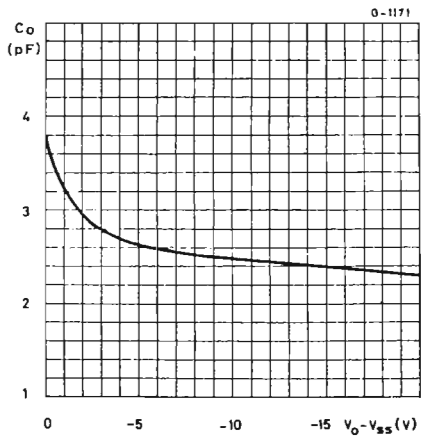
	Parameter		Test conditions	Min.	Typ.	Max.	Unit
→	f_{min}	Min. input data rate	$t\phi_{pw}$ = 130 ns R_L = 3 kΩ T_{amb} = 25°C		100		Hz
→	f_{max}	Max. input data rate	R_L = 3 kΩ $t\phi_{pw}$ = 50 ns	5	10		MHz
→	t_{Dr}, t_{Df}	Delay time to rise and to fall			60	80	ns
→	t_s	Set-up time		70	50		ns
	t_h	Input hold time		20			ns
→	$C\phi$*	Clock capacitance	$V\phi = V_{SS}$ at 1 MHz		140		pF
	$C\phi\phi$*	Clock to clock capacitance			6.5		pF
→	C_i*	Input capacitance	$V_i = V_{SS}$ at 1 MHz		3		pF
	C_o*	Output capacitance	$V_o = V_{SS}$ at 1 MHz		3	4	pF

* This parameter is periodically sampled and is not 100% tested

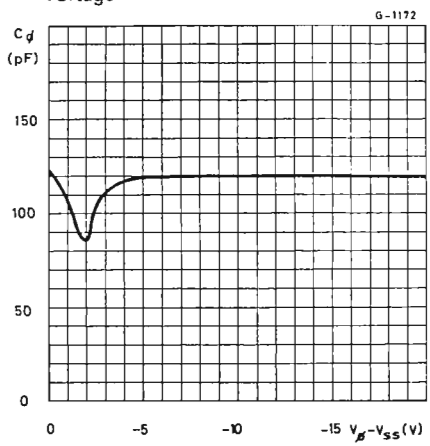


Typical input capacitance vs. input voltage

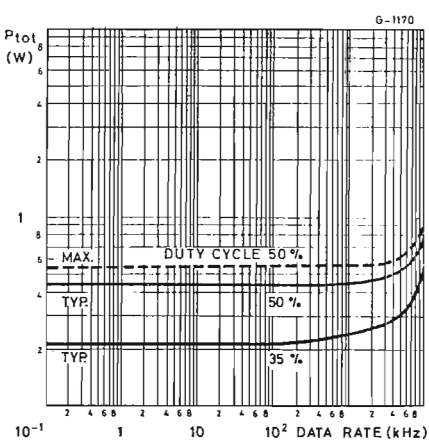
Typical output capacitance vs. output voltage



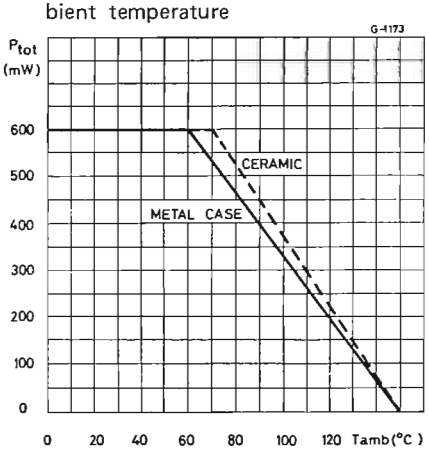
Typical clock capacitance vs. clock voltage



Power dissipation vs. data rate

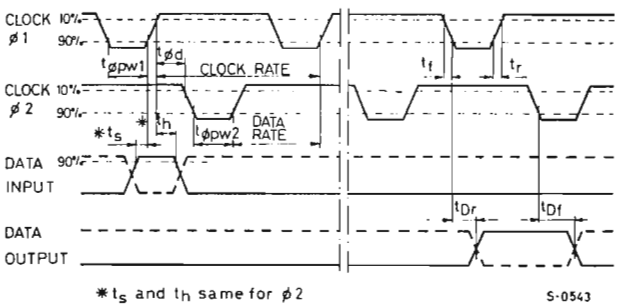


Maximum power dissipation vs. ambient temperature

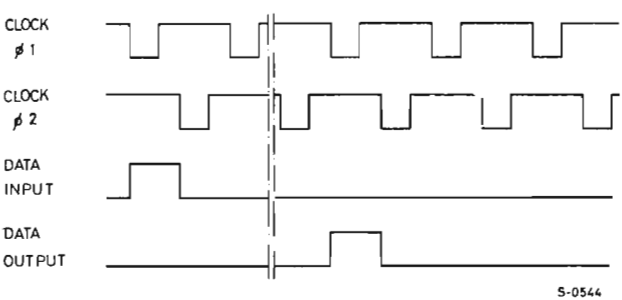


SWITCHING TIMES

Waveforms



Timing diagram



Dual 64-bit fully DC shift register

EXTENDED TEMPERATURE RANGE
-55°C to 125°C
STANDARD TEMPERATURE RANGE
0°C to 70°C

- FULLY TTL COMPATIBLE
- DC TO 2MHz OPERATION
- SINGLE PHASE CLOCK
- INPUT GATE PROTECTION

The M 137 consists of 2 separate 64-bit shift registers with independent input and output terminals and common single phase clock. Data inputs and clock can be driven directly from DTL/TTL levels and the outputs can drive DTL/TTL directly. The entire device is constructed on a single monolithic chip utilizing nitride-Planox technology. Transferring data into the register is accomplished while the clock is low and output data appears on the positive going edge of the clock.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

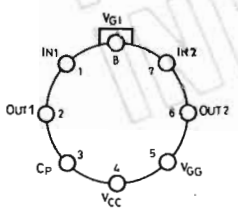
Input Voltage (1)	-20 to + 0.3V
Clock Voltage (1)	-20 to + 0.3V
Supply Voltage (1)	-20 to + 0.3V
Storage Temperature Range	-65°C to 150°C

ORDERING NUMBER

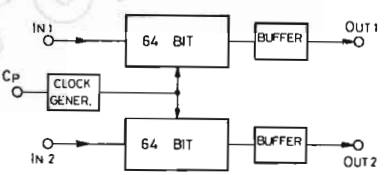
M 137 T1 (for Standard Temperature Range)
M 137 T2 (for Extended Temperature Range)

Note 1 With respect to V_{CC}

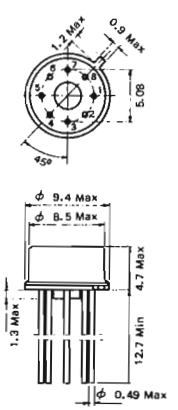
CONNECTION DIAGRAM
(top view)



LOGIC DIAGRAM



PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-99 outline

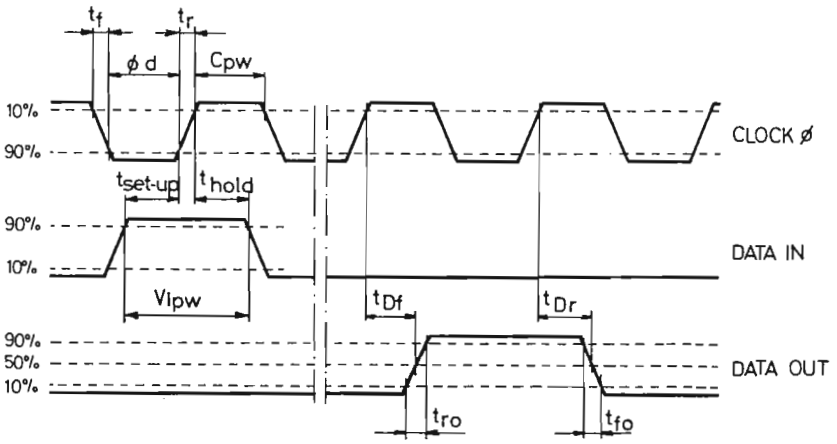


Note: all dimensions in mm.

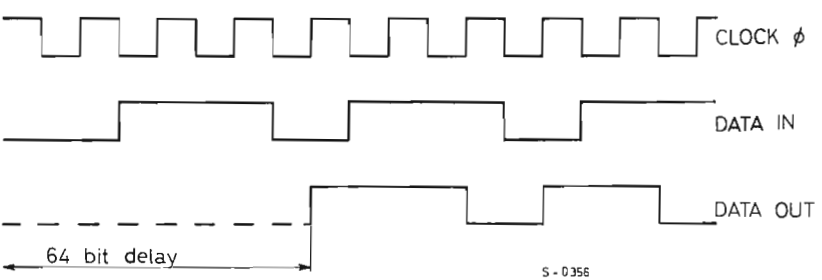
ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 0.5V; V_{GI} = GND; V_{GG} = -12V ± 1V; unless otherwise noted)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
	CLOCK PULSES					
f	Repetition Rate Range	0		2	MHz	
C_{pw}	Pulse Width	200			ns	
ϕd	Pulse Separation	200			ns	
t_r, t_f	Rise and Fall Time			1	μs	f = 100 kHz
V_{ILcp}	"0" Level Voltage			V_{CC}-4.2	V	
V_{IHcp}	"1" Level Voltage	V_{CC}-1.5			V	
I_{Lcp}	Leakage Current			1	μA	$V_{cp}=V_{CC}$ - 15V T_A = 25°C
C_{cp}	Input Capacitance			15	pF	$V_{cp}=V_{CC}$ f = 1 MHz
	DATA INPUT					
V_{IL}	"0" Level Voltage			V_{CC}-4.2	V	
V_{IH}	"1" Level Voltage	V_{CC}-1.5			V	
V_{Ipw}	Pulse Width	250			ns	T_A = 25°C f = 2 MHz
I_L	Leakage Current			1	μA	$V_{in}=V_{CC}$-15V T_A = 25°C
C_{in}	Input Capacitance			5	pF	$V_{in}=V_{CC}$ T_A=25°C f=1MHz
t_{set-up}	Set-up Time		100		ns	see waveforms
t_{hold}	Hold Time		150		ns	see waveforms
	DATA OUTPUT					
V_{OL}	"0" Level Voltage			0.4	V	load = 10 pF I_{sink} = 1.6 mA
V_{OH}	"1" Level Voltage	V_{CC} - 1			V	I_{OH} = 100 μA
t_{ro}	Rise Time		60		ns	T_A = 25°C see waveforms
t_{fo}	Fall Time		90		ns	T_A = 25°C see waveforms
	SWITCHING TIME					
t_{Dr}	Delay Time to Rise		300		ns	T_A = 25°C see waveforms
t_{Df}	Delay Time to Fall		300		ns	T_A = 25°C see waveforms
	POWER CONSUMPTION					
I_{GG}	Gate Supply Current		13		mA	
P_D	Total Power Consumption		220		mW	nominal power supply

WAVEFORMS

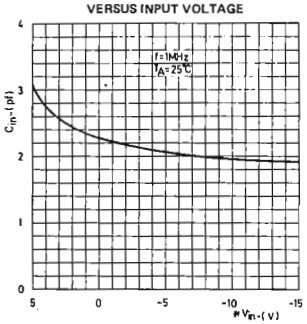


TYPICAL TIMING DIAGRAM

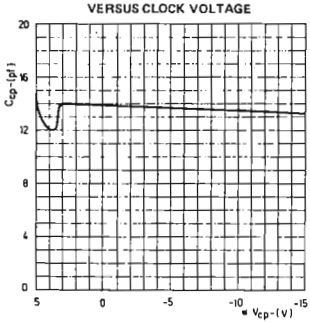


TYPICAL ELECTRICAL CHARACTERISTICS

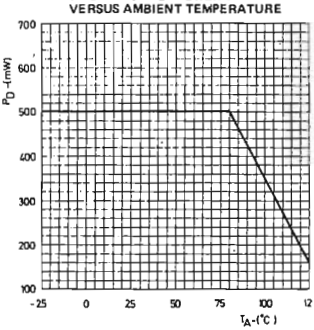
INPUT CAPACITANCE VERSUS INPUT VOLTAGE



CLOCK CAPACITANCE VERSUS CLOCK VOLTAGE

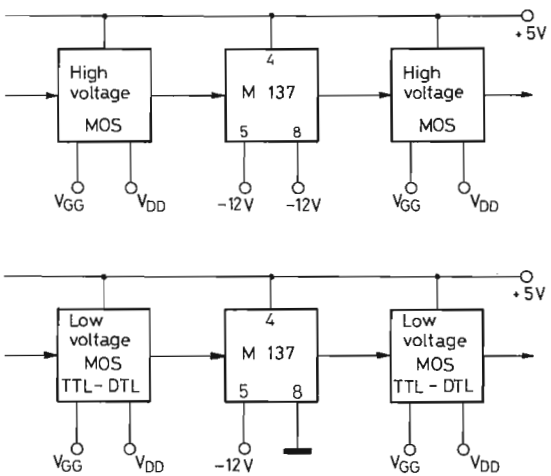


MAXIMUM PACKAGE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



* Note : These voltages are with respect to V_{CC} pin voltage

TYPICAL INTERFACE CIRCUITS



Dual 32-bit fully DC shift register

EXTENDED TEMPERATURE RANGE
-55°C to 125°C
STANDARD TEMPERATURE RANGE
0°C to 70°C

- FULLY TTL COMPATIBLE
- DC TO 2 MHz OPERATION
- SINGLE PHASE CLOCK
- INPUT GATE PROTECTION
- INPUT SELECT

The M 140 is a dual 32-bit fully DC shift register constructed on a single chip using silicon nitride-Planox, P-channel technology. The M 140 requires only a single phase and may be operated till 2 MHz over the temperature range -55°C to 125°C. The device contains two separate 32-bit registers utilizing common power and clock line and having low impedance output buffers capable of sinking TTL/DTL load current without using external components. The patented Planox technology minimizes the parasitic capacitances for higher speed operation and provides the best reliability.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

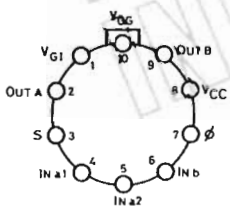
Input Voltage (1)	-20 V to 0.3 V
Clock Voltage (1)	-20 V to 0.3 V
Supply Voltage (1)	-20 V to 0.3 V
Storage Temperature Range	-65°C to 150°C

(1) This voltage is with respect to the V_{CC} pin voltage.

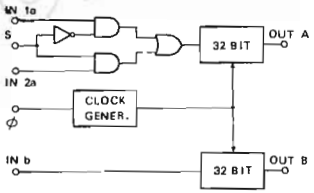
ORDERING NUMBER

M 140 T1 (for standard temperature range)
M 140 T2 (for extended temperature range)

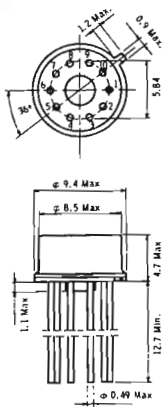
CONNECTION DIAGRAM
(top view)



LOGIC DIAGRAM



PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-100

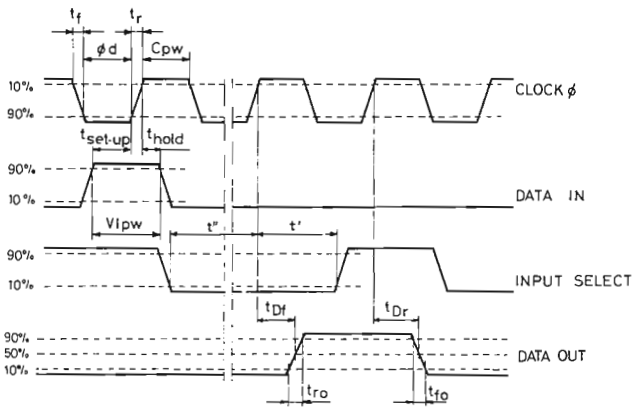


Note : all dimensions in mm.

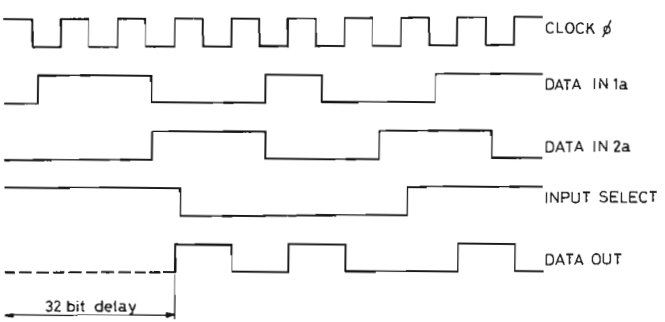
ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 0.5V; V_{GI} = GND; V_{GG} = -12V ± 1V; unless otherwise noted)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
	CLOCK PULSES					
f	Repetition Rate Range	0		2	MHz	
C_{pw}	Pulse Width	200			ns	
ϕd	Pulse Separation	200			ns	
t_r,t_f	Rise and Fall Time			1	μs	f = 100 kHz
V_{ILcp}	"0" Level Voltage			V_{CC}-4.2	V	
V_{IHcp}	"1" Level Voltage	V_{CC}-1.5			V	
I_{Lcp}	Leakage Current			1	μA	$V_{cp} = V_{CC}$ - 15V T_A = 25°C
C_{cp}	Input Capacitance			15	pF	$V_{cp} = V_{CC}$ f = 1 MHz
	DATA AND SELECT INPUTS					
V_{IL}	"0" Level Voltage			V_{CC}-4.2	V	
V_{IH}	"1" Level Voltage	V_{CC}-1.5			V	
V_{Ipw}	Pulse Width	250			ns	T_A = 25°C f = 2 MHz
I_L	Leakage Current			1	μA	$V_{in} = V_{CC}$ - 15V T_A = 25°C
C_{in},C_s	Input and Select Capacitance			5	pF	$V_{in} = V_{CC}$ T_A = 25°C f = 1 MHz
t_{set-up}	Set-up Time		100		ns	see waveforms
t_{hold}	Hold Time		150		ns	see waveforms
t"	Select Set-up Time		100		ns	} f = 1 MHz d.c. ϕ = 50%
t'	Select Hold Time		10		ns	} see waveforms
	DATA OUTPUTS					
V_{OL}	"0" Level Voltage			0.4	V	load = 10 pF Isink=1.6mA
V_{OH}	"1" Level Voltage	V_{CC} - 1			V	I_{OH} = 100 μA
t_{ro}	Rise Time		60		ns	T_A = 25°C see waveforms
t_{fo}	Fall Time		90		ns	T_A = 25°C see waveforms
	SWITCHING TIME					
t_{Dr}	Delay Time to Rise		150		ns	T_A = 25°C see waveforms
t_{Df}	Delay Time to Fall		100		ns	T_A = 25°C see waveforms
	POWER CONSUMPTION					
I_{GG}	Gate Supply Current		6		mA	
P_D	Total Power Consumption		100		mW	nominal power supply

WAVEFORMS

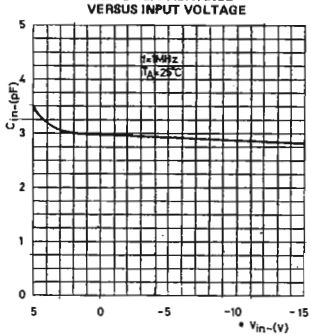


TIMING DIAGRAM

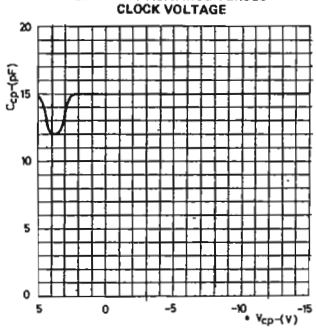


TYPICAL ELECTRICAL CHARACTERISTICS

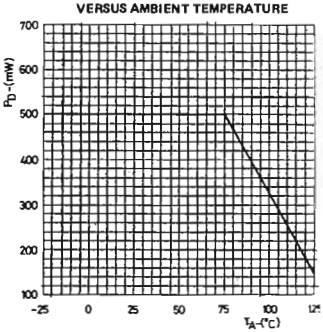
INPUT CAPACITANCE VERSUS INPUT VOLTAGE



CLOCK CAPACITANCE VERSUS CLOCK VOLTAGE



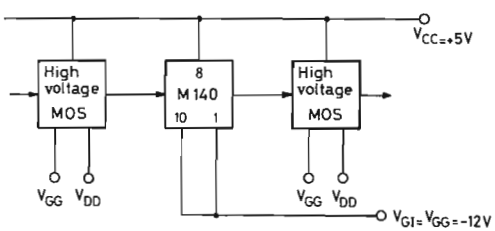
MAXIMUM PACKAGE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



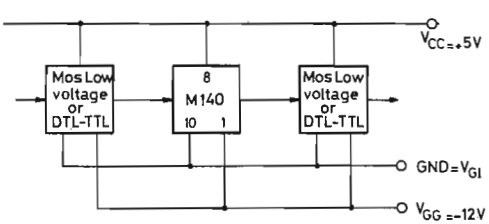
* These voltages are with respect to the V_{CC} pin voltage.

TYPICAL INTERFACE CIRCUITS

MOS OPERATION (one supply voltage)



MOS AND TTL OPERATION



1024-bit static read only memory

STANDARD TEMPERATURE RANGE,
0°C to 70°C

- INPUT GATE PROTECTION
- LOW POWER 150 mW
- CHIP SELECT INPUT
- DIRECT DRIVE OF DTL AND TTL FAMILY

The M 200 is a monolithic integrated circuit constructed on a single silicon chip by means of the P-channel MOS process. It is organized as an array of 128 words of 8 bits each and is ideally suited for code conversion, random logic synthesis, table look-up and character generation. Programming of the content is accomplished by changes in one mask during the device fabrication. Output buffers allow direct TTL interface and, in conjunction with "chip select" (CS) input, many M 200's could be used together to expand either the number of words or the number of bits per word.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Input Voltage	-30 V to 0.3V
Supply Voltage	-30 V to 0.3V
Storage Temperature	-55°C to 150°C

ORDERING NUMBER :

M 200 M1AA When the content is that shown on page 245
M 200 M1XX For your own content where **XX** will indicate your type.
In this case instructions given on page 246 should be followed.

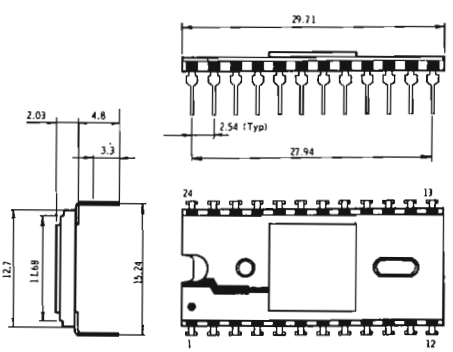
OPERATING CONDITIONS

Drain Supply Voltage (V_{DD})	-13V ± 1V
Output Buffer Supply Voltage (V_{CC})	-12V to -28V
Gate Supply Voltage (V_{GG})	-27V ± 1V

PIN CONNECTION

FUNCTION	PIN No.	FUNCTION	PIN No.
V_{DD}	1	V_{CC} Buffer Supply	13
V_{GG}	2	Output 8	14
NC	3	Output 7	15
NC	4	Output 6	16
NC	5	Output 5	17
NC	6	Output 4	18
Address 1	7	Output 3	19
Address 2	8	Output 2	20
Address 3	9	Output 1	21
Address 4	10	Address 7	22
Address 5	11	Address 6	23
Ground	12	Chip Select	24

PHYSICAL DIMENSIONS
24 pin ceramic DIP



Note : All dimensions in mm.

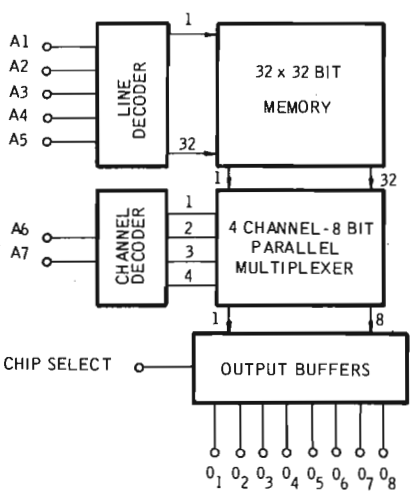
STANDARD TEMPERATURE RANGE

ELECTRICAL CHARACTERISTICS

(T_A = 0°C to 70°C unless otherwise noted; V_{DD} = -13V ± 1V; V_{CC} = -27V ± 1V; V_{CC} = -13V ± 1V; Load = 10M Ω and 10 pF).

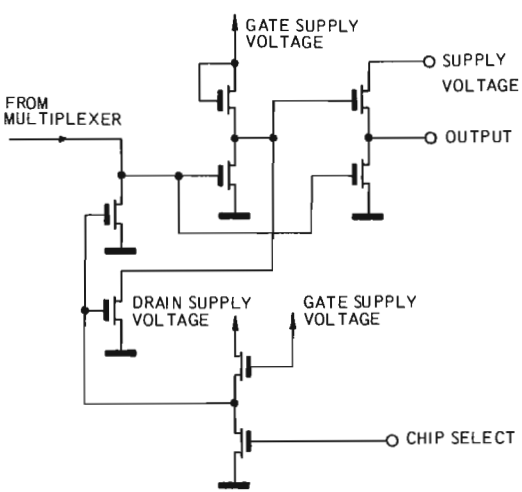
SYMBOL	CHARACTERISTICS	Min.	Typ.	Max.	Unit	TEST CONDITIONS
	ADDRESS INPUT					
V_{IL}	"0" Level Voltage			-2	V	
V_{IH}	"1" Level Voltage	-9			V	
I_L	Leakage Current			5	μA	V_{IN} = -20V
C_{in}	Input Capacitance		7		pF	
	OUTPUTS					
V_{OL}	"0" Level Voltage		-0.5	-1	V	
V_{OL1}	"0" Level Voltage			-2	V	I_{OL1} = -60μA
V_{OH}	"1" Level Voltage	-10	-13		V	
V_{OH1}	"1" Level Voltage	- 5	- 8		V	I_{OH} = 1.6mA
V_{OH2}	"1" Level Voltage		-10		V	I_{OH} = 500 μA V_{CC} = -15V
I_L	Leakage Current			-1	μA	CS = -2V V_{OUT} = -20V
	PROPAGATION DELAY					
	Address Input to Output		2.5	4	μsec	See waveforms T_A = 25°C
	POWER CONSUMPTION					
I_{DD}	Drain Current		5		mA	
I_{GG}	Gate Current		3		mA	

BLOCK DIAGRAM

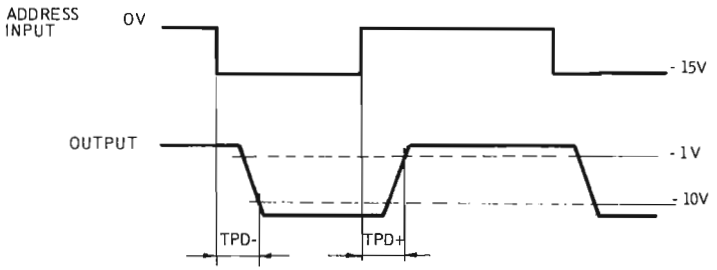


Note: When "chip select" input is "0" (-2V maw.) the outputs are floating.

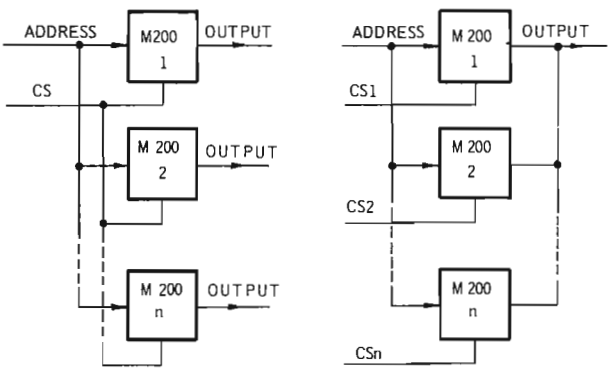
OUTPUT BUFFER CIRCUIT DIAGRAM



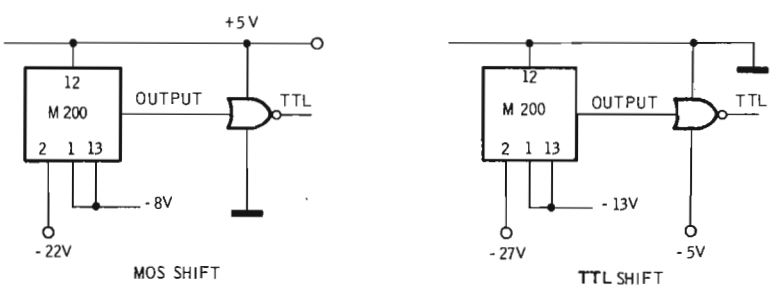
WAVEFORMS



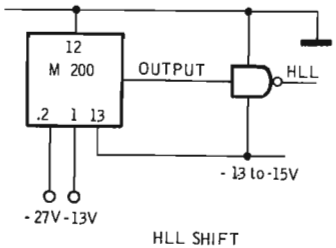
MEMORY EXPANSION



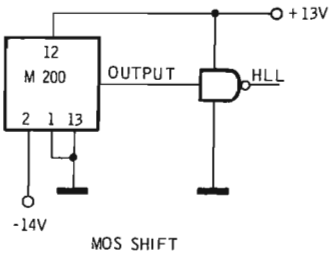
TTL DRIVE



HLL DRIVE

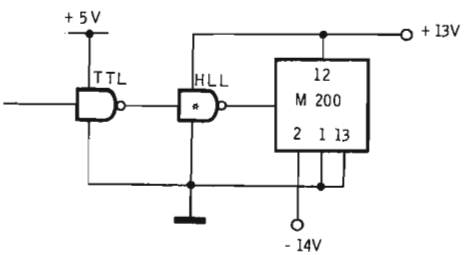


HLL SHIFT



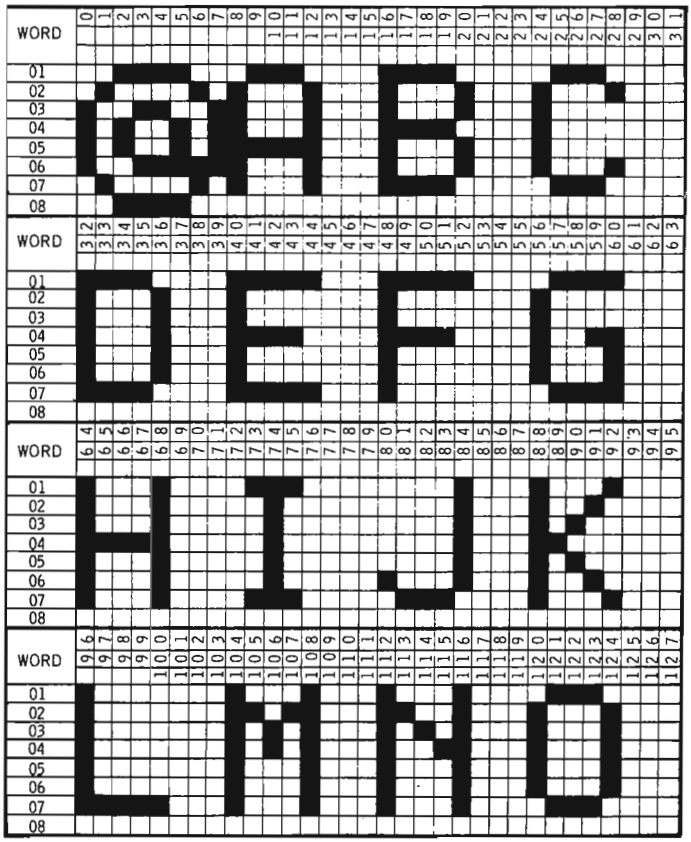
MOS SHIFT

MOS DRIVE



* Use H 114 HLL device for TTL interface

M 200 M1AA CONTENT



■ logic "1"
□ logic "0"

HOW TO HAVE A CUSTOMIZED ROM

The SGS CAD facilities are used to customize the ROM. A large computer drives a photocomposition machine to make, from your content punched cards, the test sequence, the truth table and the masks.
This unique system eliminates pattern conversion errors; upon request a computer generated truth table can be supplied for customer re-check purposes.

Punched card format

The punched cards suitable for SGS CAD are the 80 column IBM type and one card per word is needed.

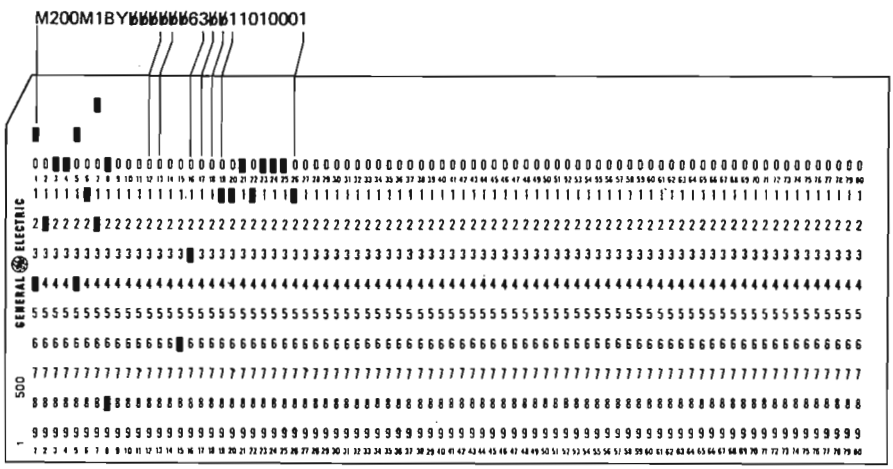
1st to 12th column - part number, alphanumeric. Each custom ROM is assigned its unique part number. First column shows the first character.

13th to 16th column - word number, numeric. First word is always called no. zero. Last column is the unity digit.

17th and 18th column - blanks ∅

19th to 26th column - word content expressed in one's and zero's. Column 19th corresponds to the output O_1, the 20th to O_2, etc. .

EXAMPLE



MOS INTEGRATED CIRCUIT

M 240

4096 BIT STATIC READ ONLY MEMORY

- WIRED OR CAPABILITY
- INPUT AMPLIFIER ELIMINATES ALL PULL-UP RESISTOR
- FULLY TTL COMPATIBLE-WITHOUT EXTERNAL COMPONENTS
- 500 ns TYPICAL ACCESS TIME
- STATIC : NO CLOCK REQUIRED

The M240 is a 4096 bit Read Only Memory constructed by means of the MOS low threshold silicon gate technology, which minimizes the parasitic capacitances for higher speed operation and provides the best reliability. The memory is arranged as 512 words of 8-bit. A 9-bit address applied at the inputs (A_0 - A_8) causes a corresponding 8-bit word to appear at the outputs (O_0 - O_7). A 4-bit programmable chip select (CS_0 - CS_3) allows one of 16 memories to be selected without need of external gating. When a chip is not selected its outputs are floating (i.e. a high impedance to both V_{SS} and V_{DD}).

ABSOLUTE MAXIMUM RATINGS

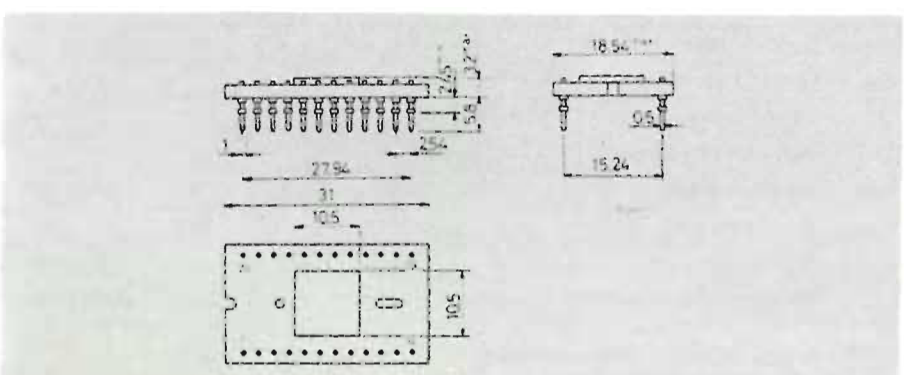
V_i *	Input voltage on any pin	-20 to 0.3	V
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	0 to 70	°C

* This voltage is with respect to the V_{SS} pin voltage

ORDERING NUMBER : M240 D1 (The device is also available in ML7 ceramic package)

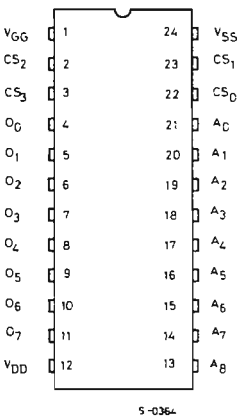
MECHANICAL DATA

Dimensions in mm

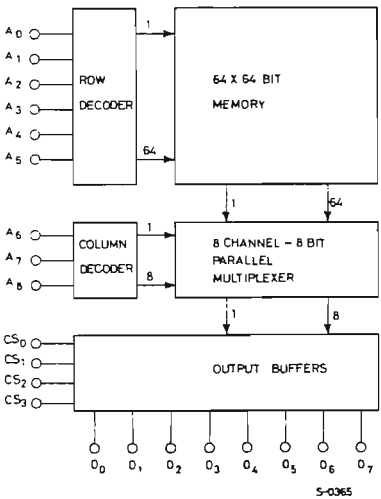


M 240

CONNECTION DIAGRAM
(top view)



BLOCK DIAGRAM



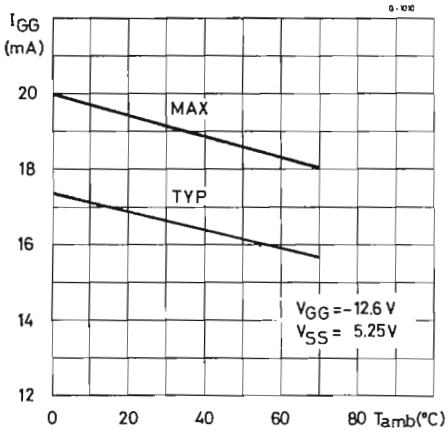
STATIC ELECTRICAL CHARACTERISTICS (V_{GG} = -11.4 to -12.6 V, V_{DD} = 0, V_{SS} = 4.75 to 5.25 V, T_{amb} = 0 to 70°C unless otherwise specified)

	Parameter		Test conditions	Min.	Typ.	Max.	Unit
→	V_{IH}	Input high voltage		V_{SS}-2.5		V_{SS}	V
	V_{IL}	Input low voltage		V_{GG}	0	0.55	V
	V_{OH}	Output high voltage	I_{OH} = 0.5 mA	2.4		V_{SS}	V
	V_{OL}*	Output low voltage	I_{OL} < 2.4 mA	0		0.4	V
	I_{LI}*	Input leakage current	$V_i = V_{SS}$ - 6V			1	µA
	I_{LO}**	Output leakage current	$V_o = V_{SS}$ - 6V			1	µA
→	I_{DD}	Supply current			16	25	mA
→	I_{GG}	Supply current			15	25	mA
→	I_{SS}	Supply current				50	mA
	P_{tot}	Total power dissipation			350	470	mW

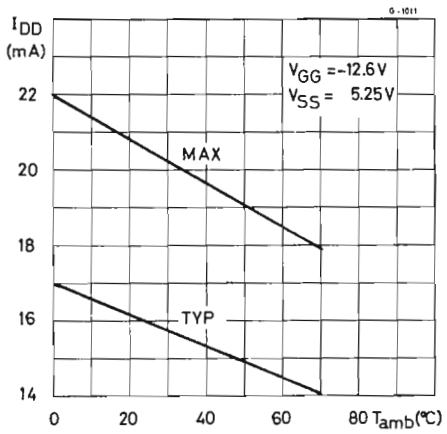
* All pins at O V except those under test

** Output floating (chip not selected)

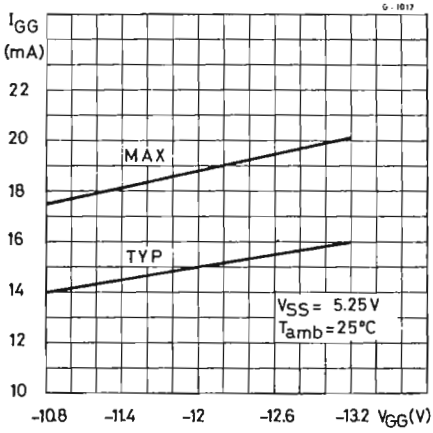
Gate current versus ambient temperature



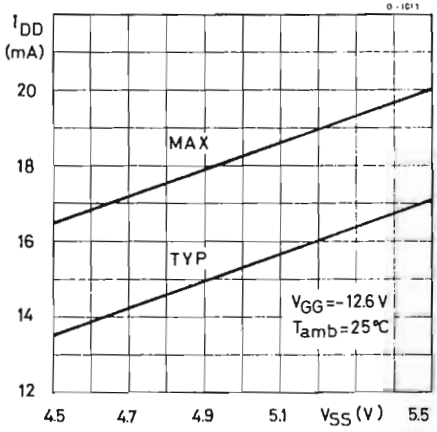
Drain current versus ambient temperature



Gate current versus supply voltage



Drain current versus substrate voltage

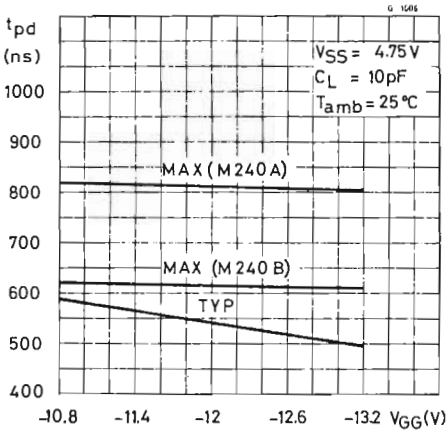


DYNAMIC ELECTRICAL CHARACTERISTICS (V_{GG}=-11.4 to 12.6V, V_{DD}= 0, V_{SS} = ± 4.75 to 5.25 V, T_{amb} = 0 to 70°C unless otherwise specified)

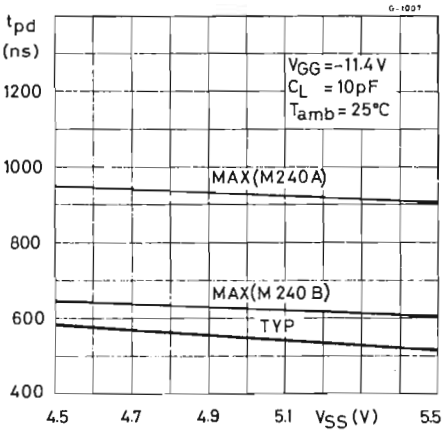
	Parameter		Test conditions (1)	Min.	Typ.	Max.	Unit
	t_{pd1}	Propagation delay time to logical "1"	1.5 TTL load				
			for **M240 A**		600	1000	ns
			for **M240 B**		500	700	ns
	t_{pd0}	Propagation delay time to logical "0"	1.5 TTL load				
			for **M240 A**		500	1000	ns
			for **M240 B**		400	700	ns
→	t_E	Enable CS propagation delay time	for **M240 A**		750	900	ns
			for **M240 B**		450	700	ns
→	t_I	Inhibit CS propagation delay time	for **M240 A**		750	900	ns
			for **M240 B**		550	700	ns
	C_i (2)	Input capacitance	$V_i = V_{SS}$ f = 1 MHz		3	5	pF
	C_o (2,3)	Output capacitance	$V_o = V_{SS}$ f = 1 MHz		7	9	pF

NOTES : 1) See waveforms and characteristic curves
2) Output floating (chip not selected)
3) Parameter guaranteed by design

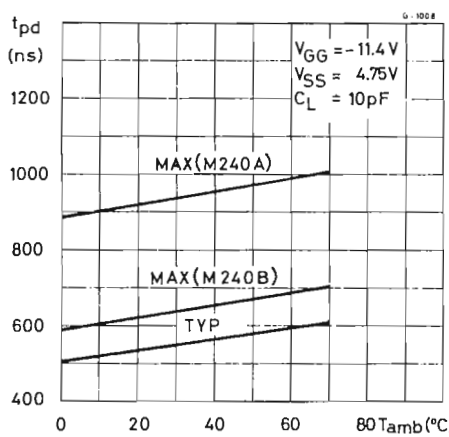
Access time versus supply voltage



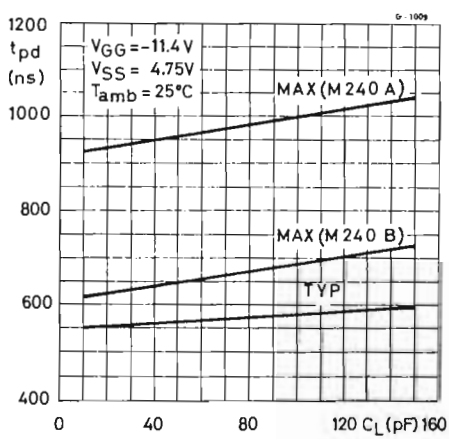
Access time versus substrate voltage



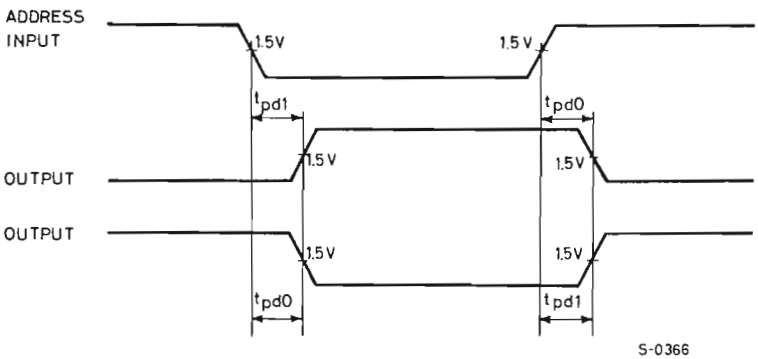
Access time versus ambient temperature

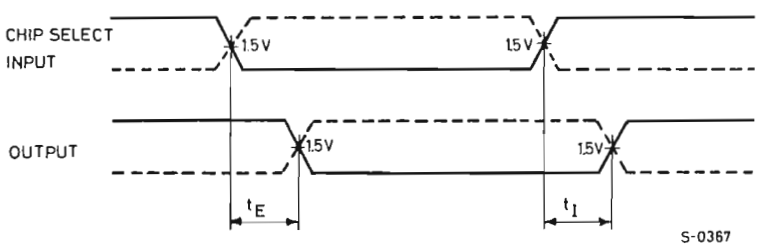


Access time versus load capacitance



WAVEFORMS


ADDRESS
INPUT
1.5V
1.5V
tpd1
tpd0
OUTPUT
1.5V
1.5V
OUTPUT
1.5V
1.5V
tpd0
tpd1
S-0366


CHIP SELECT
INPUT
1.5V
1.5V
OUTPUT
1.5V
1.5V
tE
tI
S-0367

HOW TO HAVE CUSTOMIZED ROM

The SGS-ATES facilities are used to customize the ROM. A large computer drives a photo-composition machine to make, from your content punched card, the test sequence, the truth table and the masks.

This unique system eliminates pattern conversion errors; upon request a computer generated truth table can be supplied for customer re-check purposes.

Punched card format

The punched cards suitable for SGS-ATES C.A.D. are the 80 column IBM type and one card per word is needed.

Column number	Customer information	Notes
1 to 6	Customer name	Word content expressed in alphanumerical characters.
7 to 10	Not to be used	
11 to 13	Input word number	Input word content expressed in decimal units. Column 11 MSD Column 13 LSD
14 to 20	Not to be used	
21	07 MSD	Output word content expressed in one's zero's (positive logic)
22	06	
23	05	
24	04	
25	03	
26	02	
27	01	
28	00 LSD	
29 to 80	Not to be used	

HOW TO EXPAND THE MEMORY BY MEANS OF THE CHIP SELECT

Another group of cards must be used to programme the selection up to 16 memories utilizing one card per word.

Column number	Customer information	Notes
28	CS3	Word content expressed in one's and zero's (positive logic)
29	CS2	
30	CS1	
31	CS0	

All other columns not to be used.

M 240

M240 D1 AA CONTENT (Chip select conditions: $CS_0 = 0$, $CS_1 = 1$, $CS_2 = 0$, $CS_3 = 1$)

Addr. Input	OUTPUT CODE								Addr. Input	OUTPUT CODE								Addr. Input	OUTPUT CODE								Addr. Input	OUTPUT CODE							
	07	06	05	04	03	02	01	00		07	06	05	04	03	02	01	00		07	06	05	04	03	02	01	00		07	06	05	04	03	02	01	00
0	0	0	0	0	1	0	0	0	48	0	0	1	1	1	1	0	0	96	1	1	1	1	1	1	1	1	144	0	0	1	1	1	1	0	0
1	0	0	0	0	1	0	0	0	9	0	0	0	1	1	1	0	0	7	1	1	1	1	1	1	1	1	5	0	0	1	1	1	1	0	0
2	0	0	0	0	1	0	0	0	50		0	0	1	1	1	0	0	8	1	1	1	1	1	1	1	0	6	0	0	1	1	1	1	0	0
3	0	0	0	0	1	0	0	0	1	0	0	0	1	1	1	0	0	9	1	1	1	1	1	1	1	0	7	0	0	1	1	1	1	0	0
4	0	0	0	0	1	0	0	0	2	0	0	0	1	1	1	0	0	100	1	1	1	1	1	1	1	0	8	0	0	1	1	1	1	1	0
5	0	0	0	0	1	0	0	0	3	0	0	0	1	1	1	0	0	1	1	1	1	1	1	1	1	0	9	0	0	1	1	1	1	1	0
6	0	0	0	0	1	0	0	0	4	0	0	0	1	1	1	0	0	2	1	1	1	1	1	1	1	0	150	0	1	1	1	1	1	1	0
7	0	0	0	1	1	0	0	0	5	0	0	0	1	1	1	0	0	3	0	1	1	1	1	1	1	0	1	0	1	1	1	1	1	1	0
8	0	0	0	1	1	1	0	0	6	0	0	0	1	1	1	0	0	4	0	1	1	1	1	1	1	0	2	0	1	1	1	1	1	1	0
9	0	0	0	1	1	1	0	0	7	0	0	0	0	1	0	0	0	5	0	1	1	1	1	1	1	0	3	0	1	1	1	1	1	1	0
10	0	0	0	1	1	1	0	0	8	0	0	0	0	1	0	0	0	6	0	1	1	1	1	1	0	0	4	0	1	1	1	1	1	1	0
11	0	0	0	1	1	1	0	0	9	0	0	0		1	0	0	0	7	0	1	1	1	1	1	0	0	5	1	1	1	1	1	1	1	0
12	0	0	0	1	1	1	0	0	60	0	0	0	0	1	0	0	0	8	0	1	1	1	1	1	0	0	6	1	1	1	1	1	1	1	1
13	0	0	0	1	1	1	0	0	1	0	0	0	0	1	0	0	0	9	0	1	1	1	1	1	0	0	7	1	1	1	1	1	1	1	1
14	0	0	0	1	1	1	0	0	2	0	0	0	0	1	0	0	0	110	0	1	1	1	1	1	0	0	8	1	1	1	1	1	1	1	1
15	0	0	1	1	1	1	0	0	3	0	0	0	0	1	0	0	0	1	0	0	1	1	1	1	0	0	9	1	1	1	1	1	1	1	1
16	0	0	1	1	1	1	1	0	4	0	0	0	0	0	0	0	0	2	0	0	1	1	1	1	0	0	160	1	1	1	1	1	1	1	1
17	0	0	1	1	1	1	1	0	5	0	0	0	0	1	0	0	0	3	0	0	1	1	1	1	0	0	1	1	1	1	1	1	1	1	1
18	0	0	1	1	1	1	1	0	6	0	0	0	1	0	0	0	0	4	0	0	1	1	1	1	0	0	2	1	1	1	1	1	1	1	1
19	0	0	1	1	1	1	1	0	7	0	0	0	1	0	0	0	0	5	0	0	1	1	1	1	0	0	3	1	1	1	1	1	1	1	1
20	0	0	1	1	1	1	1	0	8	0	0	0	1	0	0	0	0	6	0	0	1	1	1	1	0	0	4	1	1	1	1	1	1	1	0
21	0	0	1	1	1	1	1	0	9	0	0	0	1	0	0	0	0	7	0	0	1	1	1	1	0	0	5	0	1	1	1	1	1	1	0
22	0	0	1	1	1	1	1	0	70	0	0	0	1	1	0	0	0	8	0	0	1	1	1	1	0	0	6	0	1	1	1	1	1	1	0
23	0	1	1	1	1	1	1	0	1	0	0	0	1	1	0	0	0	9	0	0	0	1	1	1	0	0	7	0	1	1	1	1	1	1	0
24	0	1	1	1	1	1	1	1	2	0	0	0	1	1	0	0	0	120	0	0	0	1	1	1	0	0	8	0	1	1	1	1	1	1	0
25	0	1	1	1	1	1	1	1	3	0	0	0	1	1	1	0	0	1	0	0	0	1	1	1	0	0	9	0	1	1	1	1	1	1	0
26	0	1	1	1	1	1	1	1	4	0	0	0	1	1	1	0	0	2	0	0	0	1	1	1	0	0	170	0	1	1	1	1	1	1	0
27	0	1	1	1	1	1	1	1	5	0	0	0	1	1	1	0	0	3	0	0	0	1	1	0	0	0	1	0	1	1	1	1	1	1	0
28	0	1	1	1	1	1	1	1	6	0	0	0	1	1	1	0	0	4	0	0	0	1	1	0	0	0	2	0	1	1	1	1	1	0	0
29	0	1	1	1	1	1	1	1	7	0	0	0	1	1	1	0	0	5	0	0	0	1	1	0	0	0	3	0	0	1	1	1	1	0	0
30	0	1	1	1	1	1	1	1	8	0	0	0	1	1	1	0	0	6	0	0	0	1	1	0	0	0	4	0	0	1	1	1	1	0	0
31	1	1	1	1	1	1	1	1	9	0	0	0	1	1	1	0	0	7	0	0	0	1	1	0	0	0	5	0	0	1	1	1	1	0	0
32	1	1	1	1	1	1	1	1	80	0	0	1	1	1	1	0	0	8	0	0	0	1	0	0	0	0	6	0	0	1	1	1	1	0	0
33	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	0	0	9	0	0	0	0	0	0	0	0	7	0	0	1	1	1	1	0	0
34	0	1	1	1	1	1	1	1	2	0	1	1	1	1	1	0	0	130	0	0	0	0	0	0	0	0	8	0	0	1	1	1	1	0	0
35	0	1	1	1	1	1	1	1	3	0	1	1	1	1	1	0	0	1	0	0	0	0	1	0	0	0	9	0	0	1	1	1	1	0	0
36	0	1	1	1	1	1	1	1	4	0	1	1	1	1	1	0	0	2	0	0	0	0	1	1	0	0	180	0	0	1	1	1	1	0	0
37	0	1	1	1	1	1	1	1	5	0	1	1	1	1	1	0	0	3	0	0	0	0	1	1	0	0	1	0	0	0	1	1	0	0	0
38	0	1	1	1	1	1	1	1	6	0	1	1	1	1	1	1	0	4	0	0	0	0	1	1	0	0	2	0	0	0	1	1	0	0	0
39	0	1	1	1	1	1	1	1	7	0	1	1	1	1	1	1	0	5	0	0	0	0	1	1	0	0	3	0	0	0	1	1	0	0	0
40	0	1	1	1	1	1	1	1	8	0	1	1	1	1	1	1	0	6	0	0	0	0	1	1	0	0	4	0	0	0	1	1	0	0	0
41	0	0	1	1	1	1	1	1	9	1	1	1	1	1	1	1	0	7	0	0	0	0	1	1	0	0	5	0	0	0	1	1	0	0	0
42	0	0	1	1	1	1	1	1	90	1	1	1	1	1	1	1	0	8	0	0	0	0	1	1	0	0	6	0	0	0	1	1	0	0	0
43	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	9	0	0	0	1	1	0	0	0	7	0	0	0	1	1	0	0	0
44	0	0	1	1	1	1	1	1	2	1	1	1	1	1	1	1	0	140	0	0	1	1	1	1	0	0		0	0	0	1	0	0	0	0
45	0	0	1	1	1	1	1	1	3	1	1	1	1	1	1	1	0	1	0	0	1	1	1	1	0	0	9	0	0	0	0	0	0	0	0
46	0	0	1	1	1	1	1	1	4	1	1	1	1	1	1	1	0	2	0	0	1	1	1	1	0	0	190	0	0	0	0	0	0	0	0
47	0	0	1	1	1	1	1	1	5	1	1	1	1	1	1	1	0	3	0	0	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0

M 240 D1 AA CONTENT (continued)

Addr. Input	OUTPUT CODE 7 6 5 4 3 2 1 0	Addr. Input	OUTPUT CODE 7 6 5 4 3 2 1 0	Addr. Input	OUTPUT CODE 7 6 5 4 3 2 1 0	Addr. Input	OUTPUT CODE 7 6 5 4 3 2 1 0
192	0 0 0 0 0 0 0 0	240	0 0 1 1 1 1 0 0	288	1 1 1 1 1 1 1 1	336	0 1 1 1 1 1 0 0
3	0 0 0 0 0 0 0 0	1	0 0 1 1 1 1 0 0	9	1 1 1 1 1 1 1 1	7	0 1 1 1 1 1 0 0
4	0 0 0 0 1 0 0 0	2	0 0 1 1 1 1 0 0	290	1 1 1 1 1 1 1 1	8	0 1 1 1 1 1 0 0
5	0 0 0 0 1 0 0 0	3	0 0 0 1 1 1 0 0	1	1 1 1 1 1 1 1 0	9	0 1 1 1 1 1 0 0
6	0 0 0 0 1 0 0 0	4	0 0 0 1 1 1 0 0	2	1 1 1 1 1 1 1 0	340	0 1 1 1 1 1 0 0
7	0 0 0 1 1 0 0 0	5	0 0 0 1 1 1 0 0	3	1 1 1 1 1 1 1 0	1	0 1 1 1 1 1 0 0
8	0 0 0 1 1 0 0 0	6	0 0 0 1 1 1 0 0	4	1 1 1 1 1 1 1 0	2	0 1 1 1 1 1 0 0
9	0 0 0 1 1 0 0 0	7	0 0 0 1 1 1 0 0	5	1 1 1 1 1 1 1 0	3	0 1 1 1 1 1 0 0
200	0 0 0 1 1 0 0 0	8	0 0 0 1 1 1 0 0	6	1 1 1 1 1 1 1 0	4	1 1 1 1 1 1 1 0
1	0 0 0 1 1 0 0 0	9	0 0 0 1 1 1 0 0	7	1 1 1 1 1 1 1 0	5	1 1 1 1 1 1 1 0
2	0 0 0 1 1 1 0 0	250	0 0 0 1 1 1 0 0	8	1 1 1 1 1 1 1 0	6	1 1 1 1 1 1 1 0
3	0 0 0 1 1 1 0 0	1	0 0 0 1 1 1 0 0	9	1 1 1 1 1 1 1 0	7	1 1 1 1 1 1 1 0
4	0 0 0 1 1 1 0 0	2	0 0 0 1 1 1 0 0	300	1 1 1 1 1 1 0 0	8	1 1 1 1 1 1 1 0
5	0 0 1 1 1 1 0 0	3	0 0 0 1 1 1 0 0	1	1 1 1 1 1 1 0 0	9	1 1 1 1 1 1 1 0
6	0 0 1 1 1 1 0 0	4	0 0 0 0 0 0 0 0	2	1 1 1 1 1 1 0 0	350	1 1 1 1 1 1 1 0
7	0 0 1 1 1 1 0 0	5	0 0 0 0 0 0 0 0	3	1 1 1 1 1 1 0 0	1	1 1 1 1 1 1 1 1
8	0 0 1 1 1 1 0 0	6	0 0 0 0 0 0 0 0	4	1 1 1 1 1 1 0 0	2	1 1 1 1 1 1 1 1
9	0 0 1 1 1 1 0 0	7	0 0 0 0 0 0 0 0	5	1 1 1 1 1 1 0 0	3	1 1 1 1 1 1 1 0
210	0 0 1 1 1 1 1 0	8	0 0 0 1 0 0 0 0	6	1 1 1 1 1 1 0 0	4	1 1 1 1 1 1 1 0
1	0 0 1 1 1 1 1 0	9	0 0 0 1 0 0 0 0	7	1 1 1 1 1 1 0 0	5	1 1 1 1 1 1 1 0
2	0 0 1 1 1 1 1 0	260	0 0 0 1 0 0 0 0	8	1 1 1 1 1 0 0 0	6	1 1 1 1 1 1 1 0
3	0 1 1 1 1 1 1 0	1	0 0 0 1 1 0 0 0	9	1 1 1 1 1 0 0 0	7	1 1 1 1 1 1 1 0
4	0 1 1 1 1 1 1 0	2	0 0 0 1 1 0 0 0	310	0 0 0 1 1 0 0 0	8	1 1 1 1 1 1 1 0
5	0 1 1 1 1 1 1 0	3	0 0 0 1 1 0 0 0	1	0 0 0 1 1 0 0 0	9	1 1 1 1 1 1 1 0
6	0 1 1 1 1 1 1 0	4	0 0 0 1 1 0 0 0	2	0 0 0 1 1 0 0 0	360	0 1 1 1 1 1 1 0
7	0 1 1 1 1 1 1 0	5	0 0 0 1 1 0 0 0	3	0 0 0 1 1 0 0 0	1	0 1 1 1 1 1 1 0
8	0 1 1 1 1 1 1 1	6	0 0 1 1 1 0 0 0	4	0 0 0 1 1 0 0 0	2	0 1 1 1 1 1 1 0
9	0 1 1 1 1 1 1 1	7	0 0 1 1 1 0 0 0	5	0 0 0 1 0 0 0 0	3	0 1 1 1 1 1 1 0
220	0 1 1 1 1 1 1 1	8	0 0 1 1 1 0 0 0	6	0 0 0 1 0 0 0 0	4	0 1 1 1 1 1 1 0
1	1 1 1 1 1 1 1 1	9	0 0 1 1 1 0 0 0	7	0 0 0 1 0 0 0 0	5	0 1 1 1 1 1 1 0
2	1 1 1 1 1 1 1 1	270	0 0 1 1 1 1 0 0	8	0 0 0 0 0 0 0 0	6	0 1 1 1 1 1 1 0
3	1 1 1 1 1 1 1 1	1	0 0 1 1 1 1 0 0	9	0 0 0 0 0 0 0 0	7	0 1 1 1 1 1 1 0
4	1 1 1 1 1 1 1 1	2	0 0 1 1 1 1 0 0	320	0 0 0 1 0 0 0 0	8	0 0 1 1 1 1 1 0
5	1 1 1 1 1 1 1 1	3	0 0 1 1 1 1 0 0	1	0 0 0 1 0 0 0 0	9	0 0 1 1 1 1 0 0
6	1 1 1 1 1 1 1 1	4	0 1 1 1 1 1 0 0	2	0 0 0 1 0 0 0 0	370	0 0 1 1 1 1 0 0
7	0 1 1 1 1 1 1 1	5	0 1 1 1 1 1 0 0	3	0 0 0 1 0 0 0 0	1	0 0 1 1 1 1 0 0
8	0 1 1 1 1 1 1 1	6	0 1 1 1 1 1 0 0	4	0 0 0 1 0 0 0 0	2	0 0 1 1 1 1 0 0
9	0 1 1 1 1 1 1 1	7	0 1 1 1 1 1 1 0	5	0 0 0 1 0 0 0 0	3	0 0 1 1 1 1 0 0
230	0 1 1 1 1 1 1 0	8	0 1 1 1 1 1 1 0	6	0 0 0 1 0 0 0 0	4	0 0 1 1 1 1 0 0
1	0 1 1 1 1 1 1 0	9	0 1 1 1 1 1 1 0	7	0 0 0 1 1 0 0 0	5	0 0 1 1 1 1 0 0
2	0 1 1 1 1 1 1 0	280	0 1 1 1 1 1 1 0	8	0 0 1 1 1 0 0 0	6	0 0 0 1 1 0 0 0
3	0 1 1 1 1 1 1 0	1	0 1 1 1 1 1 1 0	9	0 0 1 1 1 0 0 0	7	0 0 0 1 0 0 0 0
4	0 1 1 1 1 1 1 0	2	1 1 1 1 1 1 1 0	330	0 0 1 1 1 0 0 0	8	0 0 0 1 0 0 0 0
5	0 0 1 1 1 1 1 0	3	1 1 1 1 1 1 1 0	1	0 0 1 1 1 0 0 0	9	0 0 0 1 0 0 0 0
6	0 0 1 1 1 1 1 0	4	1 1 1 1 1 1 1 0	2	0 0 1 1 1 0 0 0	380	0 0 0 1 0 0 0 0
7	0 0 1 1 1 1 1 0	5	1 1 1 1 1 1 1 1	3	0 0 1 1 1 0 0 0	1	0 0 0 1 0 0 0 0
8	0 0 1 1 1 1 1 0	6	1 1 1 1 1 1 1 1	4	0 0 1 1 1 0 0 0	2	0 0 0 1 0 0 0 0
9	0 0 1 1 1 1 0 0	7	1 1 1 1 1 1 1 1	5	0 0 1 1 1 1 0 0	3	0 0 0 1 0 0 0 0

M 240 D1 AA CONTENT (continued)

Addr. Input	OUTPUT CODE O_7 O_6 O_5 O_4 O_3 O_2 O_1 O_0	Addr. Input	OUTPUT CODE O_7 O_6 O_5 O_4 O_3 O_2 O_1 O_0	Addr. Input	OUTPUT CODE O_7 O_6 O_5 O_4 O_3 O_2 O_1 O_0	Addr. Input	OUTPUT CODE O_7 O_6 O_5 O_4 O_3 O_2 O_1 O_0
384	0 0 0 0 0 0 0 0	416	1 1 1 1 1 1 1 1	448	0 0 0 0 0 0 0 0	480	1 1 1 1 1 1 1 1
5	0 0 0 0 1 0 0 0	7	1 1 1 1 1 1 1 1	9	0 0 0 0 0 0 0 0	1	1 1 1 1 1 1 1 1
6	0 0 0 0 1 0 0 0	8	0 1 1 1 1 1 1 1	450	0 0 0 0 0 0 0 0	2	1 1 1 1 1 1 1 1
7	0 0 0 0 1 0 0 0	9	0 1 1 1 1 1 1 1	1	0 0 0 0 1 0 0 0	3	1 1 1 1 1 1 1 1
8	0 0 0 0 1 0 0 0	420	0 1 1 1 1 1 1 1	2	0 0 0 1 1 0 0 0	4	0 1 1 1 1 1 1 1
9	0 0 0 0 1 0 0 0	1	0 1 1 1 1 1 1 1	3	0 0 0 1 1 0 0 0	5	0 1 1 1 1 1 1 0
390	0 0 0 1 1 0 0 0	2	0 1 1 1 1 1 1 1	4	0 0 0 1 1 0 0 0	6	0 1 1 1 1 1 1 0
1	0 0 0 1 1 0 0 0	3	0 1 1 1 1 1 1 0	5	0 0 0 1 1 0 0 0	7	0 1 1 1 1 1 1 0
2	0 0 0 1 1 0 0 0	4	0 1 1 1 1 1 1 0	6	0 0 0 1 1 0 0 0	8	0 1 1 1 1 1 1 0
3	0 0 0 1 1 1 0 0	5	0 1 1 1 1 1 1 0	7	0 0 0 1 1 0 0 0	9	0 1 1 1 1 1 1 0
4	0 0 0 1 1 1 0 0	6	0 0 1 1 1 1 1 0	8	0 0 0 1 1 0 0 0	490	0 1 1 1 1 1 1 0
5	0 0 0 1 1 1 0 0	7	0 0 1 1 1 1 1 0	9	0 0 0 1 1 1 0 0	1	0 1 1 1 1 1 1 0
6	0 0 0 1 1 1 0 0	8	0 0 1 1 1 1 1 0	460	0 0 1 1 1 1 0 0	2	0 0 1 1 1 1 1 0
7	0 0 0 1 1 1 0 0	9	0 0 1 1 1 1 1 0	1	0 0 1 1 1 1 0 0	3	0 0 1 1 1 1 0 0
8	0 0 1 1 1 1 0 0	430	0 0 1 1 1 1 1 0	2	0 0 1 1 1 1 0 0	4	0 0 1 1 1 1 0 0
9	0 0 1 1 1 1 0 0	1	0 0 1 1 1 1 0 0	3	0 0 1 1 1 1 0 0	5	0 0 1 1 1 1 0 0
400	0 0 1 1 1 1 0 0	2	0 0 1 1 1 1 0 0	4	0 0 1 1 1 1 0 0	6	0 0 1 1 1 1 0 0
1	0 0 1 1 1 1 1 0	3	0 0 1 1 1 1 0 0	5	0 0 1 1 1 1 0 0	7	0 0 1 1 1 1 0 0
2	0 0 1 1 1 1 1 0	4	0 0 0 1 1 1 0 0	6	0 0 1 1 1 1 0 0	8	0 0 1 1 1 1 0 0
3	0 0 1 1 1 1 1 0	5	0 0 0 1 1 1 0 0	7	0 0 1 1 1 1 1 0	9	0 0 1 1 1 1 0 0
4	0 0 1 1 1 1 1 0	6	0 0 0 1 1 1 0 0	8	0 1 1 1 1 1 1 0	500	0 0 0 1 1 1 0 0
5	0 0 1 1 1 1 1 0	7	0 0 0 1 1 1 0 0	9	0 1 1 1 1 1 1 0	1	0 0 0 1 1 0 0 0
6	0 1 1 1 1 1 1 0	8	0 0 0 1 1 1 0 0	470	0 1 1 1 1 1 1 0	2	0 0 0 1 1 0 0 0
7	0 1 1 1 1 1 1 0	9	0 0 0 1 1 0 0 0	1	0 1 1 1 1 1 1 0	3	0 0 0 1 1 0 0 0
8	0 1 1 1 1 1 1 0	440	0 0 0 1 1 0 0 0	2	0 1 1 1 1 1 1 0	4	0 0 0 1 1 0 0 0
9	0 1 1 1 1 1 1 1	1	0 0 0 1 1 0 0 0	3	0 1 1 1 1 1 1 0	5	0 0 0 1 1 0 0 0
410	0 1 1 1 1 1 1 1	2	0 0 0 0 1 0 0 0	4	0 1 1 1 1 1 1 0	6	0 0 0 1 1 0 0 0
1	0 1 1 1 1 1 1 1	3	0 0 0 0 1 0 0 0	5	0 1 1 1 1 1 1 1	7	0 0 0 1 1 0 0 0
2	0 1 1 1 1 1 1 1	4	0 0 0 0 1 0 0 0	6	1 1 1 1 1 1 1 1	8	0 0 0 0 1 0 0 0
3	0 1 1 1 1 1 1 1	5	0 0 0 0 1 0 0 0	7	1 1 1 1 1 1 1 1	9	0 0 0 0 0 0 0 0
4	1 1 1 1 1 1 1 1	6	0 0 0 0 1 0 0 0	8	1 1 1 1 1 1 1 1	510	0 0 0 0 0 0 0 0
5	1 1 1 1 1 1 1 1	7	0 0 0 0 0 0 0 0	9	1 1 1 1 1 1 1 1	1	0 0 0 0 0 0 0 0

MOS INTEGRATED CIRCUIT

M 250

PRELIMINARY DATA

RHYTHM GENERATOR

- DRIVES 8 SOUND GENERATORS (INSTRUMENTS)
- 5 BIT COUNTER
- 12 RHYTHMS PER INSTRUMENT
- EXTERNAL RESET

The M 250 is a monolithic rhythm generator specifically designed for electronic organs and other musical instruments. Constructed on a single chip using Planox® silicon nitride P-channel technology it is supplied in a 24-lead dual in-line ceramic package.

ABSOLUTE MAXIMUM RATINGS

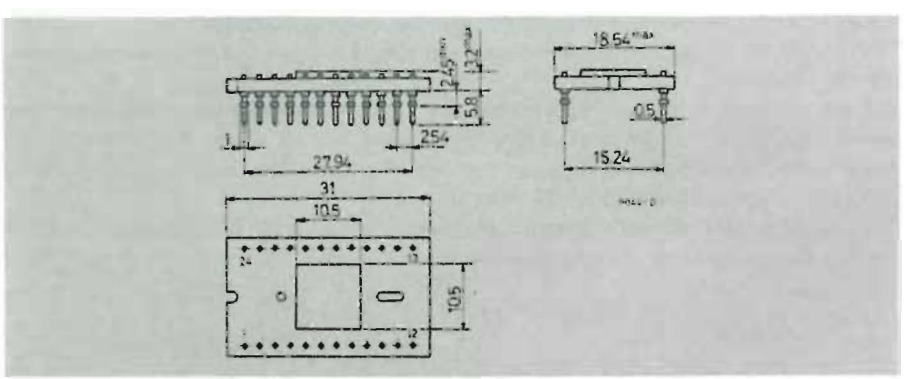
V_{GG}	Supply voltage (see note)	-20 to 0.3	V
V_I	Input voltage (see note)	-20 to 0.3	V
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	0 to 70	°C

NOTE: This voltage is with respect to the V_{SS} pin voltage.

ORDERING NUMBER : M 250 D1.

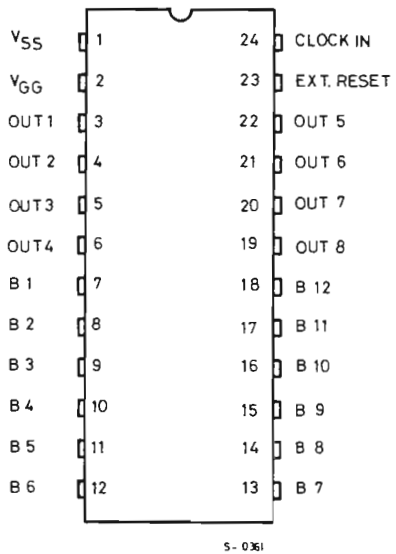
MECHANICAL DATA

Dimensions in mm



M 250

CONNECTION DIAGRAM (top view)



DEVICE DESCRIPTION

The M 250 contains a ROM which can drive 8 sound generators (instruments) with a selection of 12 rhythms for each generator. An external clock drives a phase generator which produces complementary outputs, these signals are then divided-by-2, to produce the signals to enable the output buffers and drive a 5-stage binary counter.

The outputs of the counter are decoded, being the 32 rows of the memory matrix which has 108 columns.

The 108 columns are divided into 9 groups of 12. A multiplexer is used such that any number of columns in the 9 groups can be selected from 1 to 12. Of the 9 groups in the memory matrix, 8 have buffered outputs via an enabling circuit (the enabling conditions being CS1 = "0" and at least one multiplex input at logic "1").

The 9th group in the matrix controls the internal reset which is synchronised with the counter and controls the counting sequence.

STATIC AND DYNAMIC ELECTRICAL CHARACTERISTICS

(V_{GG}= GND; V_{SS}= 14 to 18V, T_{amb} = 0 to 70°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
CLOCK INPUT						
V_{IH}	Clock high voltage		V_{SS}-1			V
V_{IL}	Clock low voltage				V_{SS}-10	V
f	Clock repetition rate		DC		100	μs
$t\phi_{pw}$*	Pulse width	Duty cycle= 50%	5			μs
$t\phi_d$	Pulse delay		5			μs
t_r**	Rise time	T_{amb}= 25°C			5	μs
t_f**	Fall time				5	μs
DATA INPUTS (B1 . . . . . B12)						
V_{IH}	Input high voltage		V_{SS}-1			V
V_{IL}	Input low voltage				V_{SS}-10	V
I_L	Input leakage current	V_i= V_{SS}-14 V T_{amb}= 25°C			10	μA
EXTERNAL RESET						
V_{IH}	Input high voltage		V_{SS}-1			V
V_{IL}	Input low voltage				V_{SS}-10	V
I_L	Input leakage current	V_i= V_{SS}-14V T_{amb}=25°C			10	μA
t_{pw}	Pulse width		5			μs
DATA OUTPUTS						
I_{OH}	Output high current	V_{SS} = 18V			100	μA

STATIC AND DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

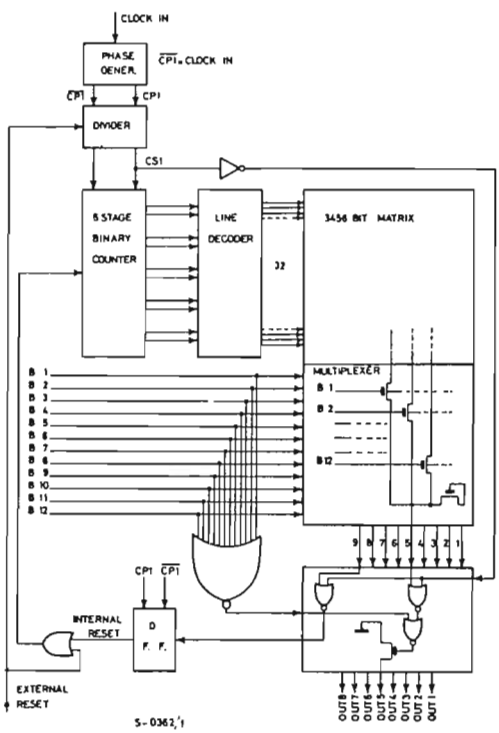
Parameter	Test conditions	Min.	Typ.	Max.	Unit
R_{ON} Output resistance	$V_o = V_{SS} - 2V$		1	2	kΩ

POWER DISSIPATION

I_{GG} Supply current	$V_{GG} = V_{SS} - 18V$ $T_{amb} = 25°C$		10		mA

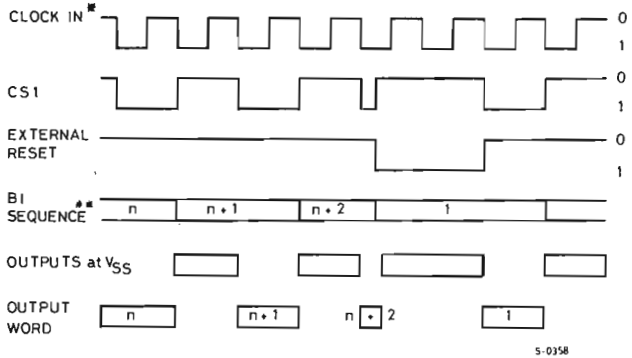
* Measured at 50% of the swing
** Measured between 10% and 90% of the swing

BLOCK DIAGRAM

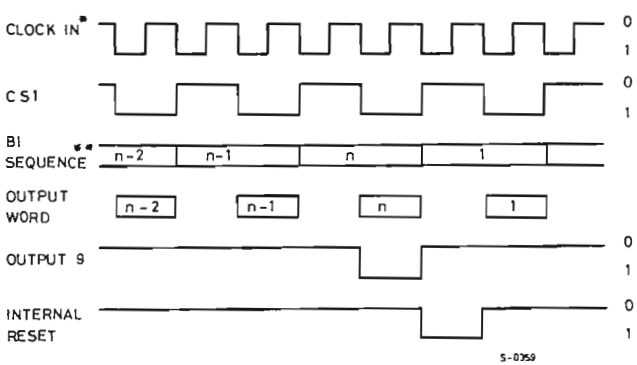


TIMING DIAGRAMS

Output words versus external reset



Output words versus internal reset



* External gating allows resetting of the variable clock generator to ensure that the beat starts at exactly the right moment

** i = 1 12

TYPICAL APPLICATIONS

Figure 1 shows the typical application of the M 250.
With two M 250 devices it is possible to increase either number of rhythms or the number of instruments available, as shown in figures 2 and 3 respectively.
The use of a memory matrix allows the customer complete flexibility, since modification of the memory is quick and relatively cheap.

Fig. 1 – Rhythm system

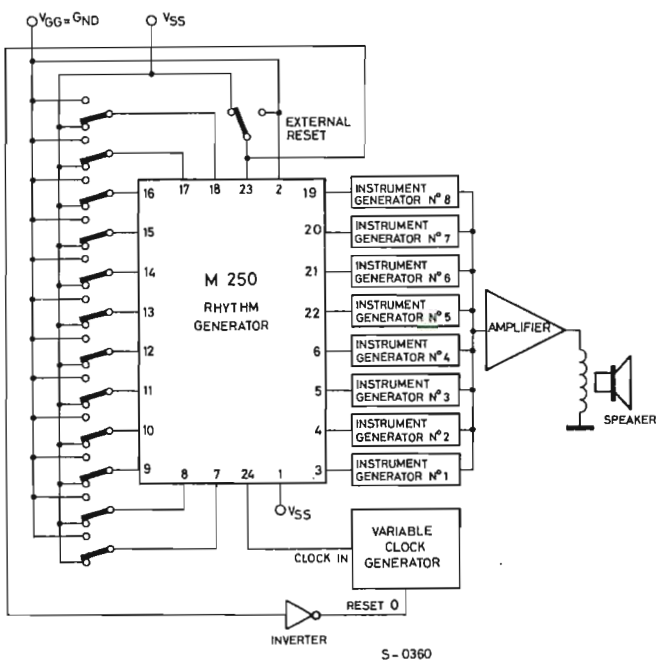
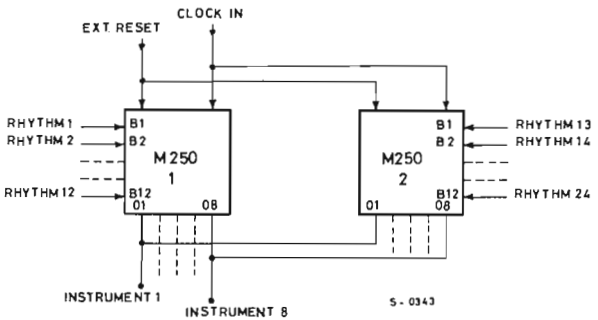
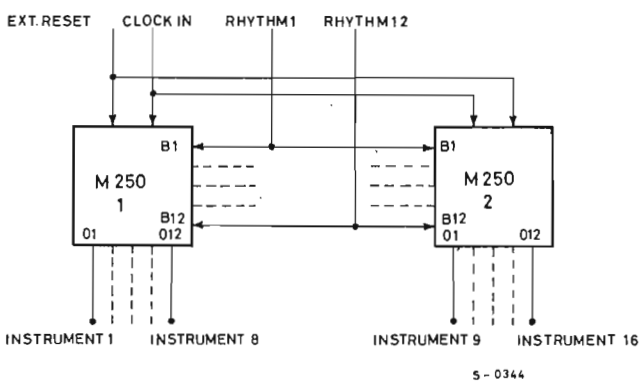


Fig. 2 - Increase in number of rhythms



Note: This solution does not allow to select simultaneously two rhythms one for each device

Fig. 3 - Increase in number of instruments



COMPLETING THE TRUTH TABLE

As described previously the ROM matrix is organized in 32 rows which represent elementary times and 108 columns (9 groups of 12) where each group represents an instrument which has at its disposition 12 programmable rhythms.
The 9th group is not used to drive a sound generator (i.e. an instrument), but to reset the counter in anyone of the 32 elementary times. As an example of this if we wish to programme a rhythm in a 4/4 time e.g. tango, we can use all 32 elementary times because 32 can be divided by 4, 8, 16, 32 and therefore no reset is required.
However, should we wish to programme a rhythm in 3/4 e.g. waltz, we must use only 24 elementary times because 24 can be divided by 3, 6, 12, 24. In this case we must put a sign in the box which corresponds to number 24, hereby obtaining the reading of the first 24 boxes or positions and the resetting of the boxes from 25 to 32.
In this way, to complete the rhythm for each instrument the following procedure must be followed;

e.g. Rhythm n. 1 - Tango
n. 2 - Waltz
n. 3 - Samba
n. 4 - Cha-cha-cha etc.

Starting with the rhythm n. 1 to which the first column of each of the 8 remaining groups corresponds, one indicates (with a cross) in the appropriate boxes the timing for each percussion required for each instrument.
A low level voltage signal will be obtained at the output where the sign is programmed, giving in this way the complete rhythm sequence.

COUNT TO 32	OUTPUT 1												OUTPUT 2												OUTPUT 3											
	rhythm 1	2	3	4	5	6	7	8	9	10	11	12	rhythm 1	2	3	4	5	6	7	8	9	10	11	12	rhythm 1	2	3	4	5	6	7	8	9	10	11	12
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ROM Columns	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36

COUNT TO 32	OUTPUT 4												OUTPUT 5												OUTPUT 6											
	rhythm 1	2	3	4	5	6	7	8	9	10	11	12	rhythm 1	2	3	4	5	6	7	8	9	10	11	12	rhythm 1	2	3	4	5	6	7	8	9	10	11	12
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ROM Columns	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72

M 250

COUNT TO 32	OUTPUT 7												OUTPUT 8												COUNTING CONTROL											
	rhythm	1	2	3	4	5	6	7	8	9	10	11	12	rhythm	1	2	3	4	5	6	7	8	9	10	11	12	rhythm	1	2	3	4	5	6	7	8	9	10	11	12
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ROM Columns	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108			

COS/MOS INTEGRATED CIRCUITS

COS/MOS INTEGRATED CIRCUITS

E. = Extended temperature range
S. = Standard temperature range

COS/MOS INTEGRATED CIRCUITS

NOR GATES: QUAD 2 INPUT HBC/HBF 4001A
DUAL 4 INPUT HBC/HBF 4002A
TRIPLE 3 INPUT HBC/HBF 4025A

- LOW QUIESCENT POWER DISSIPATION: 10 nW/PACKAGE
- WIDE SUPPLY VOLTAGE RANGE: 3 to 15V
- HIGH NOISE IMMUNITY: 45% of V_{DD} (TYP.)
- MEDIUM SPEED OPERATION: $t_{PHL} = t_{PLH} = 25$ ns (TYP.) at $C_L = 15$ pF
- INPUTS FULLY PROTECTED
- LOW "1" and "0" OUTPUT LEVEL IMPEDANCE: 500Ω and 200Ω (TYP.), RESPECTIVELY at $V_{DD} - V_{SS} = 10V$
- HIGH FANOUT: > 50

The **HBC 4001A, HBC 4002A, HBC 4025A** (extended temperature range) and **HBF 4001A, HBF 4002A, HBF 4025A** (standard temperature range) NOR gates are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic chip. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.
They are available in 14-lead dual in-line plastic or ceramic package and ceramic flat package.

ABSOLUTE MAXIMUM RATINGS

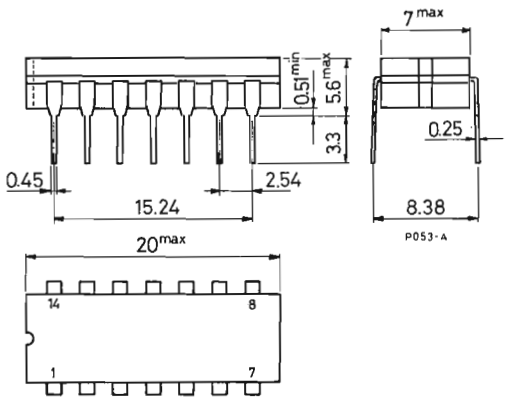
V_{DD}-V_{SS}	Supply voltage	-0.5 to 15	V
V_i	Input voltage (at any pin)	$V_{SS} \leqslant V_i \leqslant V_{DD}$	
P_{tot}	Total power dissipation (per package)	200	mW
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature:		
	for HBC types	-55 to 125	°C
	for HBF types	-40 to 85	°C

ORDERING NUMBERS:

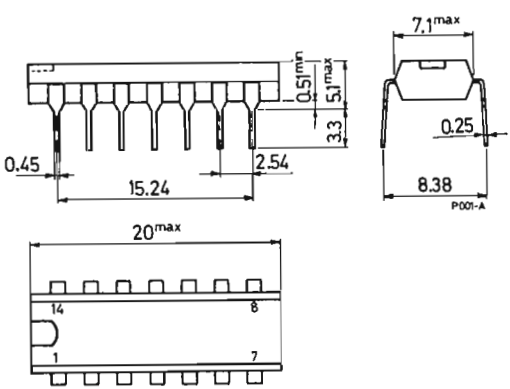
HBC 4 XXX AD for dual in-line ceramic package
HBC 4 XXX AF for dual in-line ceramic package frit seal (extended temperature range)
HBC 4 XXX AK for ceramic flat package
HBF 4 XXX AE for dual in-line plastic package
HBF 4 XXX AF for dual in-line ceramic package frit seal (standard temperature range)

MECHANICAL DATA (dimensions in mm)

Dual in-line ceramic package
for HBC 4 XXX AD and
HBC/HBF 4 XXX AF

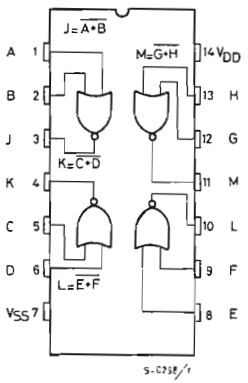


Dual in-line plastic package
(similar to TO-116)
for HBF 4 XXX AE

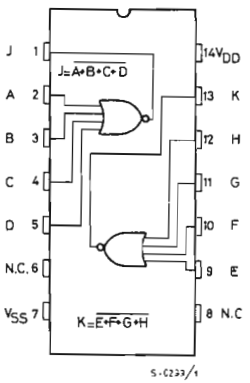


Ceramic flat package for HBC 4 XXX AK

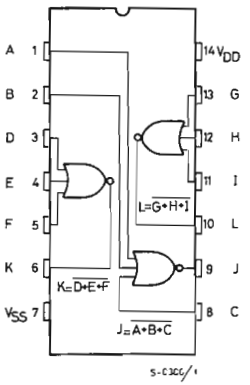
CONNECTION DIAGRAMS
(top view)



For **4001A**



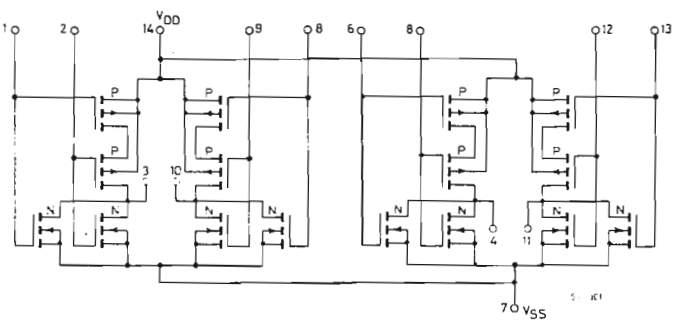
For **4002A**



For **4025A**

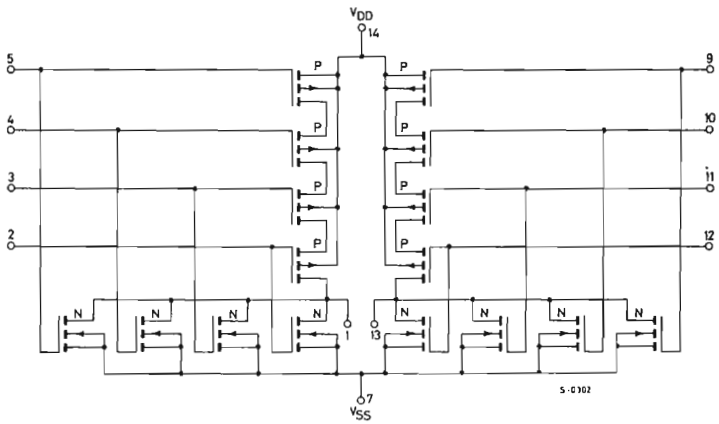
SCHEMATIC DIAGRAMS

For **4001A**

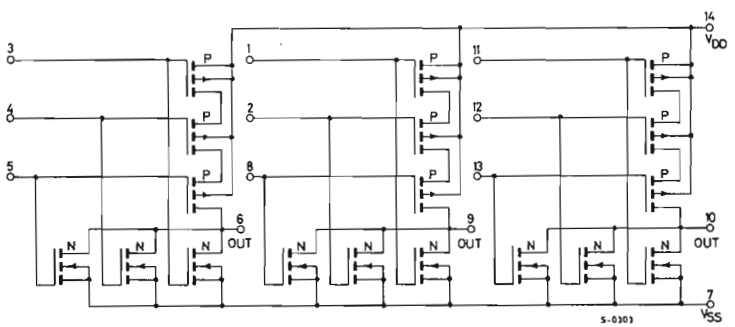


SCHEMATIC DIAGRAMS (continued)

For **4002A**



For **4025A**



RECOMMENDED OPERATING CONDITIONS

V_{DD} *	Supply voltage	3 to 15	V
V_i *	Input voltage	V_{DD} to V_{SS}	
T_{op}	Operating temperature		
	for HBC types	-55 to 125	°C
	for HBF types	-40 to 85	°C

* This is measured with respect to the V_{SS} pin voltage

STATIC ELECTRICAL CHARACTERISTICS

Parameter		Test conditions	Min.	Typ.	Max.	Unit
HBC types (extended temperature range)						
I_L	Quiescent current	V_{DD} = 5V				
		at T_{amb}=-55°C			0.05	µA
		at T_{amb}= 25°C		0.001	0.05	µA
		at T_{amb}=125°C			3	µA
		V_{DD} = 10V				
		at T_{amb}=-55°C			0.1	µA
		at T_{amb}= 25°C		0.001	0.1	µA
		at T_{amb}=125°C			6	µA
V_{OH}	Output high voltage	I_o = 0				
		V_{DD} = 5V				
		at T_{amb}=-55°C	4.99			V
		at T_{amb}= 25°C	4.99	5		V
		at T_{amb}=125°C	4.95			V
		V_{DD} = 10V				
		at T_{amb}=-55°C	9.99			V
		at T_{amb}= 25°C	9.99	10		V
		at T_{amb}=125°C	9.95			V
V_{OL}	Output low voltage	I_o = 0				
		V_{DD} = 5V or 10V				
		at T_{amb}=-55°C			0.01	V
		at T_{amb}= 25°C		0	0.01	V
		at T_{amb}=125°C			0.05	V
→ V_{NH}	Noise immunity	V_{DD} = 5V V_o = 0.95V				
		at T_{amb}=-55°C	1.4			V
		at T_{amb}= 25°C	1.5	2.25		V
		at T_{amb}=125°C	1.5			V
		V_{DD} = 10V V_o = 2.9V				
		at T_{amb}=-55°C	2.9			V
		at T_{amb}= 25°C	3	4.5		V
		at T_{amb}=125°C	3			V
→ V_{NL}	Noise immunity	V_{DD} = 5V V_o = 3.6V				
		at T_{amb}=-55°C	1.5			V
		at T_{amb}= 25°C	1.5	2.25		V
		at T_{amb}=125°C	1.4			V

STATIC ELECTRICAL CHARACTERISTICS (continued)

	Parameter		Test conditions	Min.	Typ.	Max.	Unit
→	V_{NL}	Noise immunity	V_{DD} = 10V V_o = 7.2V				
			at T_{amb}=-55°C	3			V
			at T_{amb}= 25°C	3		4.5	V
			at T_{amb}=125°C	2.9			V
→	I_DN	Output drive current N-channel	V_{DD} = 5V V_o = 0.4V				
			at T_{amb}=-55°C	0.5			mA
			at T_{amb}= 25°C	0.4		1	mA
			at T_{amb}=125°C	0.28			mA
			V_{DD} = 10V V_o = 0.5V				
			at T_{amb}=-55°C	1.1			mA
			at T_{amb}= 25°C	0.9		2.5	mA
			at T_{amb}=125°C	0.65			mA
→	I_DP	Output drive current P-channel	V_{DD} = 5V V_o = 2.5V				
			at T_{amb}=-55°C	-0.62			mA
			at T_{amb}= 25°C	-0.5		-2	mA
			at T_{amb}=125°C	-0.35			mA
			V_{DD} = 10V V_o = 9.5V				
			at T_{amb}=-55°C	-0.62			mA
			at T_{amb}= 25°C	-0.5		-1	mA
			at T_{amb}=125°C	-0.35			mA
	I_I	Input current	T_{amb} = 25°C		10		pA

HBF types (standard temperature range)

I_L	Quiescent current	V_{DD} = 5V				
		at T_{amb}=-40°C			0.5	μA
		at T_{amb}= 25°C		0.005	0.5	μA
		at T_{amb}= 85°C			15	μA
		V_{DD} = 10V				
		at T_{amb}=-40°C			5	μA
		at T_{amb}= 25°C		0.005	5	μA
		at T_{amb}= 85°C			30	μA
V_{OH}	Output high voltage	I_o = 0				
		V_{DD} = 5V				
		at T_{amb}=-40°C	4.99			V
		at T_{amb}= 25°C	4.99		5	V
		at T_{amb}= 85°C	4.95			V

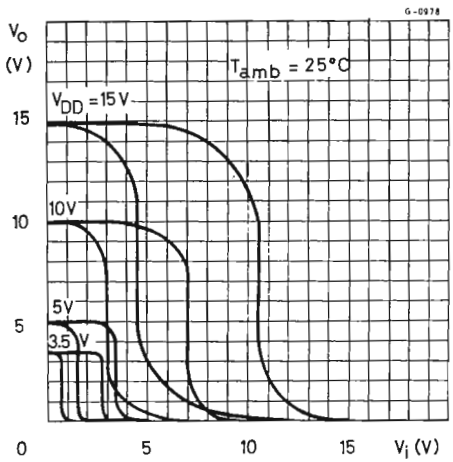
STATIC ELECTRICAL CHARACTERISTICS (continued)

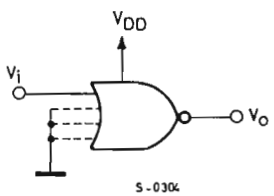
	Parameter	Test conditions	Min.	Typ.	Max.	Unit
→	V_{OH} Output high voltage	$I_o = 0$				
		$V_{DD} = 10V$				
		at T_{amb}=-40°C	9.99			V
		at T_{amb}= 25°C	9.99	10		V
		at T_{amb}= 85°C	9.95			V
	V_{OL} Output low voltage	$I_o = 0$				
		V_{DD} = 5V or 10V				
		at T_{amb}=-40°C			0.01	V
		at T_{amb}= 25°C		0	0.01	V
		at T_{amb}= 85°C			0.05	V
→	V_{NH} Noise immunity	V_{DD} = 5V V_o = 0.95V				
		at T_{amb}=-40°C	1.4			V
		at T_{amb}= 25°C	1.5	2.25		V
		at T_{amb}= 85°C	1.5			V
		V_{DD} = 10V V_o = 2.9V				
		at T_{amb}=-40°C	2.9			V
		at T_{amb}= 25°C	3	4.5		V
		at T_{amb}= 85°C	3			V
→	V_{NL} Noise immunity	V_{DD} = 5V V_o = 3.6V				
		at T_{amb}=-40°C	1.5			V
		at T_{amb}= 25°C	1.5	2.25		V
		at T_{amb}= 85°C	1.4			V
		V_{DD} = 10V V_o = 7.2V				
		at T_{amb}=-40°C	3			V
		at T_{amb}= 25°C	3	4.5		V
		at T_{amb}= 85°C	2.9			V
	I_DN Output drive current N-channel	V_{DD} = 5V V_o = 0.4V				
		at T_{amb}=-40°C	0.35			mA
		at T_{amb}= 25°C	0.3	1		mA
		at T_{amb}= 85°C	0.24			mA
		V_{DD} = 10V V_o = 0.5V				
		at T_{amb}=-40°C	0.72			mA
		at T_{amb}= 25°C	0.6	2.5		mA
		at T_{amb}= 85°C	0.48			mA

STATIC ELECTRICAL CHARACTERISTICS (continued)

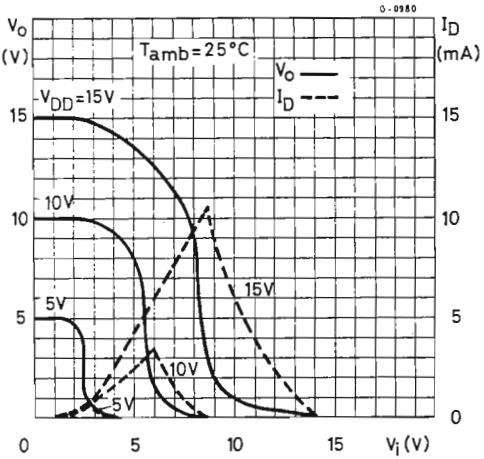
Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_DP	Output drive current P-channel	V_{DD} = 5V V_o = 2.5V				
		at T_{amb} = -40°C		-0.35		mA
		at T_{amb} = 25°C		-0.3	-2	mA
		at T_{amb} = 85°C		-0.24		mA
		V_{DD} = 10V V_o = 9.5V				
		at T_{amb} = -40°C		-0.3		mA
		at T_{amb} = 25°C		-0.25	-1	mA
		at T_{amb} = 85°C		-0.2		mA
I_i	Input current	T_{amb} = 25°C		10		pA

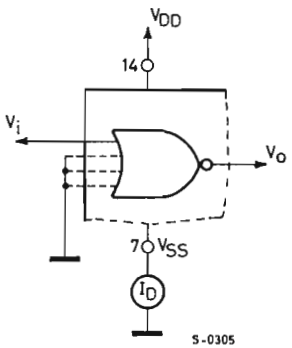
Minimum and maximum voltage transfer characteristic curves and test circuit



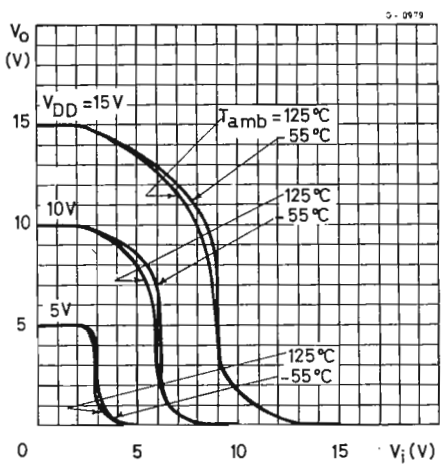


Typical current and voltage transfer characteristic curves and test circuit

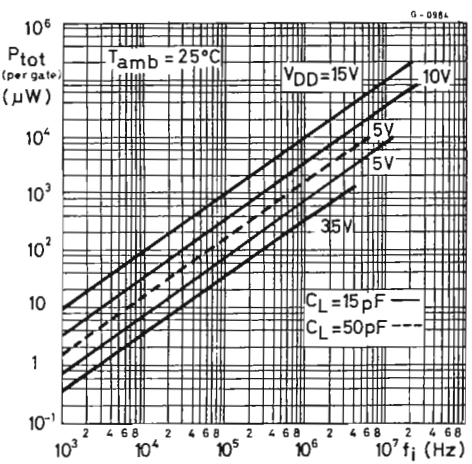




Typical voltage transfer characteristics vs. ambient temperature



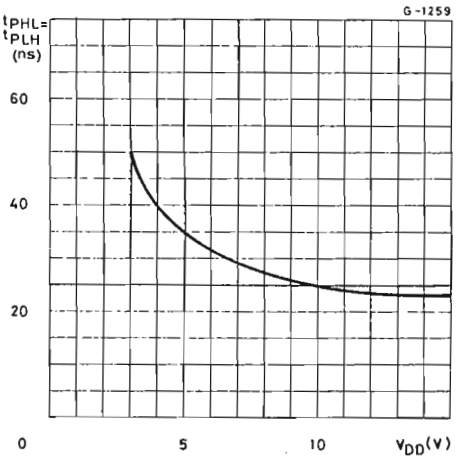
Typical power dissipation characteristics



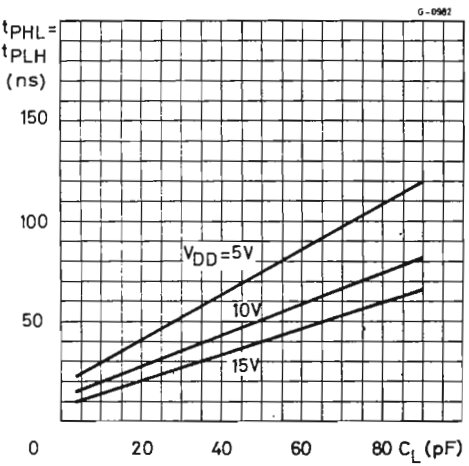
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 15 pF, typical temperature coefficient for all V_{DD} = 0.3 %/°C values)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
t_{PLH}	Propagation delay time (low to high level)	V_{DD} = 5V				
		for **HBC** types		35	95	ns
		for **HBF** types		35	120	ns
		V_{DD} = 10V				
		for **HBC** types		25	45	ns
		for **HBF** types		25	65	ns
t_{PHL}	Propagation delay time (high to low level)	V_{DD} = 5V				
		for **HBC** types		35	50	ns
		for **HBF** types		35	80	ns
		V_{DD} = 10V				
		for **HBC** types		25	40	ns
		for **HBF** types		25	55	ns
t_{TLH}	Transition time (low to high level)	V_{DD} = 5V				
		for **HBC** types		65	175	ns
		for **HBF** types		65	300	ns
		V_{DD} = 10V				
		for **HBC** types		35	75	ns
		for **HBF** types		35	125	ns
t_{THL}	Transition time (high to low level)	V_{DD} = 5V				
		for **HBC** types		65	125	ns
		for **HBF** types		65	200	ns
		V_{DD} = 10V				
		for **HBC** types		35	70	ns
		for **HBF** types		35	115	ns
C_I	Input capacitance	Any input for **HBC** and **HBF** types		5		pF

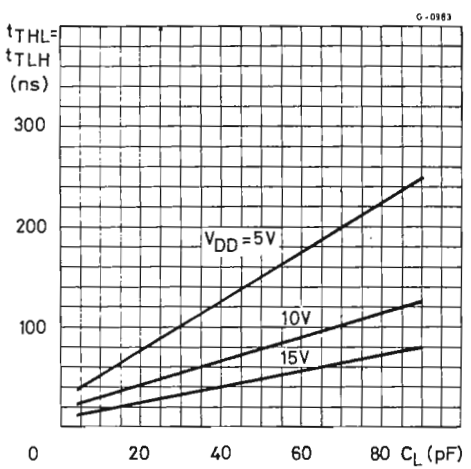
Typical propagation delay time vs. V_{DD}



Typical propagation delay time vs. C_L



Typical transition time vs. C_L



COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

DUAL COMPLEMENTARY PAIR PLUS INVERTER

- LOW QUIESCENT POWER DISSIPATION: 10 nW/PACKAGE
- WIDE SUPPLY VOLTAGE RANGE: 3 to 15V
- HIGH NOISE IMMUNITY: 45% of V_{DD} (TYP.)
- MEDIUM SPEED OPERATION: $t_{PHL} = t_{PLH} = 50$ ns (TYP.) at $C_L = 15$ pF
- INPUTS FULLY PROTECTED
- LOW "1" and "0" OUTPUT LEVEL IMPEDANCE: 500Ω (TYP.) at $V_{DD} - V_{SS} = 10V$
- HIGH FANOUT: > 50

The **HBC 4007A** (extended temperature range) and **HBF 4007A** (standard temperature range) are monolithic integrated circuits, available in 14-lead dual in-line plastic or ceramic package and ceramic flat package.

They consist of three N-channel and P-channel enhancement-type MOS transistors. Each transistor is fully accessible to provide a convenient means for constructing the various typical circuits shown in figs. 13 to 19.

Typical applications are found in: extremely high-input impedance amplifiers, inverters, shapers, linear amplifiers, threshold detectors.

ABSOLUTE MAXIMUM RATINGS

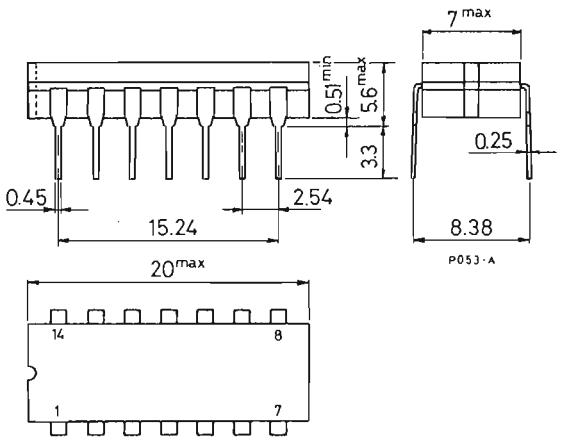
V_{DD}-V_{SS}	Supply voltage	-0.5 to 15 V
V_I	Input voltage (at any pin)	$V_{SS} \leqslant V_I \leqslant V_{DD}$
P_{tot}	Total power dissipation (per package)	200 mW
T_{stg}	Storage temperature	-65 to 150 °C
T_{op}	Operating temperature: for **HBC** types	-55 to 125 °C
	for **HBF** types	-40 to 85 °C

ORDERING NUMBERS:

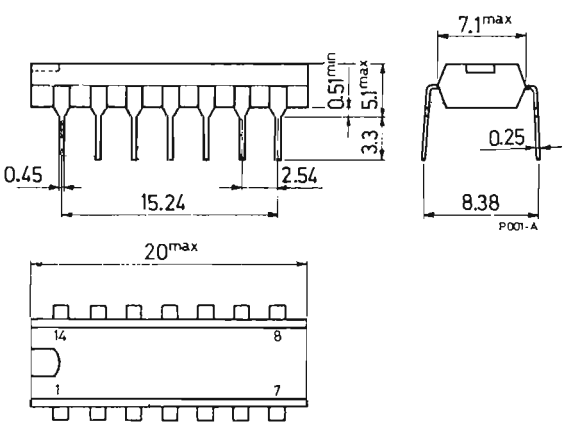
HBC 4007 AD for dual in-line ceramic package
HBC 4007 AF for dual in-line ceramic package, frit seal (extended temperature range)
HBC 4007 AK for ceramic flat package
HBF 4007 AE for dual in-line plastic package
HBF 4007 AF for dual in-line ceramic package, frit seal (standard temperature range)

MECHANICAL DATA (dimensions in mm)

Dual in-line ceramic package
for HBC 4007 AD and
HBC/HBF 4007 AF

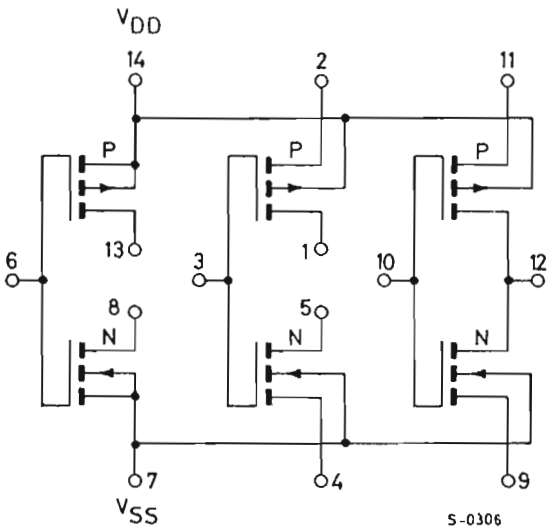


Dual in-line plastic package
(similar to TO-116)
for HBF4007AE



Ceramic flat package for HBC4007AK

SCHEMATIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

V_{DD} *	Supply voltage	3 to 15	V
V_i *	Input voltage	V_{DD} to V_{SS}	
T_{op}	Operating temperature : for **HBC** types	-55 to 125	°C
	for **HBF** types	-40 to 85	°C

* This is measured with respect to the V_{SS} pin voltage

STATIC ELECTRICAL CHARACTERISTICS

Parameter		Test conditions	Min.	Typ.	Max.	Unit
HBC types (extended temperature range)						
I_L*	Quiescent current	V_{DD}= 5V				
		at T_{amb}= -55°C			0.05	µA
		at T_{amb}= 25°C		0.001	0.05	µA
		at T_{amb}= 125°C			3	µA
		V_{DD}= 10V				
		at T_{amb}= -55°C			0.1	µA
		at T_{amb}= 25°C		0.001	0.1	µA
		at T_{amb}= 125°C			6	µA
V_{OH}	Output high voltage	I_o = 0				
		V_{DD}= 5V				
		at T_{amb}= -55°C	4.99			V
		at T_{amb}= 25°C	4.99	5		V
		at T_{amb}= 125°C	4.95			V
		V_{DD}= 10V				
		at T_{amb}= -55°C	9.99			V
		at T_{amb}= 25°C	9.99	10		V
		at T_{amb}= 125°C	9.95			V
V_{OL}	Output low voltage	I_o = 0				
		V_{DD}= 5V or 10V				
		at T_{amb}= -55°C			0.01	V
		at T_{amb}= 25°C		0	0.01	V
		at T_{amb}= 125°C			0.05	V
→ V_{NH}	Noise immunity	V_{DD}= 5V V_o = 0.95V				
		at T_{amb}= -55°C	1.4			V
		at T_{amb}= 25°C	1.5	2.25		V
		at T_{amb}= 125°C	1.5			V
		V_{DD}= 10V V_o = 2.9V				
		at T_{amb}= -55°C	2.9			V
		at T_{amb}= 25°C	3	4.5		V
		at T_{amb}= 125°C	3			V

* Obtained with test circuit of fig. 11

STATIC ELECTRICAL CHARACTERISTICS (continued)

	Parameter		Test conditions	Min.	Typ.	Max.	Unit
→	V_{NL}	Noise immunity	V_{DD}= 5V V_o = 3.6V				
			at T_{amb}= -55°C	1.5			V
			at T_{amb}= 25°C	1.5	2.25		V
			at T_{amb}= 125°C	1.4			V
			V_{DD}= 10V V_o = 7.2V				
			at T_{amb}= -55°C	3			V
			at T_{amb}= 25°C	3	4.5		V
			at T_{amb}= 125°C	2.9			V
	I_DN	Output drive current N-channel	V_{DD}= 5V V_o = 0.4V				
			at T_{amb}= -55°C	0.75			mA
			at T_{amb}= 25°C	0.6	1		mA
			at T_{amb}= 125°C	0.4			mA
			V_{DD}= 10V V_o = 0.5V				
			at T_{amb}= -55°C	1.6			mA
			at T_{amb}= 25°C	1.3	2.5		mA
			at T_{amb}= 125°C	0.95			mA
→	I_DP	Output drive current P-channel	V_{DD}= 5V V_o = 2.5V				
			at T_{amb}= -55°C	-1.75			mA
			at T_{amb}= 25°C	-1.4	-4		mA
			at T_{amb}= 125°C	-1			mA
			V_{DD}= 10V V_o = 9.5V				
			at T_{amb}= -55°C	-1.35			mA
			at T_{amb}= 25°C	-1.1	-2.5		mA
			at T_{amb}= 125°C	-0.75			mA
	I_i	Input current	T_{amb} = 25°C		10		pA

HBF types (standard temperature range)

I_L*	Quiescent current	V_{DD}= 5V				
		at T_{amb}= -40°C			0.5	μA
		at T_{amb}= 25°C		0.005	0.5	μA
		at T_{amb}= 85°C			15	μA
		V_{DD}= 10V				
		at T_{amb}= -40°C			1	μA
		at T_{amb}= 25°C		0.005	1	μA
		at T_{amb}= 85°C			30	μA

STATIC ELECTRICAL CHARACTERISTICS (continued)

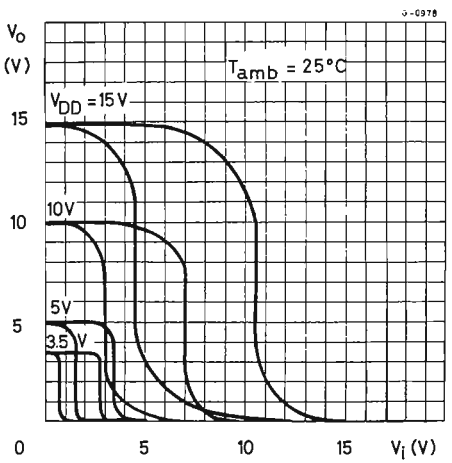
	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OH}	Output high voltage	$I_o = 0$				
		$V_{DD} = 5V$				
		at $T_{amb} = -40°C$	4.99			V
		at $T_{amb} = 25°C$	4.99	5		V
		at $T_{amb} = 85°C$	4.95			V
		$V_{DD} = 10V$				
		at $T_{amb} = -40°C$	9.99			V
		at $T_{amb} = 25°C$	9.99	10		V
		at $T_{amb} = 85°C$	9.95			V
V_{OL}	Output low voltage	$I_o = 0$				
		$V_{DD} = 5V$ or 10V				
		at $T_{amb} = -40°C$			0.01	V
		at $T_{amb} = 25°C$		0	0.01	V
		at $T_{amb} = 85°C$			0.05	V
→ V_{NH}	Noise immunity	$V_{DD} = 5V$ $V_o = 0.95V$				
		at $T_{amb} = -40°C$	1.4			V
		at $T_{amb} = 25°C$	1.5	2.25		V
		at $T_{amb} = 85°C$	1.5			V
		$V_{DD} = 10V$ $V_o = 2.9V$				
		at $T_{amb} = -40°C$	2.9			V
		at $T_{amb} = 25°C$	3	4.5		V
		at $T_{amb} = 85°C$	3			V
→ V_{NL}	Noise immunity	$V_{DD} = 5V$ $V_o = 3.6V$				
		at $T_{amb} = -40°C$	1.5			V
		at $T_{amb} = 25°C$	1.5	2.25		V
		at $T_{amb} = 85°C$	1.4			V
		$V_{DD} = 10V$ $V_o = 7.2V$				
		at $T_{amb} = -40°C$	3			V
		at $T_{amb} = 25°C$	3	4.5		V
		at $T_{amb} = 85°C$	2.9			V
I_DN	Output drive current N-channel	$V_{DD} = 5V$ $V_o = 0.4V$				
		at $T_{amb} = -40°C$	0.35			mA
		at $T_{amb} = 25°C$	0.3	1		mA
		at $T_{amb} = 85°C$	0.24			mA

STATIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_DN	Output drive current N-channel	V_{DD}= 10V V_o = 0.5V				
		at T_{amb}= -40°C	1.2			mA
		at T_{amb}= 25°C	1		2.5	mA
		at T_{amb}= 85°C	0.8			mA
I_DP	Output drive current P-channel	V_{DD}= 5V V_o = 2.5V				
		at T_{amb}= -40°C	-1.3			mA
		at T_{amb}= 25°C	-1.1		-4	mA
		at T_{amb}= 85°C	-0.9			mA
		V_{DD}= 10V V_o = 9.5V				
		at T_{amb}= -40°C	-0.65			mA
		at T_{amb}= 25°C	-0.55		-2.5	mA
		at T_{amb}= 85°C	-0.45			mA
I_i	Input current	T_{amb} = 25°C		10		pA

* Obtained with test circuit of fig. 11

Fig. 1 - Minimum and maximum voltage transfer characteristic curves and test circuit



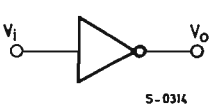
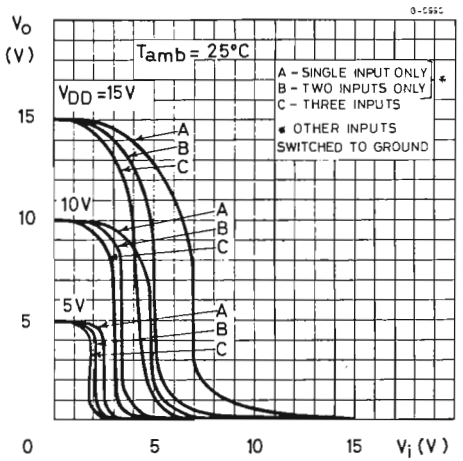


Fig. 2 - Typical voltage transfer characteristic curves and test circuit for NOR gate



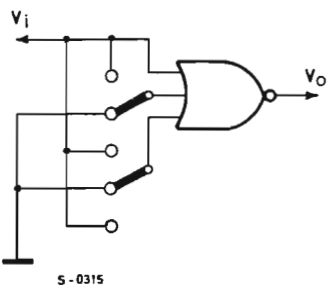
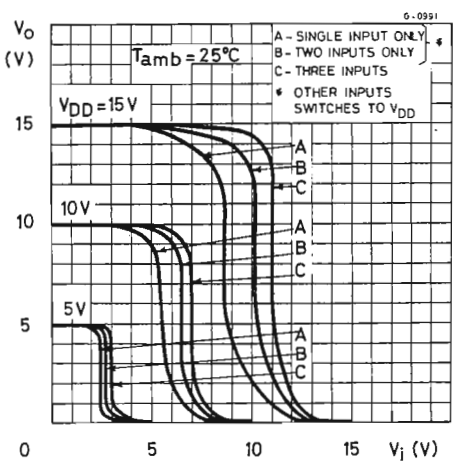


Fig. 3 - Typical voltage transfer characteristic curves and test circuit for NAND gate



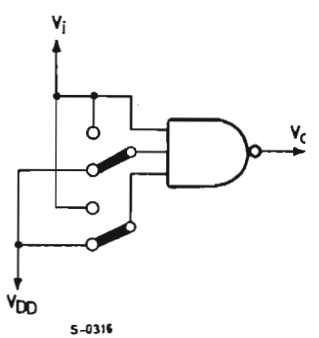
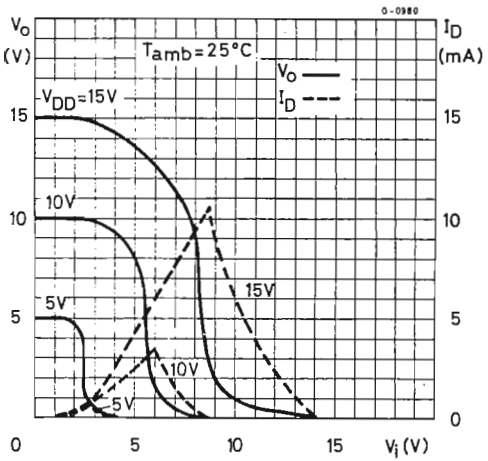


Fig. 4 - Typical current and voltage transfer characteristic curves and test circuit for inverter



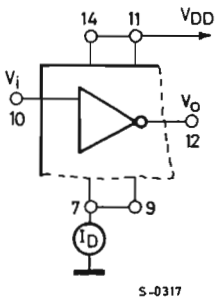


Fig. 5 - Typical voltage transfer characteristics versus ambient temperature

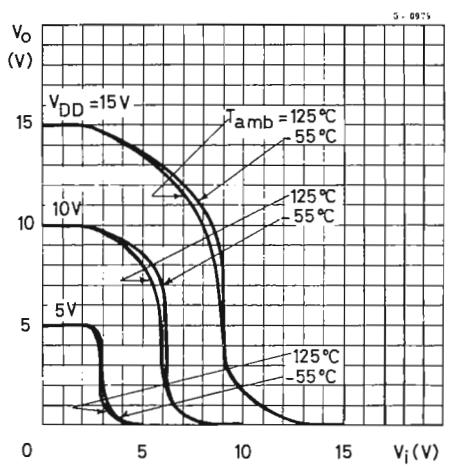


Fig. 6 - Typical power dissipation characteristics

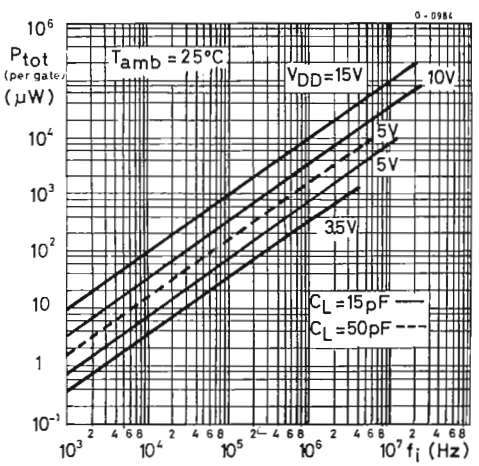


Fig. 7 - Typical N-channel drain characteristic curves and test circuit.

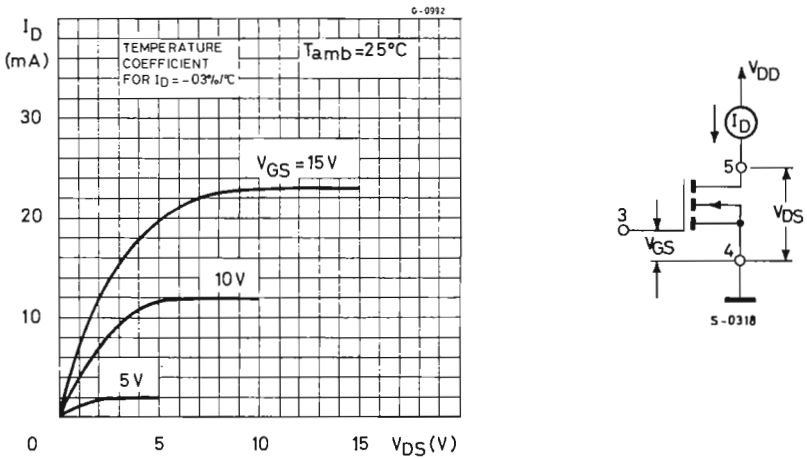


Fig. 8 - Typical P- channel drain characteristic curves and test circuit.

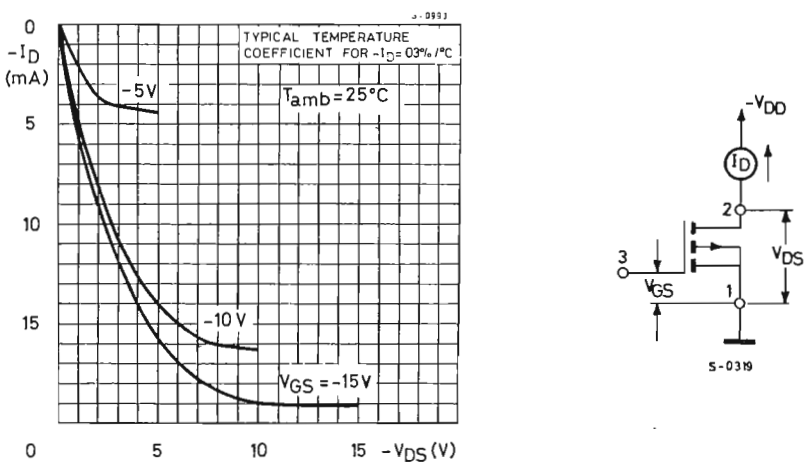


Fig. 9 - Minimum N-channel drain characteristics

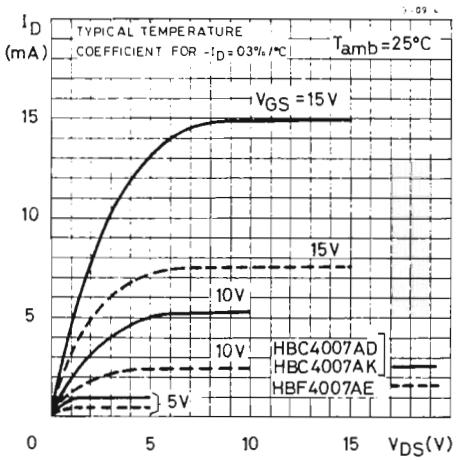


Fig. 10 - Minimum P-channel drain characteristics

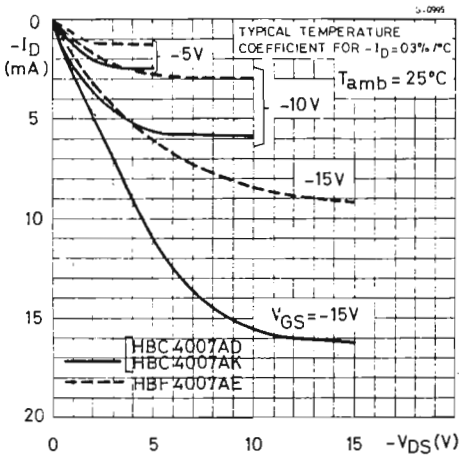
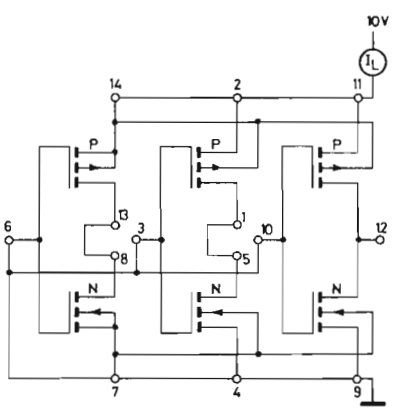


Fig. 11- Quiescent device current test circuit



DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 15 pF, typical temperature coefficient for all V_{DD} = 0.3%/°C values)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
t_{PLH}	Propagation delay time (low to high level)	V_{DD} = 5V				
		for **HBC** types		35	60	ns
		for **HBF** types		35	75	ns
		V_{DD} = 10V				
		for **HBC** types		20	40	ns
		for **HBF** types		20	50	ns
t_{PHL}	Propagation delay time (high to low level)	V_{DD} = 5V				
		for **HBC** types		35	60	ns
		for **HBF** types		35	75	ns
		V_{DD} = 10V				
		for **HBC** types		20	40	ns
		for **HBF** types		20	50	ns
t_{TLH}	Transition time (low to high level)	V_{DD} = 5V				
		for **HBC** types		50	75	ns
		for **HBF** types		50	100	ns
		V_{DD} = 10V				
		for **HBC** types		30	40	ns
		for **HBF** types		30	50	ns
t_{THL}	Transition time (high to low level)	V_{DD}= 5V				
		for **HBC** types		50	75	ns
		for **HBF** types		50	100	ns
		V_{DD} = 10V				
		for **HBC** types		30	40	ns
		for **HBF** types		30	50	ns
C_I	Input capacitance	Any input for **HBC** and **HBF** types		5		pF

Fig. 12- Maximum propagation delay time versus V_{DD}

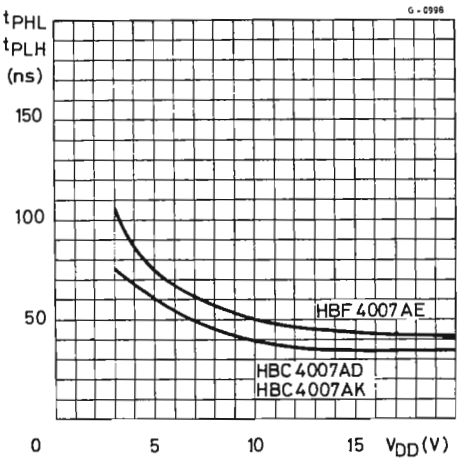
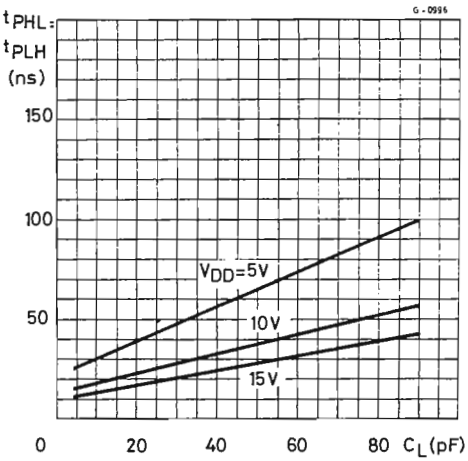


Fig. 13- Typical propagation delay time versus C_L



TYPICAL APPLICATIONS

Numbers shown in parentheses indicate pins that are connected together to form the various configurations listed.

Fig. 14- Triple inverters. (14, 2, 11); (8, 13); (1, 5); (4, 7, 9)

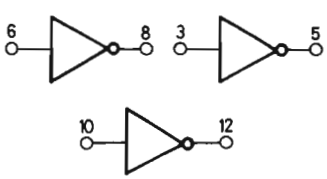


Fig. 15- 3-input NOR gate. (13, 2); (1, 11); (12, 5, 8); (7, 4, 9).

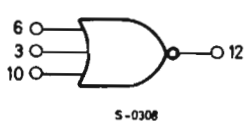


Fig. 16- 3-input NAND gate. (1, 12, 13); (2, 14, 11); (4, 8); (5, 9)

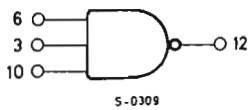


Fig. 17- High sink-current driver. (6, 3, 10); (8, 5, 12); (11, 14); (7, 4, 9)

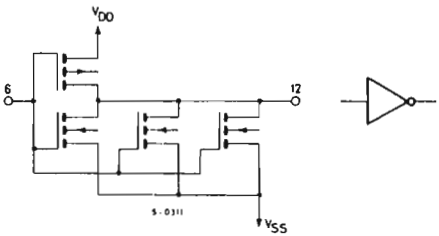


Fig. 18- High source-current driver. (6, 3, 10); (13, 1, 12); (14, 2, 11); (7, 9)

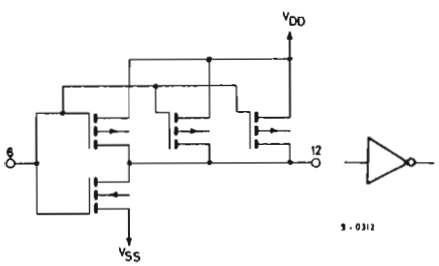


Fig. 19- High sink-and source-current driver. (6, 3, 10); (14, 2, 11); (7, 4, 9); (13, 8, 1, 5, 12)

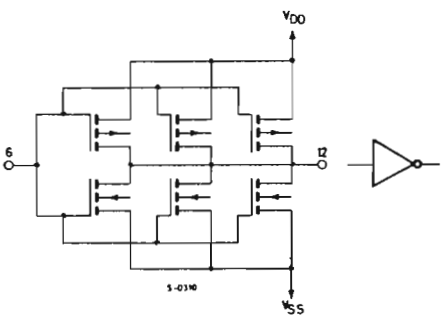
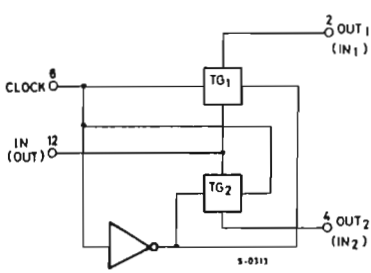


Fig. 20- Dual bi-directional transmission gating. (1, 5, 12); (2, 9); (11, 4); (8, 13, 10); (6, 3)



COS/MOS INTEGRATED CIRCUIT

HBC/HBF 4008A

PRELIMINARY DATA

FOUR-BIT FULL ADDER WITH PARALLEL CARRY OUTPUT

- LOW QUIESCENT POWER DISSIPATION
- WIDE SUPPLY VOLTAGE RANGE: 3 to 15V
- HIGH NOISE IMMUNITY: 45% of V_{DD} (TYP.)
- HIGH SPEED OPERATION
- INPUTS FULLY PROTECTED
- LOW OUTPUT IMPEDANCE
- HIGH FANOUT
- MSI COMPLEXITY on a SINGLE CHIP 4 SUM OUTPUTS PLUS PARALLEL CARRY OUTPUT
- CARRY-INPUT to CARRY-OUTPUT DELAY, t_{PHL}, t_{PLH} = 45 ns at C_L = 15 pF

The **HBC 4008A** (extended temperature range) and **HBF 4008A** (standard temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package. They consist of four full-adder stages with fast look-ahead carry provision from stage to stage. Circuitry is included to provide a fast "parallel-carry-output" bit to permit high-speed operation in arithmetic sections using several **HBC/HBF 4008A** inputs include the four sets of bits to be added, A_1 to A_4 and B_1 to B_4, in addition to the "carry input" bit from a previous section. **HBC/HBF 4008A** outputs include the four sum bits, S_1 and S_4, in addition to the high-speed "parallel-carry-output" which may be utilized at a succeeding **HBC/HBF 4008A** section.

ABSOLUTE MAXIMUM RATINGS

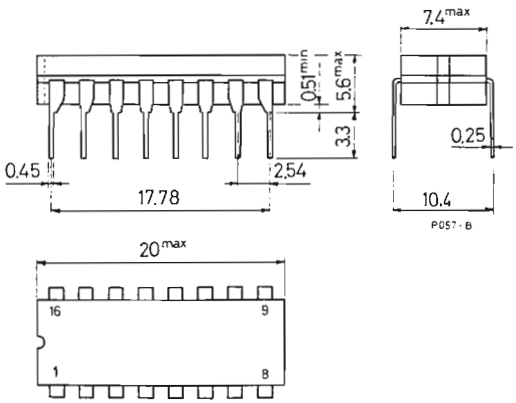
$V_{DD}-V_{SS}$	Supply voltage	-0.5 to 15	V
V_I	Input voltage (at any pin)	$V_{SS} \leqslant V_i \leqslant V_{DD}$	
P_{tot}	Total power dissipation (per package)	200	mW
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature: for **HBC** types	-55 to 125	°C
	for **HBF** types	-40 to 85	°C

ORDERING NUMBERS :

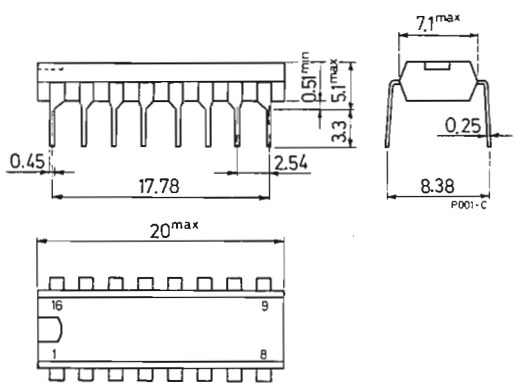
HBC 4008 AD for dual in-line ceramic package
HBC 4008 AF for dual in-line ceramic package, frit seal (extended temperature range)
HBC 4008 AK for ceramic flat package
HBF 4008 AE for dual in-line plastic package
HBF 4008 AF for dual in-line ceramic package, frit seal (standard temperature range)

MECHANICAL DATA (dimensions in mm)

Dual in-line ceramic package
for HBC 4008 AD and
HBC/HBF 4008 AF

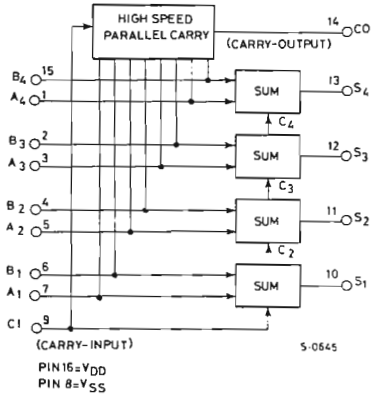


Dual in-line plastic package
for HBF 4008 AE



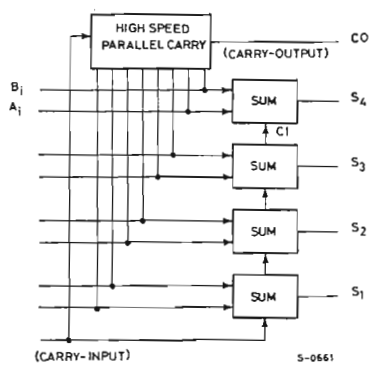
Ceramic flat package for HBC 4008 AK

CONNECTION DIAGRAM AND TRUTH TABLE

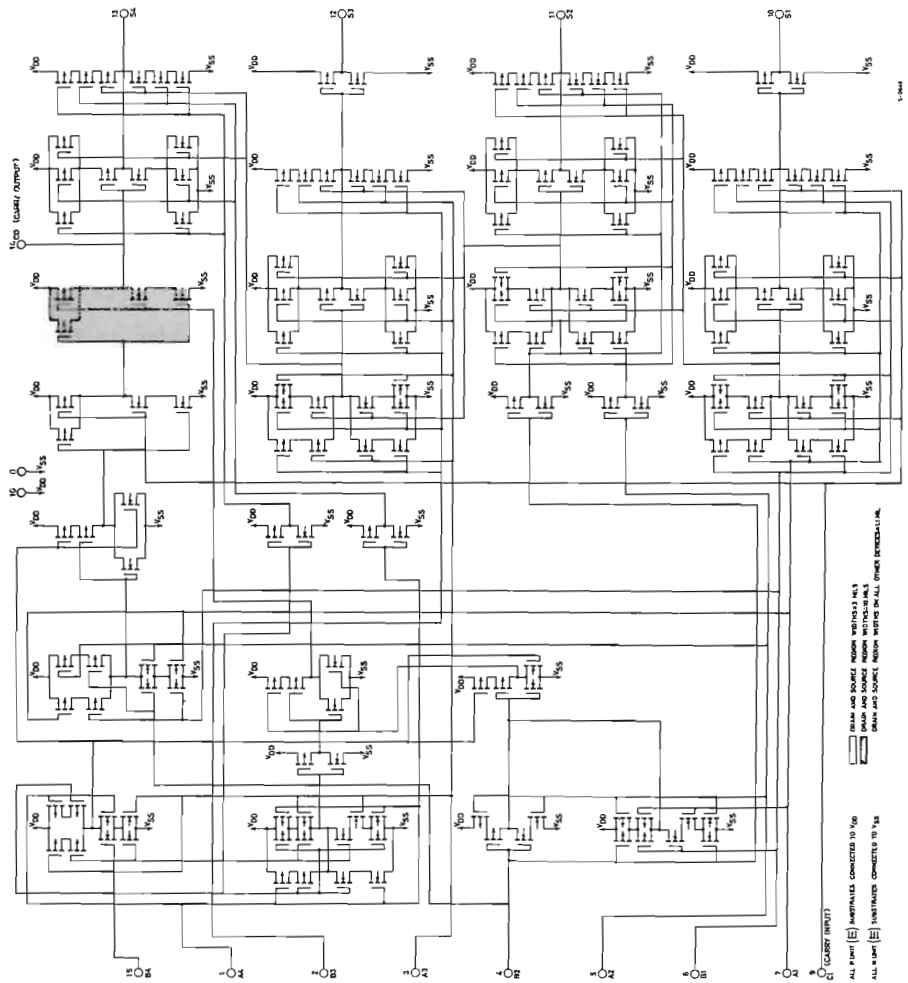


A_i	B_i	CI	CO	SUM
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

LOGIC DIAGRAM



SCHEMATIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage	3 to 15	V
V_I*	Input voltage	V_{DD} to V_{SS}	
T_{op}	Operating temperature : for **HBC** types	-55 to 125	°C
	for **HBF** types	-40 to 85	°C

*This is measured with respect to the V_{SS} pin voltage

STATIC ELECTRICAL CHARACTERISTICS

Parameter	Test conditions	Min.	Typ.	Max.	Unit
HBC types (extended temperature range)					
I_L Quiescent current	V_{DD} = 5V				
	at T_{amb} = -55°C			5	μA
	at T_{amb} = 25°C		0.3	5	μA
	at T_{amb} = 125°C			300	μA
	V_{DD} = 10V				
	at T_{amb} = -55°C			10	μA
	at T_{amb} = 25°C		0.5	10	μA
	at T_{amb} = 125°C			600	μA
V_{OH} Output high voltage	V_{DD} = 5V				
	at T_{amb} = -55°C	4.99			V
	at T_{amb} = 25°C	4.99	5		V
	at T_{amb} = 125°C	4.95			V
	V_{DD} = 10V				
	at T_{amb} = -55°C	9.99			V
	at T_{amb} = 25°C	9.99	10		V
	at T_{amb} = 125°C	9.95			V
V_{OL} Output low voltage	V_{DD} = 5V or 10V				
	at T_{amb} = -55°C			0.01	V
	at T_{amb} = 25°C		0	0.01	V
	at T_{amb} = 125°C			0.05	V

STATIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{NH}	Noise immunity	V_{DD}=5V				
		at T_{amb} = -55°C	1.4			V
		at T_{amb} = 25°C	1.5	2.25		V
		at T_{amb} = 125°C	1.5			V
		V_{DD}=10V				
		at T_{amb} = -55°C	2.9			V
		at T_{amb} = 25°C	3	4.5		V
		at T_{amb} = 125°C	3			V
V_{NL}	Noise immunity	V_{DD}=5V				
		at T_{amb} = -55°C	1.5			V
		at T_{amb} = 25°C	1.5	2.25		V
		at T_{amb} = 125°C	1.4			V
		V_{DD}=10V				
		at T_{amb} = -55°C	3			V
		at T_{amb} = 25°C	3		4.5	V
		at T_{amb} = 125°C	2.9			V
I_DN	Output drive current N - channel	Sum output				
		V_{DD}=5V V_o = 3V				
		at T_{amb} = -55°C	0.012			mA
		at T_{amb} = 25°C	0.01	0.02		mA
		at T_{amb} = 125°C	0.007			mA
		V_{DD}=10V V_o = 3V				
		at T_{amb} = -55°C	0.31			mA
		at T_{amb} = 25°C	0.25	0.5		mA
		at T_{amb} = 125°C	0.175			mA
		Carry output				
		V_{DD}=5V V_o = 0.5V				
		at T_{amb} = -55°C	0.31			mA
		at T_{amb} = 25°C	0.25	0.5		mA
		at T_{amb} = 125°C	0.175			mA
		V_{DD}=10V V_o = 0.5V				
		at T_{amb} = -55°C	0.93			mA
		at T_{amb} = 25°C	0.75	1.5		mA
		at T_{amb} = 125°C	0.53			mA

STATIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_DP	Output drive current P - channel	Sum output				
		V_{DD}=5V V_o = 2V				
		at T_{amb} = -55°C		-0.012		mA
		at T_{amb} = 25°C		-0.01	-0.02	mA
		at T_{amb} = 125°C		-0.007		mA
		V_{DD}=10V V_o = 7V				
		at T_{amb} = -55°C		-0.185		mA
		at T_{amb} = 25°C		-0.15	-0.3	mA
		at T_{amb} = 125°C		-0.105		mA
		Carry output				
		V_{DD}=5V V_o = 4.5V				
		at T_{amb} = -55°C		-0.31		mA
		at T_{amb} = 25°C		-0.25	-0.5	mA
		at T_{amb} = 125°C		-0.175		mA
		V_{DD}=10V V_o = 9.5V				
		at T_{amb} = -55°C		-0.93		mA
		at T_{amb} = 25°C		-0.75	-1.5	mA
		at T_{amb} = 125°C		-0.53		mA
I_i	Input current	T_{amb} = 25°C		10		pA

HBF types (standard temperature range)

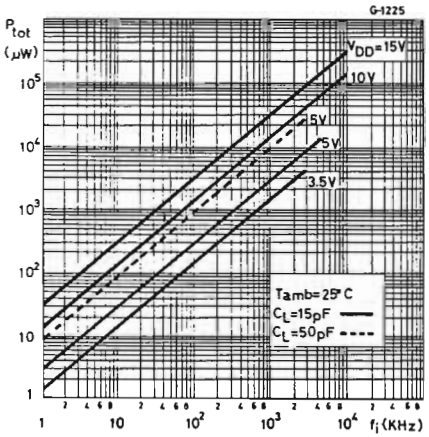
I_L	Quiescent current	V_{DD} = 5V				
		at T_{amb} = -40°C			50	μA
		at T_{amb} = 25°C		0.5	50	μA
		at T_{amb} = 85°C			700	μA
		V_{DD} = 10V				
		at T_{amb} = -40°C			100	μA
		at T_{amb} = 25°C		1	100	μA
		at T_{amb} = 85°C			1400	μA
V_{OH}	Output high voltage	I_o = 0				
		V_{DD} = 5V				
		at T_{amb} = -40°C	4.99			V
		at T_{amb} = 25°C	4.99	5		V
		at T_{amb} = 85°C	4.95			V

STATIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{OH}	Output high voltage	V_{DD} = 10V				
		at T_{amb} = -40°C	9.99			V
		at T_{amb} = 25°C	9.99	10		V
		at T_{amb} = 85°C	9.95			V
V_{OL}	Output low voltage	V_{DD} = 5V or 10V				
		at T_{amb} = -40°C			0.01	V
		at T_{amb} = 25°C		0	0.01	V
		at T_{amb} = 85°C			0.05	V
V_{NH}	Noise immunity	V_{DD}=5V				
		at T_{amb} = -40°C	1.4			V
		at T_{amb} = 25°C	1.5	2.25		V
		at T_{amb} = 85°C	1.5			V
		V_{DD}=10V				
		at T_{amb} = -40°C	2.9			V
		at T_{amb} = 25°C	3		4.5	V
		at T_{amb} = 85°C	3			V
V_{NL}	Noise immunity	V_{DD}=5V				
		at T_{amb} = -40°C	1.5			V
		at T_{amb} = 25°C	1.5	2.25		V
		at T_{amb} = 85°C	1.4			V
		V_{DD}=10V				
		at T_{amb} = -40°C	3			V
		at T_{amb} = 25°C	3		4.5	V
		at T_{amb} = 85°C	2.9			V
I_DN	Output drive current N - channel	Sum output				
		V_{DD}=5V V_o = 3V				
		at T_{amb} = -40°C	0.0085			mA
		at T_{amb} = 25°C	0.007	0.02		mA
		at T_{amb} = 85°C	0.005			mA

STATIC ELECTRICAL CHARACTERISTICS (continued)

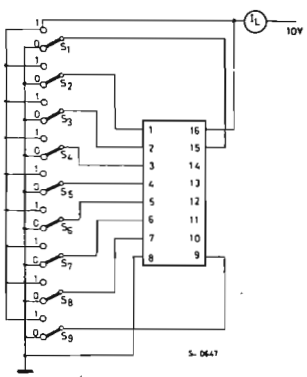
Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_DN	Output drive current N - channel	Sum output				
		V_{DD}=10V V_o = 3V				
		at T_{amb} = -40°C	0.24			mA
		at T_{amb} = 25°C	0.2		0.5	mA
		at T_{amb} = 85°C	0.16			mA
		Carry output				
		V_{DD}=5V V_o = 0.5V				
		at T_{amb} = -40°C	0.155			mA
		at T_{amb} = 25°C	0.13		0.5	mA
		at T_{amb} = 85°C	0.105			mA
		V_{DD}=10V V_o = 0.5V				
		at T_{amb} = -40°C	0.6			mA
		at T_{amb} = 25°C	0.5		1.5	mA
		at T_{amb} = 85°C	0.4			mA
I_DP	Output drive current P - channel	Sum output				
		V_{DD}=5V V_o = 2V				
		at T_{amb} = -40°C	-0.008			mA
		at T_{amb} = 25°C	-0.007		-0.02	mA
		at T_{amb} = 85°C	-0.005			mA
		V_{DD}=10V V_o = 7V				
		at T_{amb} = -40°C	-0.12			mA
		at T_{amb} = 25°C	-0.1		-0.3	mA
		at T_{amb} = 85°C	-0.08			mA
		Carry output				
		V_{DD}= 5V V_o = 4.5V				
		at T_{amb} = -40°C	-0.155			mA
		at T_{amb} = 25°C	-0.13		-0.5	mA
		at T_{amb} = 85°C	-0.105			mA
		V_{DD}=10V V_o = 9.5V				
		at T_{amb} = -40°C	-0.6			mA
		at T_{amb} = 25°C	-0.5		-1.5	mA
		at T_{amb} = 85°C	-0.4			mA
I_i	Input current	T_{amb} = 25°C		10		pA



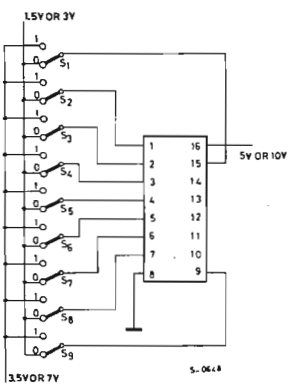
Typical power dissipation characteristics

TEST CIRCUITS

Quiescent device current



Noise immunity



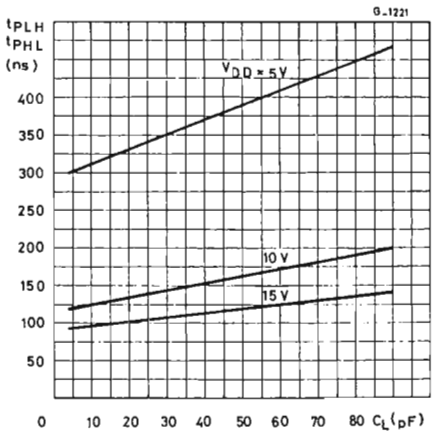
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}=25°C, C_L = 15 pF, typical temperature coefficient for all V_{DD}= 0.3%/°C values, all input rise and fall time = 20 ns)

Parameter	Test conditions	Min. Typ. Max.	Unit
C_i Input capacitance	Any input for **HBC** and **HBF** types	10	pF

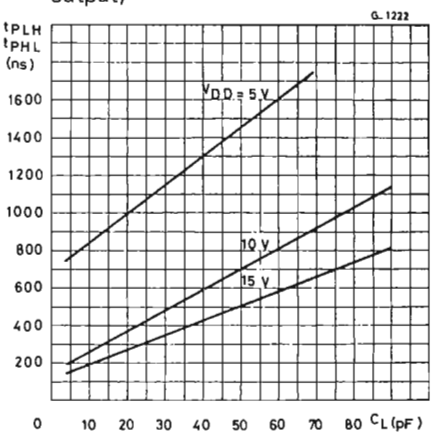
DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
SUM OUTPUTS					
t_{PLH}, t_{PHL} Propagation delay time	Sum input and carry input				
	V_{DD} = 5V				
	for **HBC** types		900	1300	ns
	for **HBF** types		900	2000	ns
	V_{DD} = 10V				
	for **HBC** types		325	500	ns
	for **HBF** types		325	650	ns
t_{TLH}, t_{THL} Transition time	V_{DD} = 5V				
	for **HBC** types		1250	2200	ns
	for **HBF** types		1250	2900	ns
	V_{DD} = 10V				
	for **HBC** types		550	900	ns
	for **HBF** types		550	1100	ns
CARRY OUTPUT					
t_{PLH}, t_{PHL} Propagation delay time	Sum input				
	V_{DD} = 5V				
	for **HBC** types		320	600	ns
	for **HBF** types		320	800	ns
	V_{DD} = 10V				
	for **HBC** types		120	200	ns
	for **HBF** types		120	240	ns
	Carry input				
	V_{DD} = 5V				
	for **HBC** types		100	175	ns
	for **HBF** types		100	200	ns
	V_{DD} = 10V				
	for **HBC** types		45	75	ns
	for **HBC** types		45	90	ns
t_{TLH}, t_{THL} Transition time	V_{DD} = 5V				
	for **HBC** types		125	225	ns
	for **HBF** types		125	290	ns
	V_{DD} = 10V				
	for **HBC** types		45	75	ns
	for **HBF** types		45	90	ns

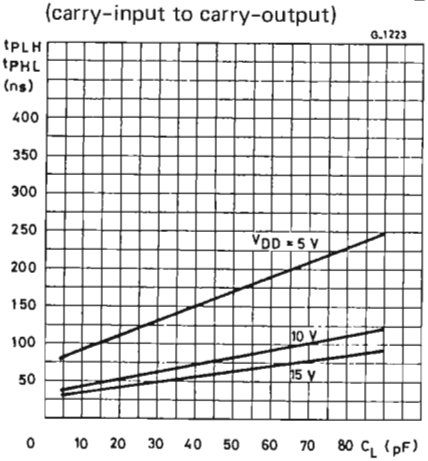
Typical propagation delay time vs. C_L (sum-input to carry-output)



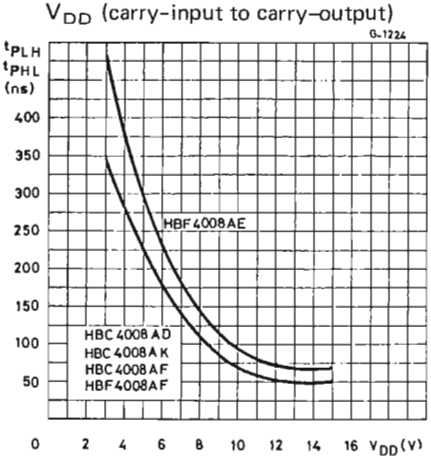
Typical propagation delay time vs. C_L (sum-input or carry-input to sum-output)



Typical propagation delay time vs. C_L (carry-input to carry-output)

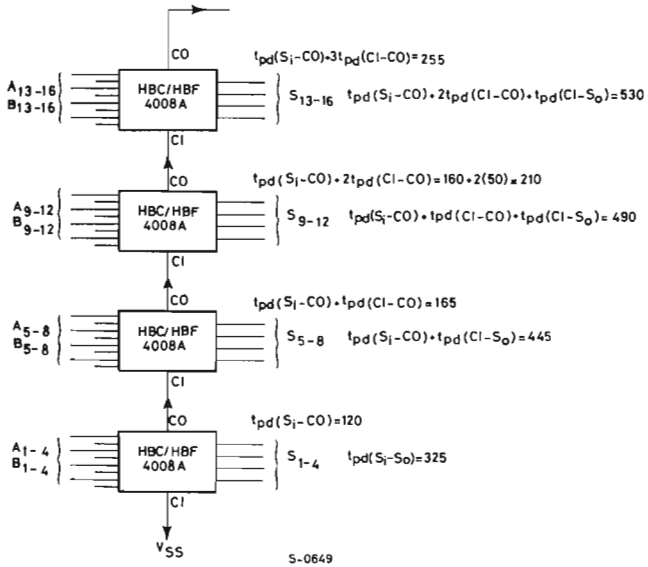


Maximum propagation delay time vs. V_{DD} (carry-input to carry-output)



TYPICAL APPLICATION

Speed characteristics of a 16-bit adder



NOTES: All "A" and "B" input bits occur at t = 0
All sums settled at t = 530 ns.
$C_L = 15$ pF, $T_{amb} = 25°C$, $V_{DD} - V_{SS} = 10V$

COS/MOS INTEGRATED CIRCUITS

PRELIMINARY DATA

HEX BUFFERS/CONVERTERS: INVERTING TYPE HBC / HBF 4009 A
NON-INVERTING TYPE HBC/HBF 4010A

- MEDIUM SPEED OPERATION
- INPUTS FULLY PROTECTED
- HIGH CURRENT SINKING CAPABILITY: 8 mA (MIN.) at V_{OL} = 0.5V and V_{DD} = 10V

The **HBC 4009A, HBC 4010A** (extended temperature range) and **HBF 4009A, HBF 4010A** (standard temperature range) may be used as a COS/MOS to DTL or TTL hex converter or a COS/MOS current driver. Conversion ranges are from COS/MOS logic operating at 3 to 15V supply levels to DTL or TTL logic operating at 3 to 6V supply levels. Conversion to logic output levels greater than 6V is permitted providing V_{CC} (DTL/TTL) $\leqslant V_{DD}$ (COS/MOS). They are available in 16-lead dual in-line plastic or ceramic package and ceramic flat package.

ABSOLUTE MAXIMUM RATINGS

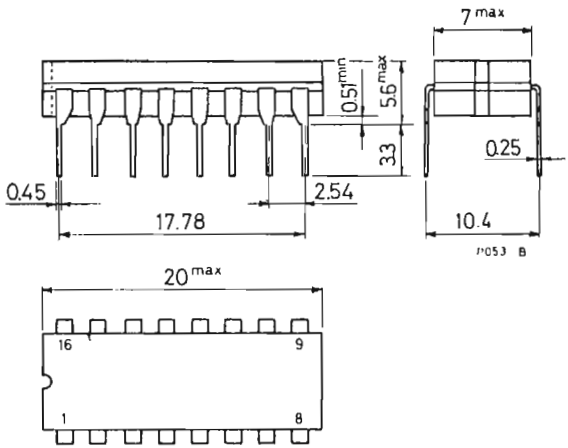
V_{DD}-V_{SS}	Supply voltage	-0.5 to 15	V
V_i	Input voltage (at any pin)	$V_{SS} \leqslant V_i \leqslant V_{DD}$	
P_{tot}	Total power dissipation (per package)	200	mW
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature: for **HBC** types	-55 to 125	°C
	for **HBF** types	-40 to 85	°C

ORDERING NUMBERS:

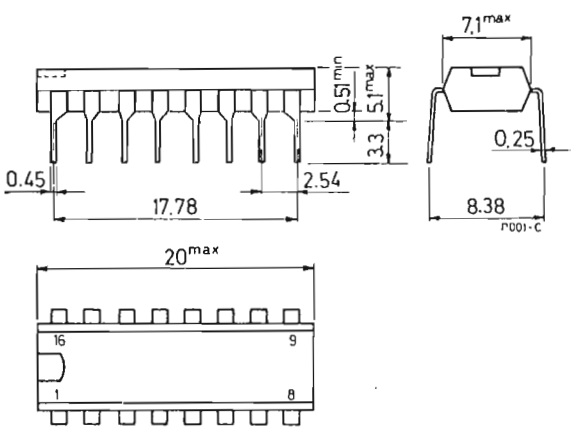
HBC 4XXX AD for dual in-line ceramic package
HBC 4XXX AF for dual in-line ceramic package, frit seal (extended temperature range)
HBC 4XXX AK for ceramic flat package
HBF 4XXX AE for dual in-line plastic package
HBF 4XXX AF for dual in-line ceramic package, frit seal (standard temperature range)

MECHANICAL DATA (dimensions in mm)

Dual in-line ceramic package
for HBC 4 XXX AD and
HBC/HBF 4 XXX AF



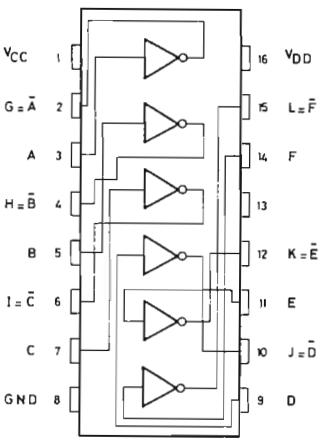
Dual in-line plastic package
for HBF 4 XXX AE types



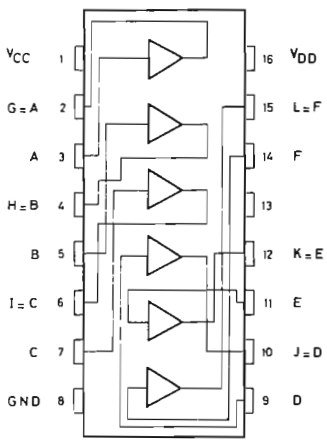
Ceramic flat package for HBC 4 XXX AK types

CONNECTION DIAGRAMS (top view)

for **4009A** type

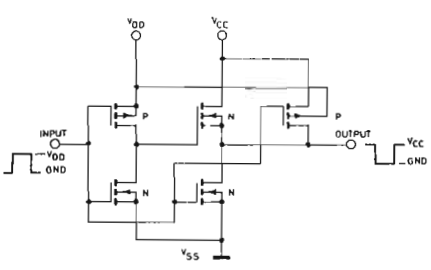


for **4010A** type



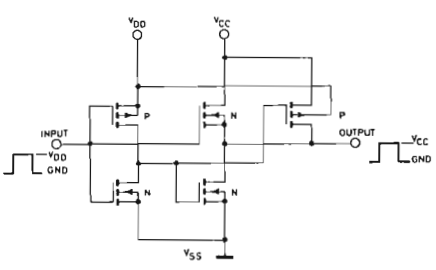
SCHEMATIC DIAGRAMS

for **4009A** type



NOTES :
Configuration – Hex COS/MOS to DTL or TTL converter (inverting).
Wiring schedule – Connect V_{CC} to DTL or TTL supply.
Connect V_{DD} to COS/MOS supply.

for **4010A** type



NOTES :
Configuration – Hex COS/MOS to DTL or TTL converter (non-inverting).
Wiring schedule – Connect V_{CC} to DTL or TTL supply.
Connect V_{DD} to COS/MOS supply.

RECOMMENDED OPERATING CONDITIONS

V_{DD} *	Supply voltage	3 to 15	V
V_i *	Input voltage	V_{DD} to V_{SS}	
T_{op}	Operating temperature :		
	for **HBC** types	-55 to 125	°C
	for **HBF** types	-40 to 85	°C

* This is measured with respect to the V_{SS} pin voltage

CAUTION : V_{CC} VOLTAGE LEVEL MUST BE EQUAL TO OR LESS POSITIVE THAN V_{DD}

STATIC ELECTRICAL CHARACTERISTICS

Parameter	Test conditions	Min.	Typ.	Max.	Unit
HBC types (extended temperature range)					
I_L Quiescent current	V_{DD} = 5V				
	at T_{amb}= -55°C			0.3	µA
	at T_{amb}= 25°C		0.01	0.3	µA
	at T_{amb}= 125°C			20	µA
	V_{DD} = 10V				
	at T_{amb}= -55°C			0.5	µA
	at T_{amb}= 25°C		0.01	0.5	µA
	at T_{amb}= 125°C			30	µA
V_{OH} Output high voltage	I_o = 0				
	V_{DD} = 5V				
	at T_{amb}= -55°C	4.99			V
	at T_{amb}= 25°C	4.99	5		V
	at T_{amb}= 125°C	4.95			V
	V_{DD} = 10V				
	at T_{amb}= -55°C	9.99			V
	at T_{amb}= 25°C	9.99	10		V
	at T_{amb}= 125°C	9.95			V

STATIC ELECTRICAL CHARACTERISTICS (continued)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OL}	Output low voltage	$I_o = 0$ V_{DD}= 5V or 10V				
		at T_{amb}= -55°C			0.01	V
		at T_{amb}= 25°C		0	0.01	V
		at T_{amb}= 125°C			0.05	V
→ V_{NH}	Noise immunity (for **4009A** only)	V_{DD}= 5V V_o= 0.95V				
		at T_{amb}= -55°C	1.4			V
		at T_{amb}= 25°C	1.5	2.25		V
		at T_{amb}= 125°C	1.5			V
		V_{DD}= 10V V_o = 2V				
		at T_{amb}= -55°C	2.9			V
		at T_{amb}= 25°C	3		4.5	V
		at T_{amb}= 125°C	3			V
→ V_{NH}	Noise immunity (for **4010A** only)	V_{DD}= 5V V_o = 3.6V				
		at T_{amb}= -55°C	1.4			V
		at T_{amb}= 25°C	1.5	2.25		V
		at T_{amb}= 125°C	1.5			V
		V_{DD}=10V V_o = 7.2V				
		at T_{amb}= -55°C	2.9			V
		at T_{amb}= 25°C	3		4.5	V
		at T_{amb}= 125°C	3			V
→ V_{NL}	Noise immunity (for **4009A** only)	V_{DD}= 5V V_o = 3.6V				
		at T_{amb}= -55°C	1			V
		at T_{amb}= 25°C	1	2.25		V
		at T_{amb}= 125°C	0.9			V
		V_{DD}=10V V_o = 7.2V				
		at T_{amb}= -55°C	2			V
		at T_{amb}= 25°C	2		4.5	V
		at T_{amb}= 125°C	1.9			V
→ V_{NL}	Noise immunity (for **4010A** only)	V_{DD}= 5V V_o = 0.95V				
		at T_{amb}= -55°C	1.5			V
		at T_{amb}= 25°C	1.5	2.25		V
		at T_{amb}= 125°C	1.4			V
		V_{DD}=10V V_o= 2.9V				
		at T_{amb}= -55°C	3			V
		at T_{amb}= 25°C	3		4.5	V
		at T_{amb}= 125°C	2.9			V

STATIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_DN	Output drive current N-channel	V_{DD}= 5V V_o = 0.4V				
		at T_{amb}= -55°C	3.75			mA
		at T_{amb}= 25°C	3		4	mA
		at T_{amb}= 125°C	2.1			mA
		V_{DD}=10V V_o = 0.5V				
		at T_{amb}= -55°C	10			mA
		at T_{amb}= 25°C	8		10	mA
		at T_{amb}= 125°C	5.6			mA
I_DP	Output drive current P-channel	V_{DD}= 5V V_o = 2.5V				
		at T_{amb}= -55°C	-1.85			mA
		at T_{amb}= 25°C	-1.25		-1.75	mA
		at T_{amb}= 125°C	-0.9			mA
		V_{DD}=10V V_o = 9.5V				
		at T_{amb}= -55°C	-0.9			mA
		at T_{amb}= 25°C	-0.6		-0.8	mA
		at T_{amb}= 125°C	-0.4			mA
I_I	Input current	T_{amb} = 25°C		10		pA

HBF types (standard temperature range)

I_L	Quiescent current	V_{DD}= 5V				
		at T_{amb}= -40°C			3	μA
		at T_{amb}= 25°C		0.03	3	μA
		at T_{amb}= 85°C			42	μA
		V_{DD}=10V				
		at T_{amb}= -40°C			5	μA
		at T_{amb}= 25°C		0.05	5	μA
		at T_{amb}= 85°C			70	μA
V_{OH}	Output high voltage	I_o = 0				
		V_{DD}= 5V				
		at T_{amb}= -40°C	4.99			V
		at T_{amb}= 25°C	4.99		5	V
		at T_{amb}= 85°C	4.95			V
		V_{DD}= 10V				
		at T_{amb}= -40°C	9.99			V
		at T_{amb}= 25°C	9.99		10	V
		at T_{amb}= 85°C	9.95			V

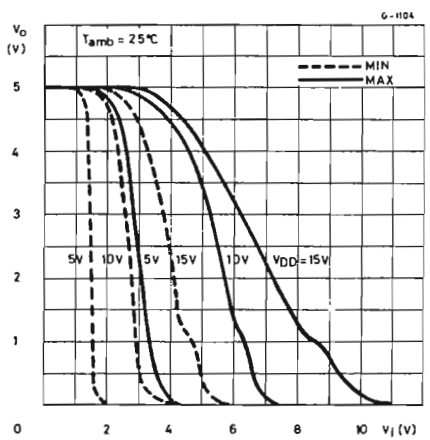
STATIC ELECTRICAL CHARACTERISTICS (continued)

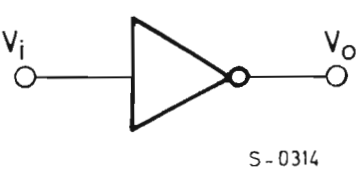
	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OL}	Output low voltage	$I_o = 0$ V_{DD}= 5V or 10V				
		at T_{amb}= -40°C			0.01	V
		at T_{amb}= 25°C		0	0.01	V
		at T_{amb}= 85°C			0.05	V
→ V_{NH}	Noise immunity (for **4009A** only)	V_{DD}= 5V V_o = 0.95V				
		at T_{amb}= -40°C	1.4			V
		at T_{amb}= 25°C	1.5	2.25		V
		at T_{amb}= 85°C	1.5			V
		V_{DD}=10V V_o = 2V				
		at T_{amb}= -40°C	2.9			V
		at T_{amb}= 25°C	3	4.5		V
		at T_{amb}= 85°C	3			V
→ V_{NH}	Noise immunity (for **4010A** only)	V_{DD}= 5V V_o = 3.6V				
		at T_{amb}= -40°C	1.4			V
		at T_{amb}= 25°C	1.5	2.25		V
		at T_{amb}= 85°C	1.5			V
		V_{DD}=10V V_o = 7.2V				
		at T_{amb}= -40°C	2.9			V
		at T_{amb}= 25°C	3	4.5		V
		at T_{amb}= 85°C	3			V
→ V_{NL}	Noise immunity (for **4009 A** only)	V_{DD}= 5V V_o = 3.6V				
		at T_{amb}= -40°C	1			V
		at T_{amb}= 25°C	1	2.25		V
		at T_{amb}= 85°C	0.9			V
		V_{DD}=10V V_o = 7.2V				
		at T_{amb}= -40°C	2			V
		at T_{amb}= 25°C	2	4.5		V
		at T_{amb}= 85°C	1.9			V
→ V_{NL}	Noise immunity (for **4010 A** only)	V_{DD}= 5V V_o = 0.95V				
		at T_{amb}= -40°C	1.5			V
		at T_{amb}= 25°C	1.5	2.25		V
		at T_{amb}= 85°C	1.4			V
		V_{DD}=10V V_o = 2.9V				
		at T_{amb}= -40°C	3			V
		at T_{amb}= 25°C	3	4.5		V
		at T_{amb}= 85°C	2.9			V

STATIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_DN	Output drive current N-channel	V_{DD}= 5V V_o = 0.4V				
		at T_{amb}= -40°C	3.6			mA
		at T_{amb}= 25°C	3		4	mA
		at T_{amb}= 85°C	2.4			mA
		V_{DD}=10V V_o = 0.5V				
		at T_{amb}= -40°C	9.6			mA
		at T_{amb}= 25°C	8		10	mA
		at T_{amb}= 85°C	6.4			mA
I_DP	Output drive current P-channel	V_{DD}= 5V V_o = 2.5V				
		at T_{amb}= -40°C	-1.5			mA
		at T_{amb}= 25°C	-1.25		-1.75	mA
		at T_{amb}= 85°C	-1			mA
		V_{DD}=10V V_o = 9.5V				
		at T_{amb}= -40°C	-0.72			mA
		at T_{amb}= 25°C	-0.6		-0.8	mA
		at T_{amb}= 85°C	-0.48			mA
I_i	Input current	T_{amb} = 25°C		10		pA

Minimum and maximum voltage transfer characteristic curves and test circuit (for **4009 A** only)





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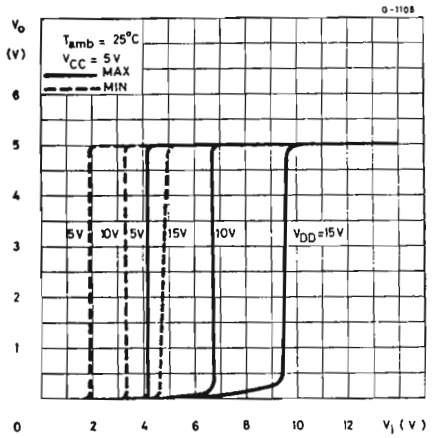
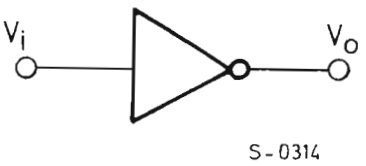
Minimum and maximum voltage transfer characteristic curves and test circuit (for **4010 A** only)





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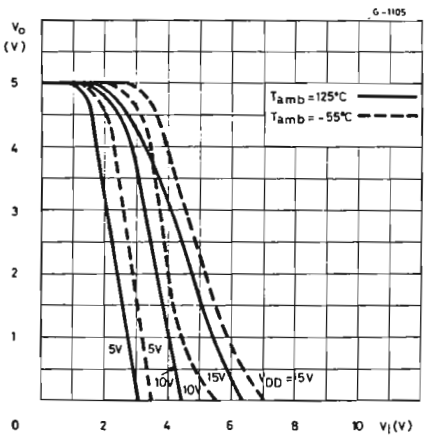
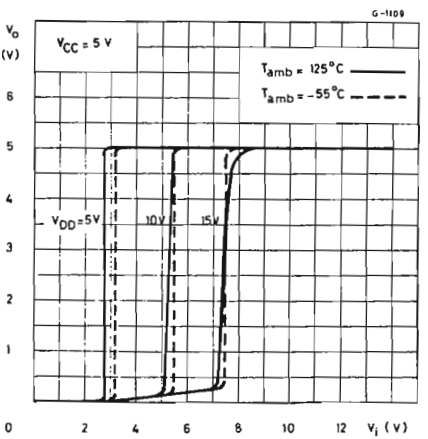
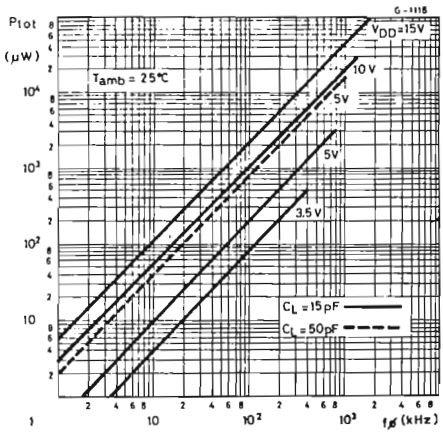
Typical voltage transfer characteristics versus ambient temperature (for **4009A** only)



Typical voltage transfer characteristics versus ambient temperature (for **4010A** only)



Typical power dissipation characteristics



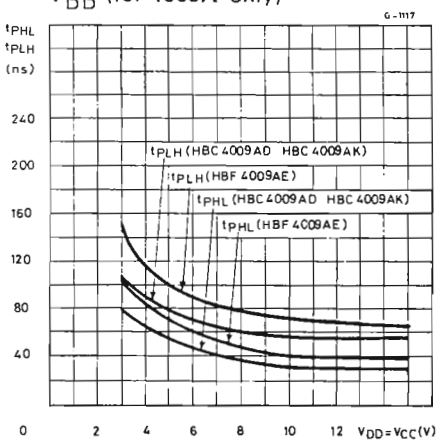
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 15 pF, typical temperature coefficient for all V_{DD} = 0.3%/°C values, and all input rise and fall time = 20 ns)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
t_{PLH}	Propagation delay time (low to high level)	$V_{CC} = V_{DD} = 5V$				
		for **HBC** types		50	80	ns
		for **HBF** types		50	100	ns
		$V_{CC} = V_{DD} = 10V$				
		for **HBC** types		25	55	ns
		for **HBF** types		25	70	ns
		$V_{DD} = 10V$ $V_{CC} = 5V$				
		for **HBC** types		15	30	ns
		for **HBF** types		15	40	ns

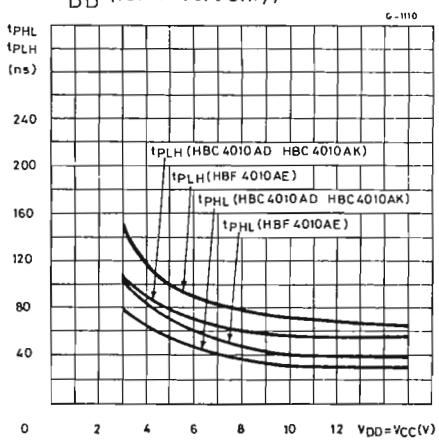
DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

	Parameter		Test conditions	Min.	Typ.	Max.	Unit
→	t_{PHL}	Propagation delay time (high to low level)	$V_{CC} = V_{DD} = 5V$				
			for **HBC** types		15	55	ns
			for **HBF** types		15	70	ns
			$V_{CC} = V_{DD} = 10V$				
			for **HBC** types		10	30	ns
			for **HBF** types		10	40	ns
			$V_{DD} = 10V$ $V_{CC} = 5V$				
			for **HBC** types		10	25	ns
			for **HBF** types		10	35	ns
	t_{TLH}	Transition time (low to high level)	$V_{CC} = V_{DD} = 5V$				
			for **HBC** types		80	125	ns
			for **HBF** types		80	160	ns
			$V_{CC} = V_{DD} = 10V$				
			for **HBC** types		50	100	ns
			for **HBF** types		50	120	ns
	t_{THL}	Transition time (high to low level)	$V_{CC} = V_{DD} = 5V$				
			for **HBC** types		20	45	ns
			for **HBF** types		20	60	ns
			$V_{CC} = V_{DD} = 10V$				
			for **HBC** types		16	40	ns
			for **HBF** types		16	50	ns
→	C_i	Input capacitance (for **4009A** only)	Any input for **HBC** and **HBF** types		15		pF
→	C_i	Input capacitance (for **4010A** only)	Any input for **HBC** and **HBF** types		5		pF

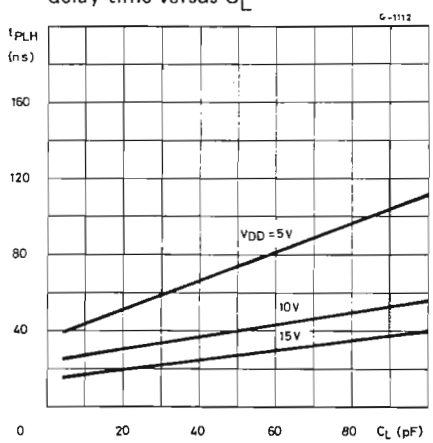
Maximum propagation delay time vs V_{DD} (for **4009A** only)



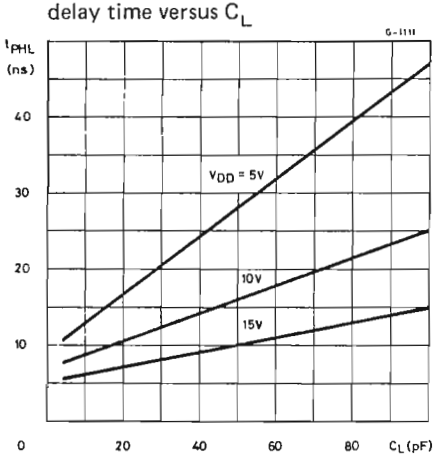
Maximum propagation delay time vs V_{DD} (for **4010A** only)



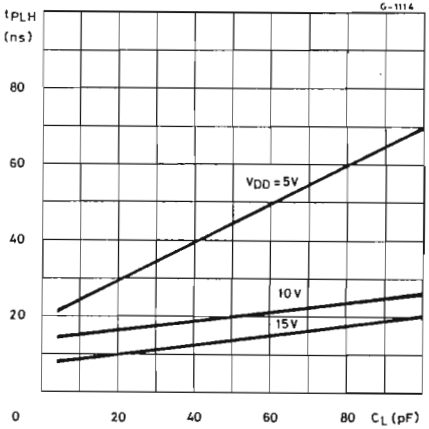
Typical low-to-high level propagation delay time versus C_L



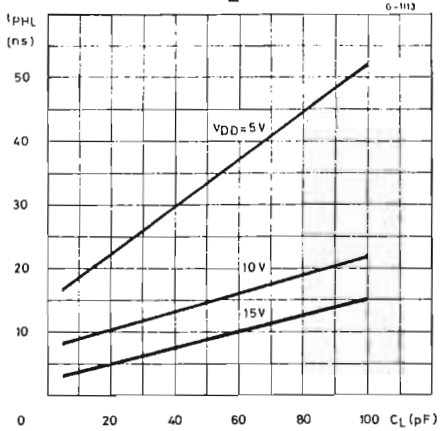
Typical high-to-low level propagation delay time versus C_L



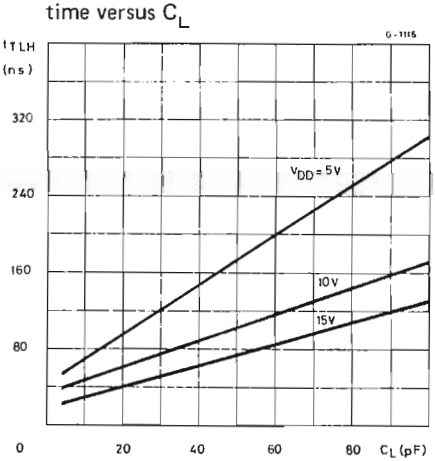
Typical low-to-high level propagation delay time versus C_L (driving TTL, DTL)



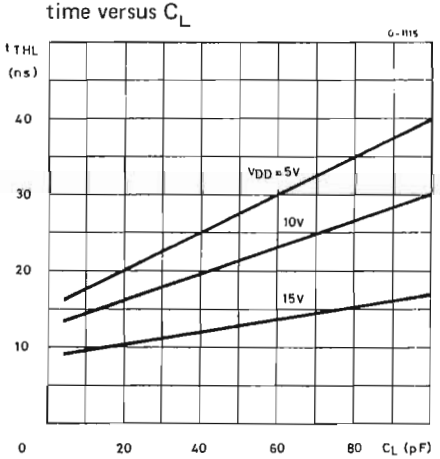
Typical high-to-low level propagation delay time versus C_L (driving TTL, DTL)



Typical low-to-high level transition time versus C_L



Typical- high-to-low level transition time versus C_L



HBC/HBF 4011 A
HBC/HBF 4012 A
HBC/HBF 4023 A

NAND GATES: QUAD 2 INPUT HBC/HBF 4011A
DUAL 4 INPUT HBC/HBF 4012A
TRIPLE 3 INPUT HBC/HBF 4023A

- LOW QUIESCENT POWER DISSIPATION: 10 nW/PACKAGE
- WIDE SUPPLY VOLTAGE RANGE: 3 to 15V
- HIGH NOISE IMMUNITY: 45% of V_{DD} (TYP.)
- MEDIUM SPEED OPERATION: $t_{PHL} = t_{PLH} = 25$ ns (TYP.) at $C_L = 15$ pF
- INPUTS FULLY PROTECTED
- LOW "1" and "0" OUTPUT LEVEL IMPEDANCE: 400Ω and 800Ω (TYP.) RESPECTIVELY at $V_{DD} - V_{SS} = 10V$
- HIGH FANOUT : > 50

The **HBC 4011A, HBC 4012A, HBC 4023A** (extended temperature range) and **HBF 4011A, HBF 4012A, HBF 4023A** (standard temperature range) NAND gates are constructed with MOS P-channel and N-channel enhancement mode device in a single monolithic chip. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.
They are available in 14-lead dual in-line plastic or ceramic package and ceramic flat package.

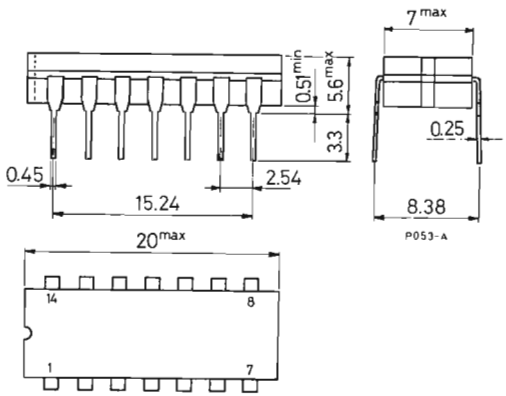
ABSOLUTE MAXIMUM RATINGS

$V_{DD}-V_{SS}$	Supply voltage	-0.5 to 15	V
V_i	Input voltage (at any pin)	$V_{SS} \leqslant V_i \leqslant V_{DD}$	
P_{tot}	Total power dissipation (per package)	200	mW
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature :		
	for HBC types	-55 to 125	°C
	for HBF types	-40 to 85	°C

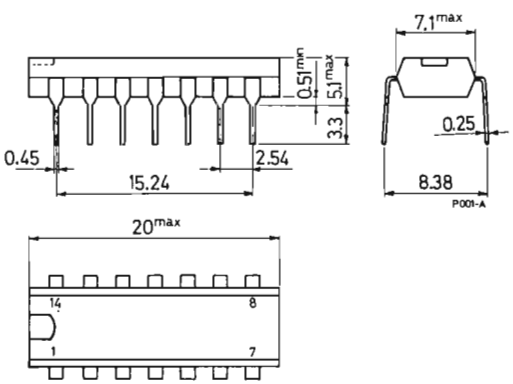
ORDERING NUMBERS:
HBC 4 XXX AD for dual in-line ceramic package
HBC 4 XXX AF for dual in-line ceramic package frit seal (extended temperature range)
HBC 4 XXX AK for ceramic flat package
HBF 4 XXX AE for dual in-line plastic package
HBF 4 XXX AF for dual in-line ceramic package frit seal (standard temperature range)

MECHANICAL DATA (dimensions in mm)

Dual in-line ceramic package
for HBC 4 XXX AD and
HBC/HBF 4 XXX AF



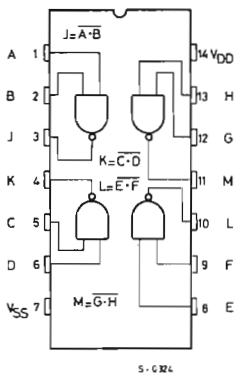
Dual in-line plastic package
(similar to TO-116)
for HBF 4 XXX AE



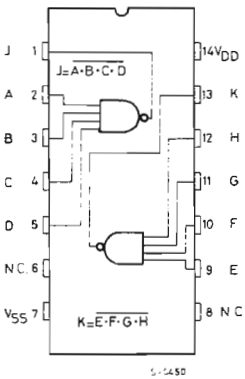
Ceramic flat package for HBC 4 XXX AK

CONNECTION DIAGRAMS

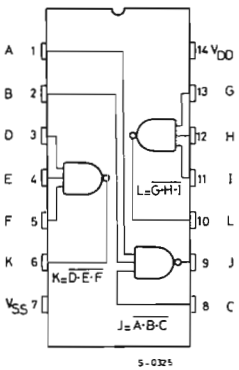
(top view)



for **4011A**



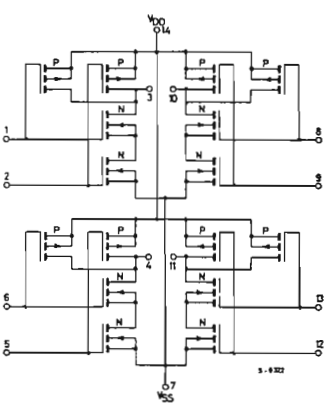
for **4012A**



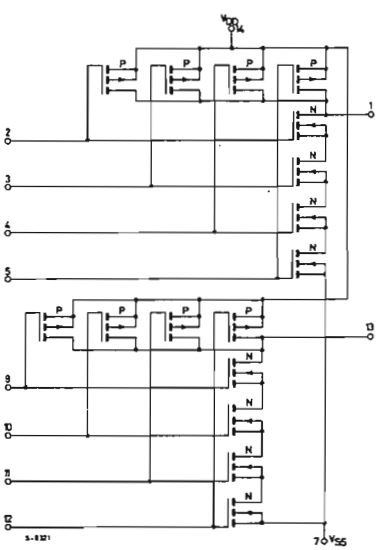
for **4023A**

SCHEMATIC DIAGRAMS

for **4011A**

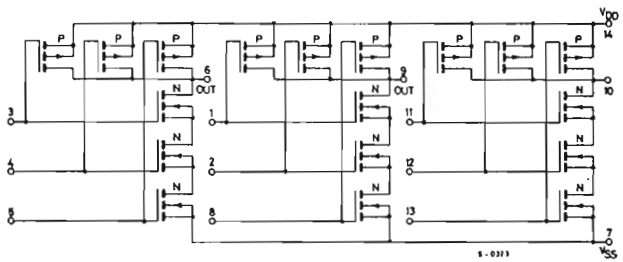


for **4012A**



SCHEMATIC DIAGRAMS (continued)

for **4023A**



RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage	3 to 15	V
V_i*	Input voltage	V_{DD} to V_{SS}	
T_{op}	Operating temperature:		
	for HBC types	-55 to 125	°C
	for HBF types	-40 to 85	°C

* This is measured with respect to the V_{SS} pin voltage

STATIC ELECTRICAL CHARACTERISTICS

Parameter	Test conditions	Min.	Typ.	Max.	Unit
HBC types (extended temperature range)					
I_L Quiescent current	V_{DD} = 5V				
	at T_{amb} = -55°C			0.05	μA
	at T_{amb} = 25°C		0.001	0.05	μA
	at T_{amb} = 125°C			3	μA
	V_{DD} = 10V				
	at T_{amb} = -55°C			0.1	μA
	at T_{amb} = 25°C		0.001	0.1	μA
	at T_{amb} = 125°C			6	μA

STATIC ELECTRICAL CHARACTERISTICS (continued)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OH}	Output high voltage	$I_o = 0$				
		$V_{DD} = 5V$				
		at $T_{amb} = -55°C$	4.99			V
		at $T_{amb} = 25°C$	4.99	5		V
		at $T_{amb} = 125°C$	4.95			V
		$V_{DD} = 10V$				
		at $T_{amb} = -55°C$	9.99			V
		at $T_{amb} = 25°C$	9.99	10		V
		at $T_{amb} = 125°C$	9.95			V
V_{OL}	Output low voltage	$I_o = 0$				
		$V_{DD} = 5V$ or $10V$				
		at $T_{amb} = -55°C$			0.01	V
		at $T_{amb} = 25°C$		0	0.01	V
		at $T_{amb} = 125°C$			0.05	V
→ V_{NH}	Noise immunity	$V_{DD} = 5V$ $V_o = 0.95V$				
		at $T_{amb} = -55°C$	1.4			V
		at $T_{amb} = 25°C$	1.5	2.25		V
		at $T_{amb} = 125°C$	1.5			V
		$V_{DD} = 10V$ $V_o = 2.9V$				
		at $T_{amb} = -55°C$	2.9			V
		at $T_{amb} = 25°C$	3	4.5		V
		at $T_{amb} = 125°C$	3			V
→ V_{NL}	Noise immunity	$V_{DD} = 5V$ $V_o = 3.6V$				
		at $T_{amb} = -55°C$	1.5			V
		at $T_{amb} = 25°C$	1.5	2.25		V
		at $T_{amb} = 125°C$	1.4			V
		$V_{DD} = 10V$ $V_o = 7.2V$				
		at $T_{amb} = -55°C$	3			V
		at $T_{amb} = 25°C$	3	4.5		V
		at $T_{amb} = 125°C$	2.9			V
I_DN	Output drive current N-channel	$V_{DD} = 5V$ $V_o = 0.5V$				
		for **4011A** and **4023A** types				
		at $T_{amb} = -55°C$	0.31			mA
		at $T_{amb} = 25°C$	0.25	0.5		mA
		at $T_{amb} = 125°C$	0.175			mA

STATIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_DN	Output drive current N-channel	for **4012A** type				
		at T_{amb} = -55°C		0.15		mA
		at T_{amb} = 25°C		0.12	0.25	mA
		at T_{amb} = 125°C		0.085		mA
		V_{DD} = 10V V_o = 0.5V				
		for **4011A** and **4023A** types				
		at T_{amb} = -55°C		0.62		mA
		at T_{amb} = 25°C		0.5	0.6	mA
		at T_{amb} = 125°C		0.35		mA
		for **4012A** type				
		at T_{amb} = -55°C		0.31		mA
		at T_{amb} = 25°C		0.25	0.6	mA
		at T_{amb} = 125°C		0.175		mA
I_DP	Output drive current P-channel	V_{DD} = 5V V_o = 4.5V				
		at T_{amb} = -55°C		-0.31		mA
		at T_{amb} = 25°C		-0.25	-0.5	mA
		at T_{amb} = 125°C		-0.175		mA
		V_{DD} = 10V V_o = 9.5V				
		at T_{amb} = -55°C		-0.75		mA
		at T_{amb} = 25°C		-0.6	-1.2	mA
		at T_{amb} = 125°C		-0.4		mA
I_i	Input current	T_{amb} = 25°C		10		pA

HBF types (standard temperature range)

I_L	Quiescent current	V_{DD} = 5V				
		at T_{amb} = -40°C			0.5	µA
		at T_{amb} = 25°C		0.005	0.5	µA
		at T_{amb} = 85°C			15	µA
		V_{DD} = 10V				
		at T_{amb} = -40°C			5	µA
		at T_{amb} = 25°C		0.005	5	µA
		at T_{amb} = 85°C			30	µA

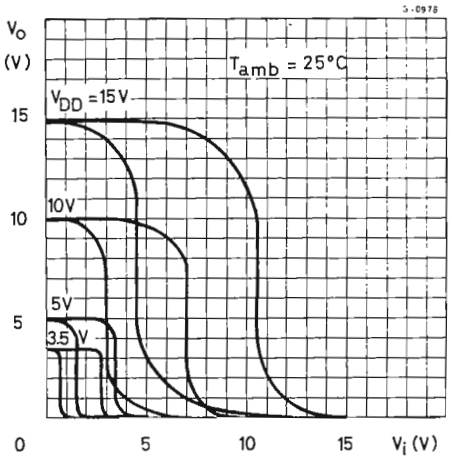
STATIC ELECTRICAL CHARACTERISTICS (continued)

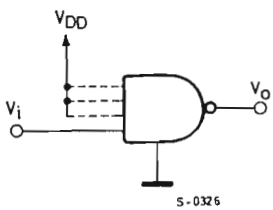
	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OH}	Output high voltage	$I_o = 0$				
		$V_{DD} = 5V$				
		at $T_{amb} = -40°C$	4.99			V
		at $T_{amb} = 25°C$	4.99	5		V
		at $T_{amb} = 85°C$	4.95			V
		$V_{DD} = 10V$				
		at $T_{amb} = -40°C$	9.99			V
		at $T_{amb} = 25°C$	9.99	10		V
		at $T_{amb} = 85°C$	9.95			V
V_{OL}	Output low voltage	$I_o = 0$				
		$V_{DD} = 5V$ or $10V$				
		at $T_{amb} = -40°C$			0.01	V
		at $T_{amb} = 25°C$		0	0.01	V
		at $T_{amb} = 85°C$			0.05	V
→ V_{NH}	Noise immunity	$V_{DD} = 5V$ $V_o = 0.95V$				
		at $T_{amb} = -40°C$	1.4			V
		at $T_{amb} = 25°C$	1.5	2.25		V
		at $T_{amb} = 85°C$	1.5			V
		$V_{DD} = 10V$ $V_o = 2.9V$				
		at $T_{amb} = -40°C$	2.9			V
		at $T_{amb} = 25°C$	3	4.5		V
		at $T_{amb} = 85°C$	3			V
→ V_{NL}	Noise immunity	$V_{DD} = 5V$ $V_o = 3.6V$				
		at $T_{amb} = -40°C$	1.5			V
		at $T_{amb} = 25°C$	1.5	2.25		V
		at $T_{amb} = 85°C$	1.4			V
		$V_{DD} = 10V$ $V_o = 7.2V$				
		at $T_{amb} = -40°C$	3			V
		at $T_{amb} = 25°C$	3	4.5		V
		at $T_{amb} = 85°C$	2.9			V
I_DN	Output drive current N-channel	$V_{DD} = 5V$ $V_o = 0.5V$ for **4011A** and **4023A** types				
		at $T_{amb} = -40°C$	0.145			mA
		at $T_{amb} = 25°C$	0.12	0.5		mA
		at $T_{amb} = 85°C$	0.95			mA

STATIC ELECTRICAL CHARACTERISTICS (continued)

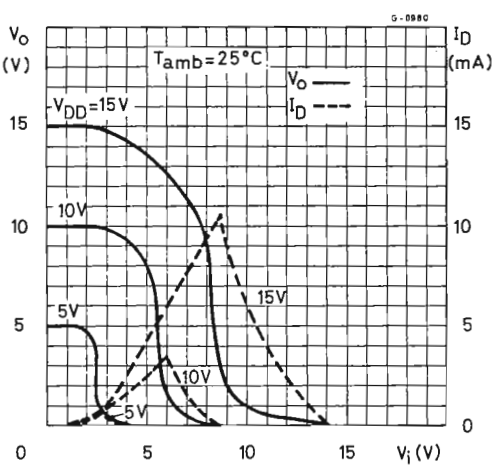
Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_DN	Output drive current N-channel	for **4012A** type				
		at T_{amb} = -40°C		0.072		mA
		at T_{amb} = 25°C		0.06	0.25	mA
		at T_{amb} = 85°C		0.05		mA
		V_{DD} = 10V V_o = 0.5V				
		for **4011A** and **4023A** types				
		at T_{amb} = -40°C		0.3		mA
		at T_{amb} = 25°C		0.25	0.6	mA
		at T_{amb} = 85°C		0.2		mA
		for **4012A** type				
		at T_{amb} = -40°C		0.155		mA
		at T_{amb} = 25°C		0.13	0.6	mA
		at T_{amb} = 85°C		0.105		mA
I_DP	Output drive current P-channel	V_{DD} = 5V V_o = 4.5V				
		at T_{amb} = -40°C		-0.145		mA
		at T_{amb} = 25°C		-0.12	-0.5	mA
		at T_{amb} = 85°C		-0.95		mA
		V_{DD} = 10V V_o = 9.5V				
		at T_{amb} = -40°C		-0.35		mA
		at T_{amb} = 25°C		-0.3	-1.2	mA
		at T_{amb} = 85°C		-0.24		mA
I_i	Input current	T_{amb} = 25°C		10		pA

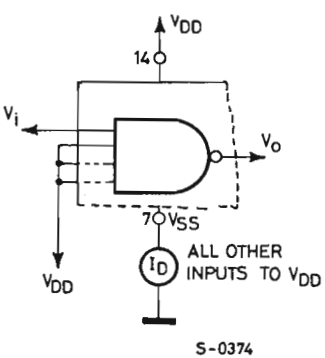
Minimum and maximum voltage transfer characteristic curves and test circuit



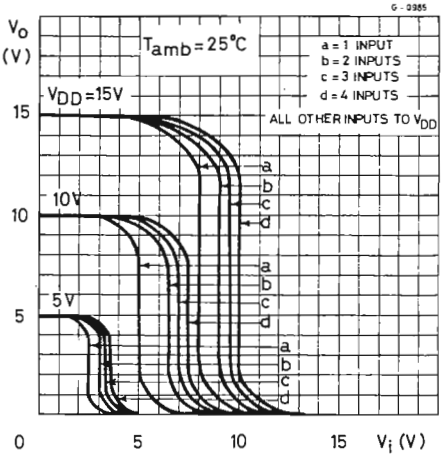


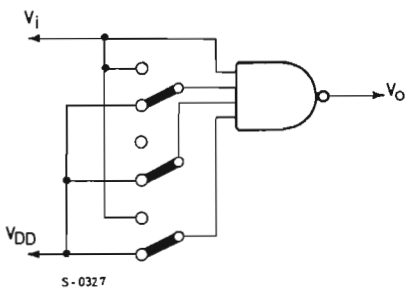
Typical current and voltage transfer characteristic curves and test circuit



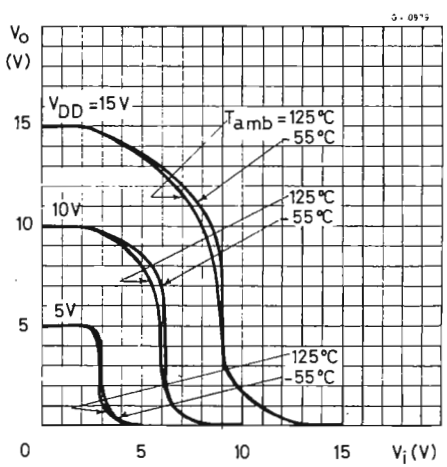


Typical multiple input switching transfer characteristic curves and test circuit (for **4012A** only)

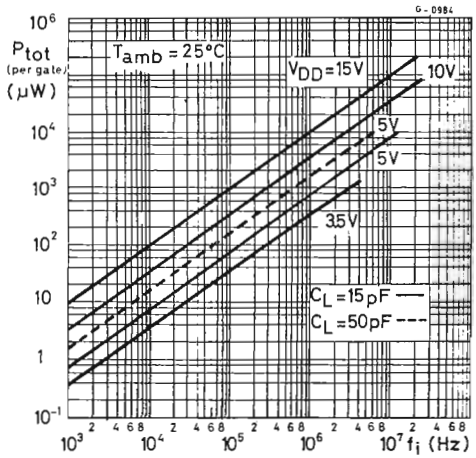




Typical voltage transfer characteristics vs. ambient temperature



Typical power dissipation characteristics



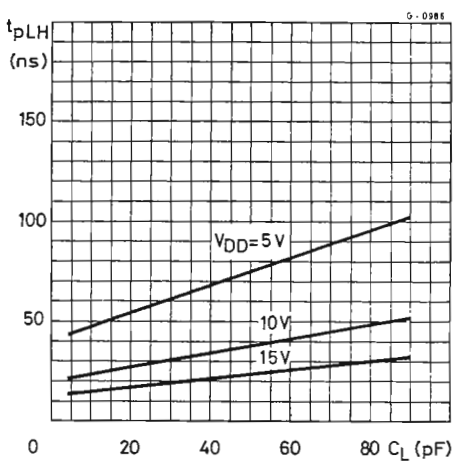
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 15 pF, typical temperature coefficient for all V_{DD} = 0.3%/°C values)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
HBC types (extended temperature range)						
t_{PLH}	Propagation delay time (low to high level)	V_{DD} = 5V		50	75	ns
		V_{DD} = 10V		25	40	ns
t_{PHL}	Propagation delay time (high to low level)	V_{DD} = 5V				
		for **4011A** and **4023A** types		50	75	ns
		for **4012A** type		100	150	ns
		V_{DD} = 10V				
		for **4011A** and **4023A** types		25	40	ns
		for **4012A** type		50	75	ns
t_{TLH}	Transition time (low to high level)	V_{DD} = 5V		75	100	ns
		V_{DD} = 10V		40	60	ns
t_{THL}	Transition time (high to low level)	V_{DD} = 5V				
		for **4011A** and **4023A** types		75	125	ns
		for **4012A** type		250	375	ns
		V_{DD} = 10V				
		for **4011A** and **4023A** types		50	75	ns
		for **4012A** type		125	200	ns
C_I	Input capacitance	Any input		5		pF
HBF types (standard temperature range)						
t_{PLH}	Propagation delay time (low to high level)	V_{DD} = 5V		50	100	ns
		V_{DD} = 10V		25	50	ns
t_{PHL}	Propagation delay time (high to low level)	V_{DD} = 5V				
		for **4011A** and **4023A** types		50	100	ns
		for **4012A** type		100	200	ns
		V_{DD} = 10V				
		for **4011A** and **4023A** types		25	50	ns
		for **4012A** type		50	100	ns

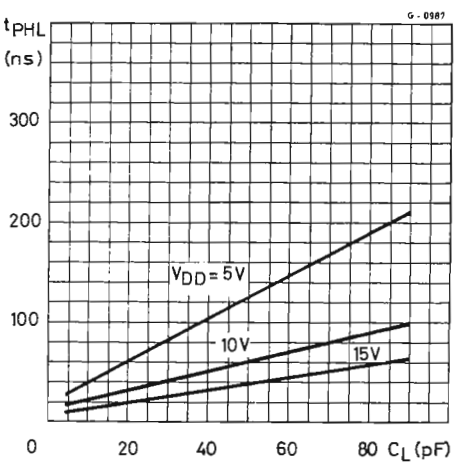
DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
t_{TLH}	Transition time (low to high level)	$V_{DD} = 5V$		75	125	ns
		$V_{DD} = 10V$		40	75	ns
t_{THL}	Transition time (high to low level)	$V_{DD} = 5V$				
		for **4011A** and **4023A** types		75	150	ns
		for **4012A** type		250	500	ns
		$V_{DD} = 10V$				
		for **4011A** and **4023A** types		50	100	ns
		for **4012A** type		125	250	ns
C_i	Input capacitance	Any input		5		pF

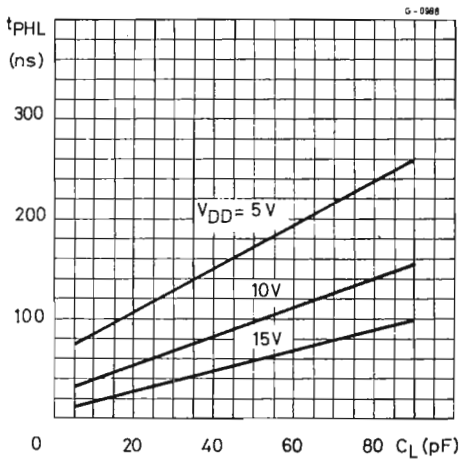
Typical low-to-high level propagation delay time vs. C_L



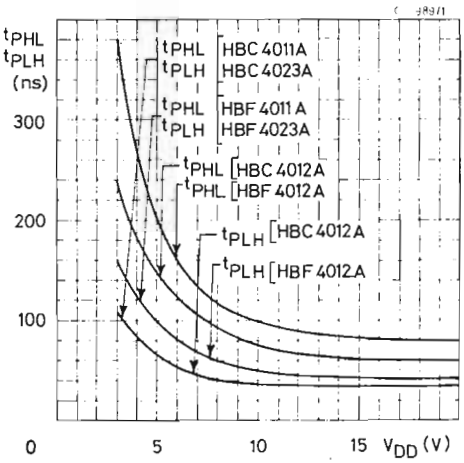
Typical high-to-low level propagation delay time vs. C_L (for **4011A** and **4023A** only)



Typical high-to-low level propagation delay time vs. C_L (for **4012A** only)



Minimum propagation delay time vs. V_{DD}



COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

DUAL "D" TYPE FLIP-FLOP WITH SET-RESET CAPABILITY

- LOW QUIESCENT POWER DISSIPATION
- WIDE SUPPLY VOLTAGE RANGE: 3 to 15V
- HIGH NOISE IMMUNITY: 45% of V_{DD} (TYP.)
- HIGH SPEED OPERATION: 10 MHz (TYP.) CLOCK TOGGLE RATE at V_{DD}-V_{SS}=10V
- INPUTS FULLY PROTECTED
- LOW OUTPUT IMPEDANCE
- HIGH FANOUT
- STATIC FLIP-FLOP OPERATION

The **HBC 4013A** (extended temperature range) and **HBF 4013A** (standard temperature range) are monolithic integrated circuits, available in 14-lead dual in-line plastic or ceramic package and ceramic flat package.
The **HBC/HBF 4013A** types consist of two identical, independent data-type flip-flops. Each flip-flop has independent data, set, reset and clock inputs and Q and $\overline{Q}$ outputs (for functions see truth table). These devices can be used in shift register and, by connecting $\overline{Q}$ output to the data input, in counter and toggle applications.

ABSOLUTE MAXIMUM RATINGS

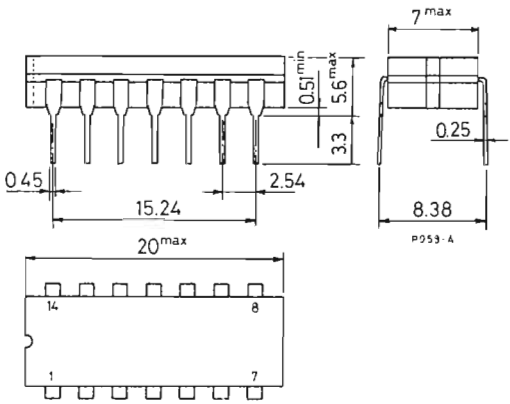
V_{DD}-V_{SS}	Supply voltage	-0.5 to 15	V
V_i	Input voltage (at any pin)	$V_{SS} \leqslant V_i \leqslant V_{DD}$	
P_{tot}	Total power dissipation (per package)	200	mW
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature: for **HBC** types	-55 to 125	°C
	for **HBF** types	-40 to 85	°C

ORDERING NUMBERS :

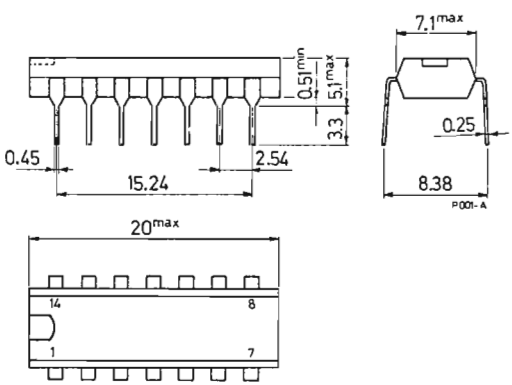
HBC 4013 AD	for dual in-line ceramic package
HBC 4013 AF	for dual in-line ceramic package frit seal (extended temperature range)
HBC 4013 AK	for ceramic flat package
HBF 4013 AE	for dual in-line plastic package
HBF 4013 AF	for dual in-line ceramic package frit seal (standard temperature range)

MECHANICAL DATA (dimensions in mm)

Dual in-line ceramic package
for HBC 4013 AD and
HBC/HBF 4013 AF

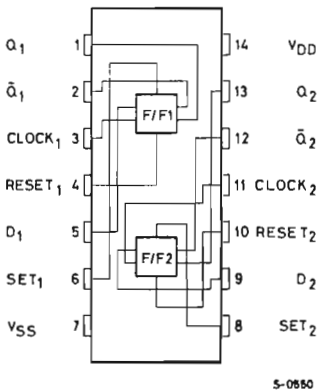


Dual in-line plastic package
for HBF 4013 AE

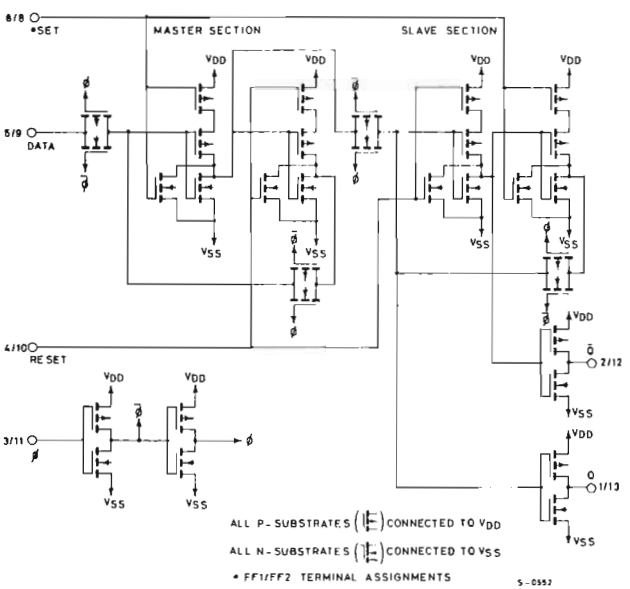


Ceramic flat package for HBC 4013 AK

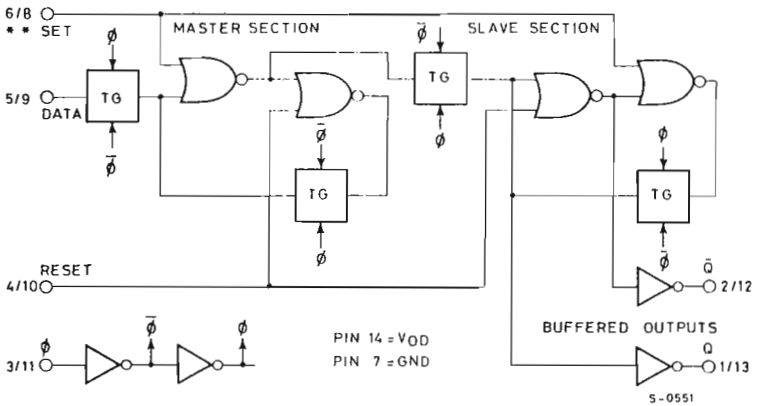
CONNECTION DIAGRAM (top view)



SCHEMATIC DIAGRAM



FUNCTIONAL LOGIC DIAGRAM and TRUTH TABLE



* = INVALID CONDITION
** = FF1/FF2 TERMINAL ASSIGNMENTS
X = DON'T CARE CASE

CLOCK ϕ	D	R	S	Q	$\bar{Q}$	
⌐‾	0	0	0	0	1	
⌐‾	1	0	0	1	0	
‾⌐	X	0	0	Q	$\bar{Q}$	← No change
X	X	1	0	0	1	
X	X	0	1	1	0	
X	X	1	1	*	*	

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage	3 to 15	V
V_i*	Input voltage	V_{DD} to V_{SS}	
T_{op}	Operating temperature: for **HBC** types	-55 to 125	°C
	for **HBF** types	-40 to 85	°C

* This is measured with respect to the V_{SS} pin voltage

STATIC ELECTRICAL CHARACTERISTICS

Parameter	Test conditions	Min.	Typ.	Max.	Unit
HBC types (extended temperature range)					
I_L Quiescent current	V_{DD} = 5V				
	at T_{amb}=-55°C			1	μA
	at T_{amb}= 25°C		0.005	1	μA
	at T_{amb}=125°C			60	μA
	V_{DD} = 10V				
	at T_{amb}=-55°C			2	μA
	at T_{amb}= 25°C		0.005	2	μA
	at T_{amb}=125°C			120	μA
V_{OH} Output high voltage	I_o = 0				
	V_{DD} = 5V				
	at T_{amb}=-55°C	4.99			V
	at T_{amb}= 25°C	4.99	5		V
	at T_{amb}=125°C	4.95			V
	V_{DD}= 10V				
	at T_{amb}=-55°C	9.99			V
	at T_{amb}= 25°C	9.99	10		V
	at T_{amb}=125°C	9.95			V
V_{OL} Output low voltage	I_o = 0				
	V_{DD} = 5V or 10V				
	at T_{amb}=-55°C			0.01	V
	at T_{amb}= 25°C		0	0.01	V
	at T_{amb}=125°C			0.05	V
→ V_{NH} Noise immunity	V_{DD} = 5V V_o = 4.2V				
	at T_{amb}=-55°C	1.4			V
	at T_{amb}= 25°C	1.5	2.25		V
	at T_{amb}=125°C	1.5			V
	V_{DD} = 10V V_o = 9V				
	at T_{amb}=-55°C	2.9			V
	at T_{amb}= 25°C	3	4.5		V
	at T_{amb}=125°C	3			V

STATIC ELECTRICAL CHARACTERISTICS (continued)

	Parameter		Test conditions		Min.	Typ.	Max.	Unit
→	V_{NL}	Noise immunity	V_{DD} = 5V	V_o = 0.8V				
				at T_{amb}=-55°C	1.5			V
				at T_{amb}= 25°C	1.5		2.25	V
				at T_{amb}=125°C	1.4			V
			V_{DD} = 10V	V_o = 1V				
				at T_{amb}=-55°C	3			V
				at T_{amb}= 25°C	3		4.5	V
				at T_{amb}=125°C	2.9			V
	I_DN	Output drive current N-channel	V_{DD} = 5V	V_o = 0.5V				
				at T_{amb}=-55°C	0.65			mA
				at T_{amb}= 25°C	0.5		1	mA
				at T_{amb}=125°C	0.35			mA
			V_{DD} = 10V	V_o = 0.5V				
				at T_{amb}=-55°C	1.25			mA
				at T_{amb}= 25°C	1		2.5	mA
				at T_{amb}=125°C	0.75			mA
	I_DP	Output drive current P-channel	V_{DD} = 5V	V_o = 4.5V				
				at T_{amb}=-55°C	-0.31			mA
				at T_{amb}= 25°C	-0.25		-0.5	mA
				at T_{amb}=125°C	-0.175			mA
			V_{DD} = 10V	V_o = 9.5V				
				at T_{amb}=-55°C	-0.8			mA
				at T_{amb}= 25°C	-0.65		-1.3	mA
				at T_{amb}=125°C	-0.45			mA
	I_i	Input current	T_{amb} = 25°C			10		pA

HBF types (standard temperature range)

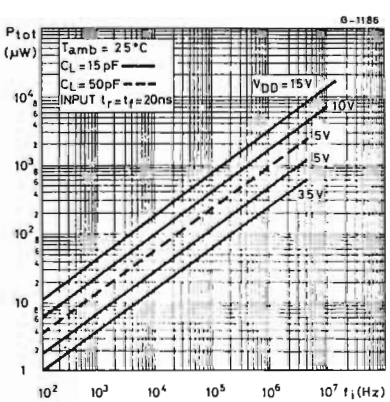
I_L	Quiescent current	V_{DD} = 5V				
			at T_{amb}=-40°C		10	μA
			at T_{amb}= 25°C	0.01	10	μA
			at T_{amb}= 85°C		140	μA

STATIC ELECTRICAL CHARACTERISTICS (continued)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_L	Quiescent current	V_{DD} = 10V				
		at T_{amb}=-40°C			20	μA
		at T_{amb}= 25°C		0.02	20	μA
		at T_{amb}= 85°C			280	μA
V_{OH}	Output high voltage	I_o = O				
		V_{DD} = 5V				
		at T_{amb}=-40°C	4.99			V
		at T_{amb}= 25°C	4.99	5		V
		at T_{amb}= 85°C	4.95			V
		V_{DD} = 10V				
		at T_{amb}=-40°C	9.99			V
		at T_{amb}= 25°C	9.99	10		V
		at T_{amb}= 85°C	9.95			V
V_{OL}	Output low voltage	I_o = O				
		V_{DD}= 5V or 10V				
		at T_{amb}=-40°C			0.01	V
		at T_{amb}= 25°C		0	0.01	V
		at T_{amb}= 85°C			0.05	V
→ V_{NH}	Noise immunity	V_{DD} = 5V V_o = 4.2V				
		at T_{amb}=-40°C	1.4			V
		at T_{amb}= 25°C	1.5	2.25		V
		at T_{amb}= 85°C	1.5			V
		V_{DD} = 10V V_o = 9V				
		at T_{amb}=-40°C	2.9			V
		at T_{amb}= 25°C	3	4.5		V
		at T_{amb}= 85°C	3			V
→ V_{NL}	Noise immunity	V_{DD} = 5V V_o = 0.8V				
		at T_{amb}=-40°C	1.5			V
		at T_{amb}= 25°C	1.5	2.25		V
		at T_{amb}= 85°C	1.4			V

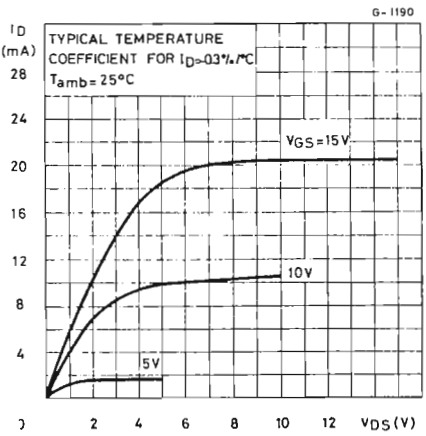
STATIC ELECTRICAL CHARACTERISTICS (continued)

	Parameter		Test conditions	Min.	Typ.	Max.	Unit
→	V_{NL}	Noise immunity	V_{DD} = 10V V_o = 1V				
			at T_{amb}=-40°C	3			V
			at T_{amb}= 25°C	3		4.5	V
			at T_{amb}= 85°C	2.9			V
	I_DN	Output drive current N-channel	V_{DD} = 5V V_o = 0.5V				
			at T_{amb}=-40°C	0.35			mA
			at T_{amb}= 25°C	0.3		1	mA
			at T_{amb}= 85°C	0.24			mA
			V_{DD} = 10V V_o = 0.5V				
			at T_{amb}=-40°C	0.72			mA
			at T_{amb}= 25°C	0.6		2.5	mA
			at T_{amb}= 85°C	0.5			mA
→	I_DP	Output drive current P-channel	V_{DD} = 5V V_o = 4.5V				
			at T_{amb}=-40°C	-0.17			mA
			at T_{amb}= 25°C	-0.14		-0.5	mA
			at T_{amb}= 85°C	-0.12			mA
			V_{DD} = 10V V_o = 9.5V				
			at T_{amb}=-40°C	-0.4			mA
			at T_{amb}= 25°C	-0.33		-1.3	mA
			at T_{amb}= 85°C	-0.27			mA
	I_i	Input current	T_{amb} = 25°C		10		pA

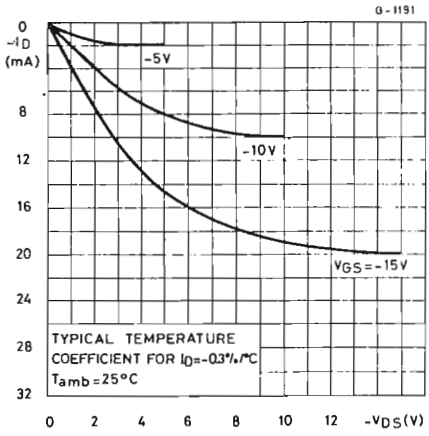


Typical power dissipation characteristics

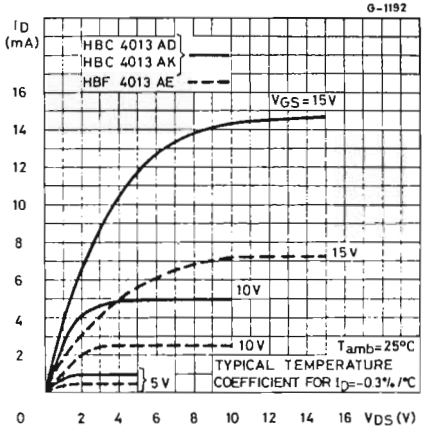
Typical N-channel drain characteristics



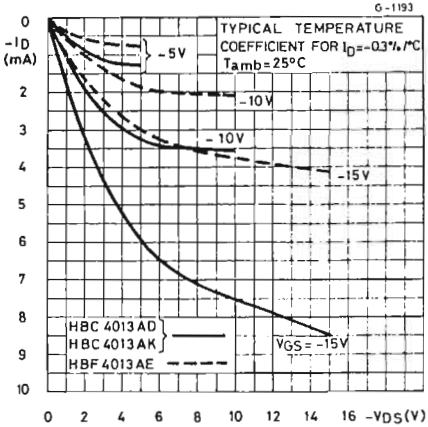
Typical P-channel drain characteristics



Minimum N-channel drain characteristics

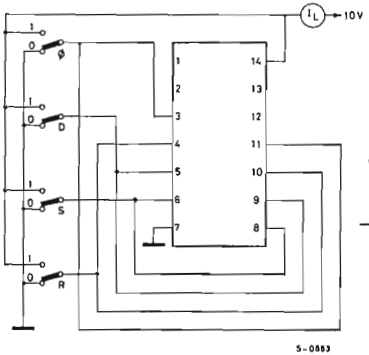


Minimum P-channel drain characteristics



TEST CIRCUITS

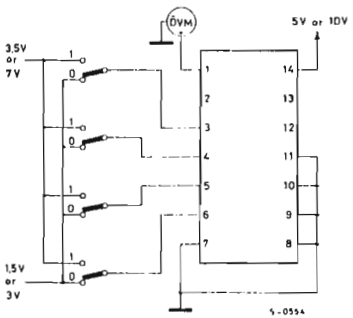
Quiescent device current



TEST PERFORMED WITH THE FOLLOWING SEQUENCE OF "1's" AND "0's".

Φ	D	S	R
0	1	0	1
0	0	1	1
0	0	1	0
1	0	1	0

Noise immunity



DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 15 pF typical temperature coefficient for all V_{DD} = 0.3%/°C values, all input rise and fall time = 20 ns, except $t_{\phi r}$ and $t_{\phi f}$)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
CLOCKED OPERATION					
t_{PLH}, t_{PHL} Propagation delay time	V_{DD} = 5V				
	for HBC types		150	300	ns
	for HBF types		150	350	ns
	V_{DD} = 10V				
	for HBC types		75	110	ns
	for HBF types		75	125	ns
t_{TLH}, t_{THL} Transition time	V_{DD} = 5V				
	for HBC types		75	125	ns
	for HBF types		75	150	ns
	V_{DD} = 10V				
	for HBC types		50	70	ns
	for HBF types		50	75	ns

DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
t_{pwH}, t_{pwL}	Minimum clock pulse width	$V_{DD} = 5V$				
		for **HBC** types		125	200	ns
		for **HBF** types		125	500	ns
		$V_{DD} = 10V$				
		for **HBC** types		50	80	ns
		for **HBF** types		50	100	ns
$t_{\phi r}$, $t_{\phi f}$	Clock rise and fall time	$V_{DD} = 5V$				
		for **HBC** and **HBF** types			15	μs
		$V_{DD} = 10V$				
		for **HBC** and **HBF** types			5	μs
t_s	Set-up time	$V_{DD} = 5V$				
		for **HBC** types		20	40	ns
		for **HBF** types		20	50	ns
		$V_{DD} = 10V$				
		for **HBC** types		10	20	ns
		for **HBF** types		10	25	ns
f_{max}	Maximum clock frequency	$V_{DD} = 5V$				
		for **HBC** types	2.5	4		MHz
		for **HBF** types	1	4		MHz
		$V_{DD} = 10V$				
		for **HBC** types	7	10		MHz
		for **HBF** types	5	10		MHz
C_i	Input capacitance	Any input for **HBC** and **HBF** types		5		pF

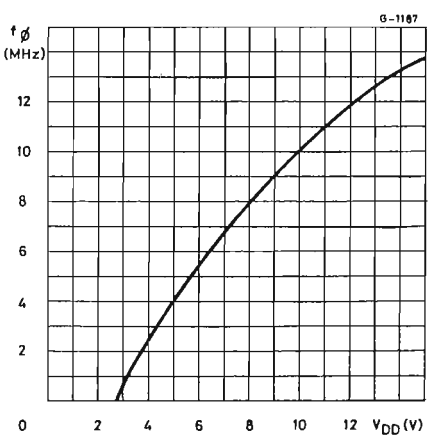
SET and RESET OPERATION

$t_{PLH(S)}$, $t_{PHL(R)}$	Propagation delay time	$V_{DD} = 5V$				
		for **HBC** types		175	300	ns
		for **HBF** types		175	350	ns

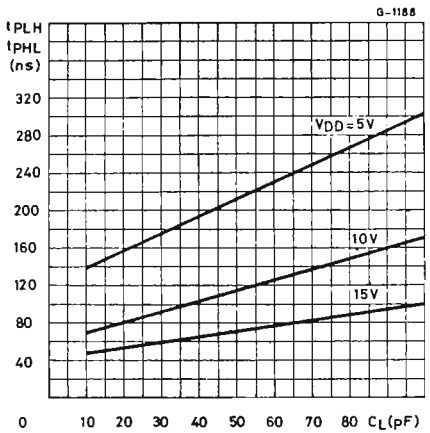
DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{PLH(S)}$, Propagation delay time $t_{PHL(R)}$	V_{DD} = 10V				
	for **HBC** types		75	110	ns
	for **HBF** types		75	125	ns
$t_{pwH(S)}$, Minimum set and $t_{pwL(R)}$ reset pulse widths	V_{DD} = 5V				
	for **HBC** types		125	250	ns
	for **HBF** types		125	500	ns
	V_{DD} = 10V				
	for **HBC** types		50	100	ns
	for **HBF** types		50	125	ns

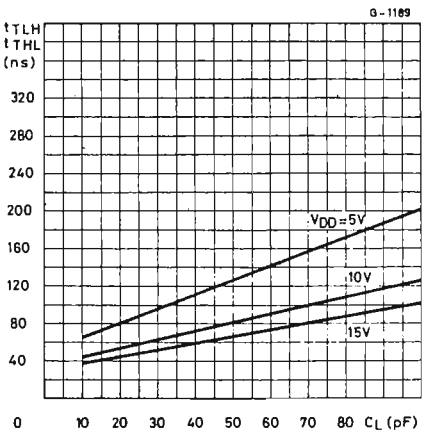
Typical clock frequency vs. V_{DD}



Typical propagation delay time vs. C_L



Typical transition time vs. C_L



COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

8-STAGE STATIC SHIFT REGISTER SYNCHRONOUS PARALLEL OR SERIAL INPUT/SERIAL OUTPUT

- LOW QUIESCENT POWER DISSIPATION
- WIDE SUPPLY VOLTAGE RANGE: 3 to 15V
- HIGH NOISE IMMUNITY: 45% of V_{DD} (TYP.)
- MEDIUM SPEED OPERATION: 5 MHz (TYP.) CLOCK RATE $V_{DD} - V_{SS} = 10V$
- INPUTS FULLY PROTECTED
- FULLY STATIC OPERATION
- MSI COMPLEXITY on a SINGLE CHIP:
  8 MASTER-SLAVE FLIP-FLOPS PLUS OUTPUT BUFFERING and CONTROL GATING

The **HBC 4014A** (extended temperature range) and **HBF 4014A** (standard temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package. The **HBC/HBF 4014A** types are 8-stage parallel-input/serial output registers having common clock and parallel-serial control inputs, a single serial data input, and individual parallel "Jam" inputs to each register stage. Each register stage is a D-type, master-slave flip-flop. In addition to an output from stage 8, "Q" outputs are also available from stage 6 and 7. Parallel as well as serial entry is made into the register synchronous with the positive clock line transition and under control of the parallel-serial control input. When the parallel-serial control input is "low", data is serially shifted into the 8-stage register synchronously with the positive transition of the clock line. When the parallel-serial control input is "high", data is jammed into the 8-stage register via the parallel input lines and synchronous with the positive transition of the clock line. Register expansion using multiple **HBC/HBF 4014A** packages is permitted.

ABSOLUTE MAXIMUM RATINGS

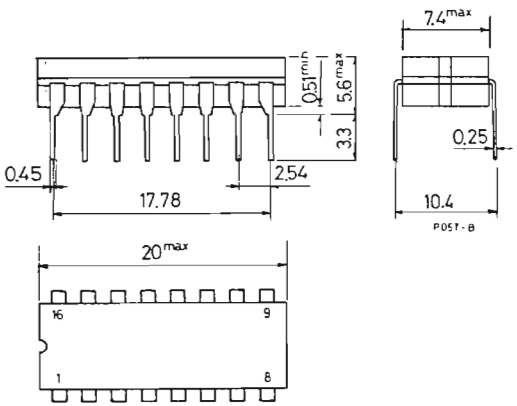
$V_{DD}-V_{SS}$	Supply voltage	-0.5 to 15	V
V_i	Input voltage (at any pin)	$V_{SS} \leqslant V_I \leqslant V_{DD}$	
P_{tot}	Total power dissipation (per package)	200	mW
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature : for **HBC** types	-55 to 125	°C
	for **HBF** types	-40 to 85	°C

ORDERING NUMBERS:

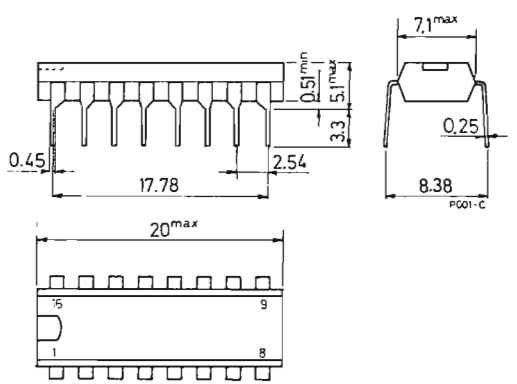
HBC 4014 AD for dual in-line ceramic package
HBC 4014 AF for dual in-line ceramic package, frit seal (extended temperature range)
HBC 4014 AK for ceramic flat package
HBF 4014 AE for dual in-line plastic package
HBF 4014 AF for dual in-line ceramic package, frit seal (standard temperature range)

MECHANICAL DATA (dimensions in mm)

Dual in-line ceramic package
for HBC 4014 AD and
HBC/HBF 4014 AF

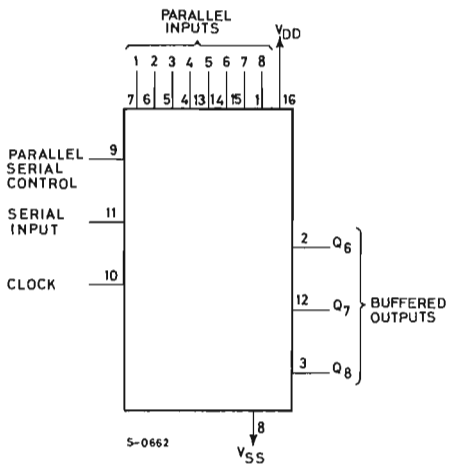


Dual in-line plastic package
for HBF 4014 AE

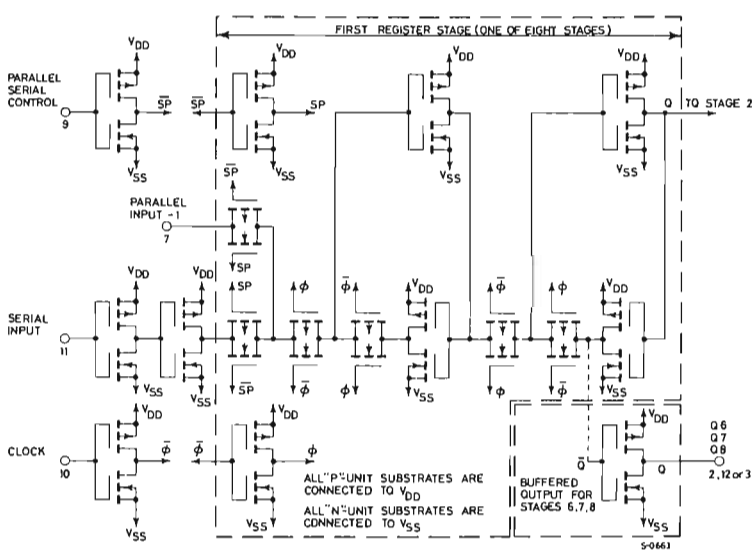


Ceramic flat package for HBC 4014 AK

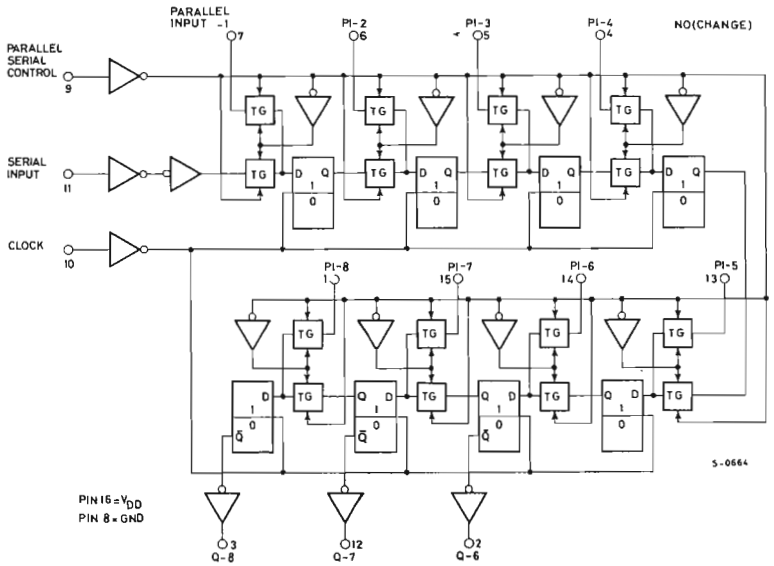
CONNECTION DIAGRAM (top view)



SCHEMATIC DIAGRAM



LOGIC BLOCK DIAGRAM



TRUTH TABLE

CLOCK* ϕ	Serial Input	Parallel Serial Control	Parallel Input-1	Parallel Input-n	(Internal) Q_1	Q_n	
⌒	X	I	O	O	O	O	
⌒	X	I	I	O	I	O	
⌒	X	I	O	I	O	I	
⌒	X	I	I	I	I	I	
⌒	O	O	X	X	O	Q_n-1	
⌒	I	O	X	X	I	Q_n-1	
⌣	X	X	X	X	Q_1	Q_n	← No change

* = Level Change
X = Don't care case

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage	3 to 15	V
V_i*	Input voltage	V_{DD} to V_{SS}	
T_{op}	Operating temperature: for **HBC** types	-55 to 125	°C
	for **HBF** types	-40 to 85	°C

*This is measured with respect to the V_{SS} pin voltage

STATIC ELECTRICAL CHARACTERISTICS

Parameter		Test conditions	Min.	Typ.	Max.	Unit
HBC types (extended temperature range)						
I_L	Quiescent current	V_{DD} = 5V				
		at T_{amb} = -55°C			5	μA
		at T_{amb} = 25°C		0.5	5	μA
		at T_{amb} = 125°C			300	μA
		V_{DD} = 10V				
		at T_{amb} = -55°C			10	μA
		at T_{amb} = 25°C		1	10	μA
		at T_{amb} = 125°C			600	μA
V_{OH}	Output high voltage	I_o = 0				
		V_{DD} = 5V				
		at T_{amb} = -55°C	4.99			V
		at T_{amb} = 25°C	4.99	5		V
		at T_{amb} = 125°C	4.95			V
		V_{DD} = 10V				
		at T_{amb} = -55°C	9.99			V
		at T_{amb} = 25°C	9.99	10		V
		at T_{amb} = 125°C	9.95			V
V_{OL}	Output low voltage	I_o = 0				
		V_{DD} = 5V or 10V				
		at T_{amb} = -55°C			0.01	V
		at T_{amb} = 25°C		0	0.01	V
		at T_{amb} = 125°C			0.05	V

STATIC ELECTRICAL CHARACTERISTICS (continued)

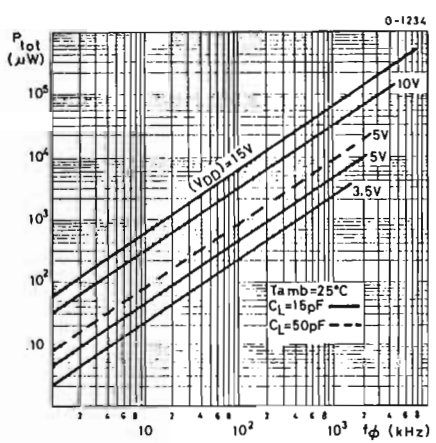
Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{NH}	Noise immunity	V_{DD} = 5V V_o = 4.2V				
		at T_{amb} = -55°C	1.4			V
		at T_{amb} = 25°C	1.5		2.25	V
		at T_{amb} = 125°C	1.5			V
		V_{DD} = 10V V_o = 9V				
		at T_{amb} = -55°C	2.9			V
		at T_{amb} = 25°C	3		4.5	V
		at T_{amb} = 125°C	3			V
V_{NL}	Noise immunity	V_{DD} = 5V V_o = 0.8V				
		at T_{amb} = -55°C	1.5			V
		at T_{amb} = 25°C	1.5		2.25	V
		at T_{amb} = 125°C	1.4			V
		V_{DD} = 10V V_o = 1V				
		at T_{amb} = -55°C	3			V
		at T_{amb} = 25°C	3		4.5	V
		at T_{amb} = 125°C	2.9			V
I_DN	Output drive current N-channel	V_{DD} = 5V V_o = 0.5V				
		at T_{amb} = -55°C	0.15			mA
		at T_{amb} = 25°C	0.12		0.3	mA
		at T_{amb} = 125°C	0.085			mA
		V_{DD} = 10V V_o = 0.5V				
		at T_{amb} = -55°C	0.31			mA
		at T_{amb} = 25°C	0.25		0.5	mA
		at T_{amb} = 125°C	0.175			mA
I_DP	Output drive current P-channel	V_{DD} = 5V V_o = 4.5V				
		at T_{amb} = -55°C	-0.1			mA
		at T_{amb} = 25°C	-0.08		-0.16	mA
		at T_{amb} = 125°C	-0.055			mA
		V_{DD} = 10V V_o = 9.5V				
		at T_{amb} = -55°C	-0.25			mA
		at T_{amb} = 25°C	-0.20		-0.44	mA
		at T_{amb} = 125°C	-0.14			mA
I_i	Input current	T_{amb} = 25°C		10		pA

STATIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
HBF types (standard temperature range)						
I_L	Quiescent current	$V_{DD} = 5V$				
		at $T_{amb} = -40°C$			50	μA
		at $T_{amb} = 25°C$		0.5	50	μA
		at $T_{amb} = 85°C$			700	μA
		$V_{DD} = 10V$				
		at $T_{amb} = -40°C$			100	μA
		at $T_{amb} = 25°C$		1	100	μA
		at $T_{amb} = 85°C$			1400	μA
V_{OH}	Output high voltage	$I_o = 0$				
		$V_{DD} = 5V$				
		at $T_{amb} = -40°C$	4.99			V
		at $T_{amb} = 25°C$	4.99	5		V
		at $T_{amb} = 85°C$	4.95			V
		$V_{DD} = 10V$				
		at $T_{amb} = -40°C$	9.99			V
		at $T_{amb} = 25°C$	9.99	10		V
		at $T_{amb} = 85°C$	9.95			V
V_{OL}	Output low voltage	$I_o = 0$				
		$V_{DD} = 5V$ or $10V$				
		at $T_{amb} = -40°C$			0.01	V
		at $T_{amb} = 25°C$		0	0.01	V
		at $T_{amb} = 85°C$			0.05	V
V_{NH}	Noise immunity	$V_{DD} = 5V$ $V_o = 4.2V$				
		at $T_{amb} = -40°C$	1.4			V
		at $T_{amb} = 25°C$	1.5	2.25		V
		at $T_{amb} = 85°C$	1.5			V
		$V_{DD} = 10V$ $V_o = 9V$				
		at $T_{amb} = -40°C$	2.9			V
		at $T_{amb} = 25°C$	3	4.5		V
		at $T_{amb} = 85°C$	3			V
V_{NL}	Noise immunity	$V_{DD} = 5V$ $V_o = 0.8V$				
		at $T_{amb} = -40°C$	1.5			V
		at $T_{amb} = 25°C$	1.5	2.25		V
		at $T_{amb} = 85°C$	1.4			V

STATIC ELECTRICAL CHARACTERISTICS (continued)

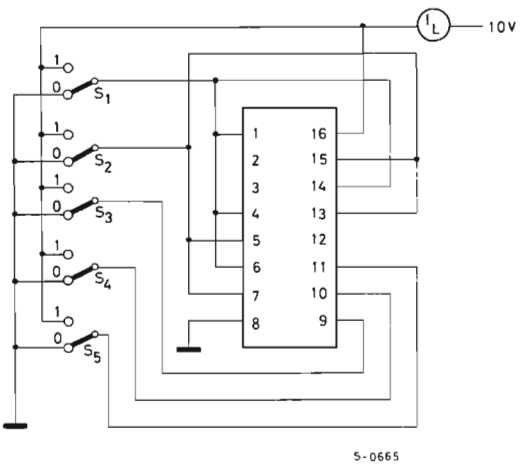
Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{NL}	Noise immunity	V_{DD} = 10V V_o = 1V				
		at T_{amb} = -40°C	3			V
		at T_{amb} = 25°C	3		4.5	V
		at T_{amb} = 85°C	2.9			V
I_DN	Output drive current N-channel	V_{DD} = 5V V_o = 0.5V				
		at T_{amb} = -40°C	0.072			mA
		at T_{amb} = 25°C	0.06		0.3	mA
		at T_{amb} = 85°C	0.05			mA
		V_{DD}=10V V_o = 0.5V				
		at T_{amb} = -40°C	0.12			mA
		at T_{amb} = 25°C	0.1		0.5	mA
		at T_{amb} = 85°C	0.08			mA
I_DP	Output drive current P-channel	V_{DD} = 5V V_o = 4.5V				
		at T_{amb} = -40°C	-0.06			mA
		at T_{amb} = 25°C	-0.05		-0.16	mA
		at T_{amb} = 85°C	-0.04			mA
		V_{DD}=10V V_o = 9.5V				
		at T_{amb} = -40°C	-0.12			mA
		at T_{amb} = 25°C	-0.1		-0.44	mA
		at T_{amb} = 85°C	-0.08			mA
I_I	Input current	T_{amb} = 25°C		10		pA



Typical power dissipation characteristics

TEST CIRCUITS

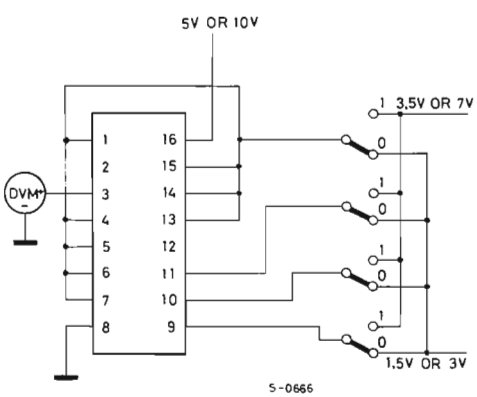
Quiescent device current



TEST PERFORMED WITH THE FOLLOWING SEQUENCE OF "1's" and "0's".

	S_1	S_2	S_3	S_4	S_5
Don't Test	0	1	1	0	0
Test	0	1	1	1	0
Test	1	0	0	0	0
Test	1	0	1	1	1
Test	1	0	0	0	1

Noise immunity



DYNAMIC ELECTRICAL CHARACTERISTICS

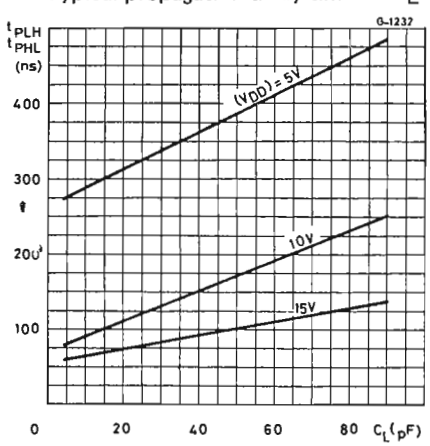
(T_{amb} = 25°C, C_L = 15 pF, typical temperature coefficient for all V_{DD} = 0.3%/°C values, all input rise and fall time = 20 ns, except $t_{\phi r}$ and $t_{\phi f}$)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
CLOCKED OPERATION					
t_{PLH}, t_{PHL} Propagation delay time	V_{DD} = 5V				
	for **HBC** types		300	750	ns
	for **HBF** types		300	1000	ns
	V_{DD} = 10V				
	for **HBC** types		100	225	ns
	for **HBF** types		100	300	ns
t_{TLH}, t_{THL} Transition time	V_{DD} = 5V				
	for **HBC** types		150	300	ns
	for **HBF** types		150	400	ns
	V_{DD} = 10V				
	for **HBC** types		75	125	ns
	for **HBF** types		75	150	ns
t_{pwH}, t_{pwL} Minimum clock pulse width	V_{DD} = 5V				
	for **HBC** types		200	500	ns
	for **HBF** types		200	830	ns
	V_{DD} = 10V				
	for **HBC** types		100	175	ns
	for **HBF** types		100	200	ns
$t_{\phi r}$, $t_{\phi f}$ Clock rise and fall time	V_{DD} = 5V or 10V				
	for **HBC** and **HBF** types			15	μs
t_s Set-up time	V_{DD} = 5V				
	for **HBC** types		100	350	ns
	for **HBF** types		100	500	ns
	V_{DD} = 10V				
	for **HBC** types		50	80	ns
	for **HBF** types		50	100	ns
f_{max} Maximum clock frequency	V_{DD} = 5V				
	for **HBC** types	1	2.5		MHz
	for **HBF** types	0.6	2.5		MHz

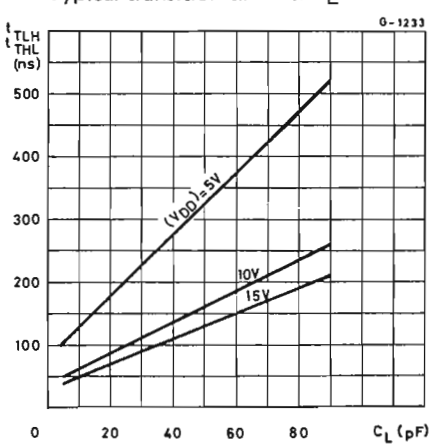
DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
f_{max}	Maximum clock frequency	$V_{DD} = 10V$				
		for **HBC** types	3	5		MHz
		for **HBF** types	2.5	5		MHz
C_i	Input capacitance	Any input for **HBC** and **HBF** types		5		pF

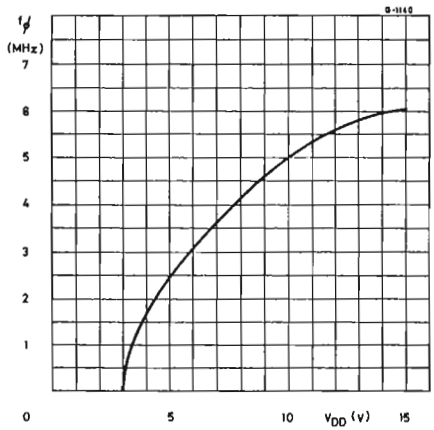
Typical propagation delay time vs. C_L



Typical transition time vs. C_L



Max. input clock frequency vs. V_{DD}



COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

DUAL 4-STAGE STATIC SHIFT REGISTER WITH SERIAL INPUT/PARALLEL OUTPUT

- LOW QUIESCENT POWER DISSIPATION
- WIDE SUPPLY VOLTAGE : 3 to 15V
- HIGH NOISE IMMUNITY
- MEDIUM SPEED OPERATION: 5 MHz (TYP.) CLOCK RATE at $V_{DD} - V_{SS} = 10V$
- FULLY STATIC OPERATION
- MSI COMPLEXITY on a SINGLE CHIP: 8 MASTER SLAVE FLIP-FLOPS PLUS OUTPUT BUFFERING

The **HBC 4015A** (extended temperature range) and **HBF 4015A** (standard temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package. The **HBC/HBF 4015A** types consist of two identical, independent, 4-stage serial-input/parallel-output registers. Each register has independent "Clock" and "Reset" inputs as well as a single serial "Data" input "Q" outputs are available from each of the four stages on both registers. All register stages are D-type, master-slave flip-flops. The logic level present at the data input is transferred into the first register stage and shifted over one stage at each positive - going clock transition. Resetting of all stages is accomplished by a high level on the reset line. Register expansion to 8 stages using one **HBC/HBF 4015A** package, or to more than 8 stages using additional **HBC/HBF 4015A** is possible.

ABSOLUTE MAXIMUM RATINGS

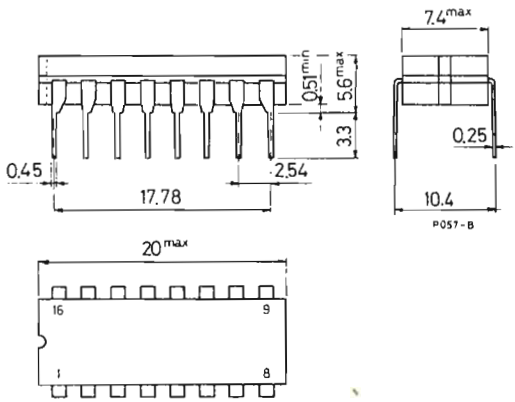
$V_{DD}-V_{SS}$	Supply voltage		- 0.5 to 15 V
V_i	Input voltage (at any pin)		$V_{SS} \leqslant V_i \leqslant V_{DD}$
P_{tot}	Total power dissipation (per package)		200 mW
T_{stg}	Storage temperature		-65 to 150 °C
T_{op}	Operating temperature:	for **HBC** types	-55 to 125 °C
		for **HBF** types	-40 to 85 °C

ORDERING NUMBERS:

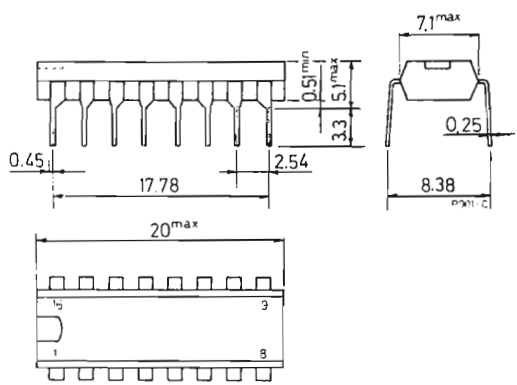
HBC 4015 AD for dual in-line ceramic package
HBC 4015 AF for dual in-line ceramic package, frit seal (extended temperature range)
HBC 4015 AK for ceramic flat package
HBF 4015 AE for dual in-line plastic package
HBF 4015 AF for dual in-line ceramic package, frit seal (standard temperature range)

MECHANICAL DATA (dimensions in mm)

Dual in-line ceramic package
for HBC 4015 AD and
HBC/HBF 4015 AF

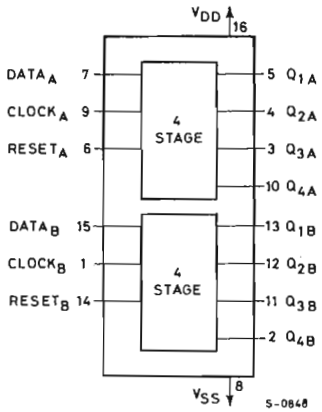


Dual in-line plastic package
for HBF 4015 AE



Ceramic flat package for HBC 4015 AK

CONNECTION DIAGRAM

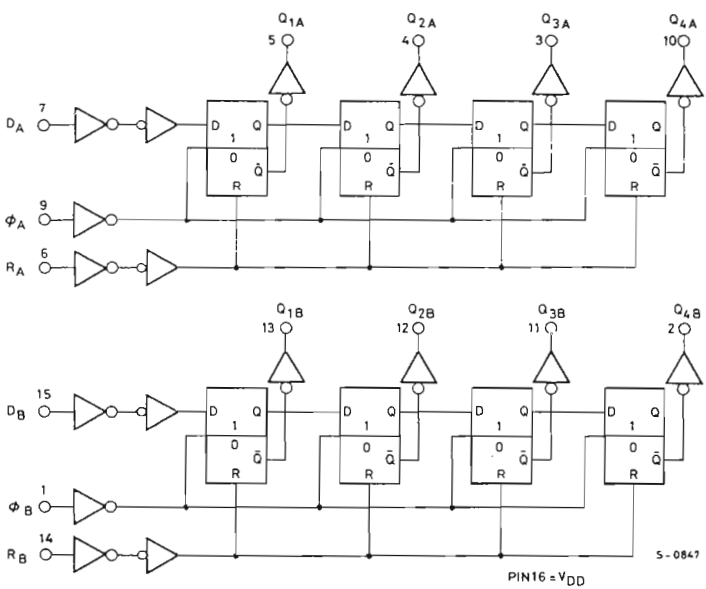


TRUTH TABLE

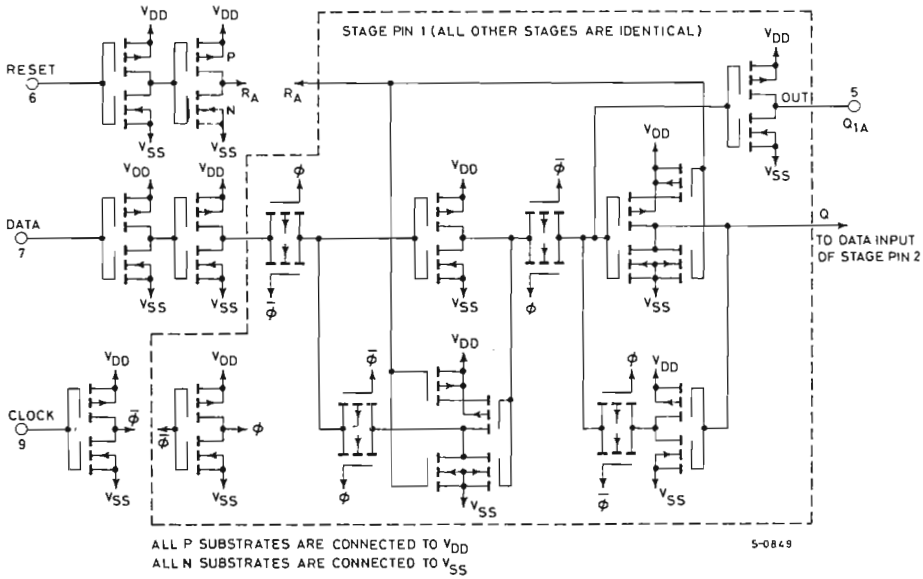
ϕ ▲	D	R	Q_1	Q_n	
⌐	0	0	0	Q_{n-1}	
⌐	1	0	1	Q_{n-1}	
⌐	X	0	Q_1	Q_n	No change ←
X	X	1	0	0	

▲ = LEVEL CHANGE
X = DON'T CARE CASE

LOGIC DIAGRAM



SCHEMATIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage	3 to 15	V
V_i*	Input voltage	V_{DD} to V_{SS}	
T_{op}	Operating temperature: for **HBC** types	-55 to 125	°C
	for **HBF** types	-40 to 85	°C

* This is measured with respect to the V_{SS} pin voltage

STATIC ELECTRICAL CHARACTERISTICS

Parameter	Test conditions	Min.	Typ.	Max.	Unit
HBC types (extended temperature range)					
I_L Quiescent current	V_{DD} = 5V				
	at T_{amb}=-55°C			5	μA
	at T_{amb}= 25°C		0.5	5	μA
	at T_{amb}=125°C			300	μA
	V_{DD} = 10V				
	at T_{amb}=-55°C			10	μA
	at T_{amb}= 25°C		1	10	μA
	at T_{amb}=125°C			600	μA
V_{OH} Output high voltage	V_{DD} = 5V				
	at T_{amb}=-55°C	4.99			V
	at T_{amb}= 25°C	4.99	5		V
	at T_{amb}=125°C	4.95			V
	V_{DD}= 10V				
	at T_{amb}=-55°C	9.99			V
	at T_{amb}= 25°C	9.99	10		V
	at T_{amb}=125°C	9.95			V
V_{OL} Output low voltage	V_{DD} = 5V or 10V				
	at T_{amb}=-55°C			0.01	V
	at T_{amb}= 25°C		0	0.01	V
	at T_{amb}=125°C			0.05	V
V_{NH} Noise immunity	V_{DD} = 5V V_o = 4.2 V				
	at T_{amb}=-55°C	1.4			V
	at T_{amb}= 25°C	1.5	2.25		V
	at T_{amb}=125°C	1.5			V
	V_{DD} = 10V V_o = 9 V				
	at T_{amb}=-55°C	2.9			V
	at T_{amb}= 25°C	3	4.5		V
	at T_{amb}=125°C	3			V

STATIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{NL}	Noise immunity	V_{DD} = 5V V_o = 0.8V				
		at T_{amb}=-55°C	1.5			V
		at T_{amb}= 25°C	1.5	2.25		V
		at T_{amb}=125°C	1.4			V
		V_{DD} = 10V V_o = 1V				
		at T_{amb}=-55°C	3			V
		at T_{amb}= 25°C	3		4.5	V
		at T_{amb}=125°C	2.9			V
I_DN	Output drive current N-channel	V_{DD} = 5V V_o = 0.5V				
		at T_{amb}=-55°C	0.15			mA
		at T_{amb}= 25°C	0.12		0.3	mA
		at T_{amb}=125°C	0.085			mA
		V_{DD} = 10V V_o = 0.5V				
		at T_{amb}=-55°C	0.31			mA
		at T_{amb}= 25°C	0.25		0.3	mA
		at T_{amb}=125°C	0.175			mA
I_DP	Output drive current P-channel	V_{DD} = 5V V_o = 4.5V				
		at T_{amb}=-55°C	-0.1			mA
		at T_{amb}= 25°C	-0.08		-0.16	mA
		at T_{amb}=125°C	-0.055			mA
		V_{DD} = 10V V_o = 9.5V				
		at T_{amb}=-55°C	-0.25			mA
		at T_{amb}= 25°C	-0.20		-0.44	mA
		at T_{amb}=125°C	-0.14			mA
I_i	Input current	T_{amb} = 25°C		10		pA

HBF types (standard temperature range)

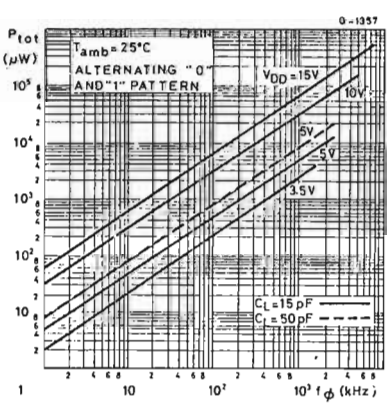
I_L	Quiescent current	V_{DD} = 5V				
		at T_{amb}=-40°C			50	µA
		at T_{amb}= 25°C		0.5	50	µA
		at T_{amb}= 85°C			700	µA

STATIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_L	Quiescent current	V_{DD} = 10V				
		at T_{amb}=-40°C			100	μA
		at T_{amb}= 25°C		1	100	μA
		at T_{amb}= 85°C			1400	μA
V_{OH}	Output high voltage	V_{DD} = 5V				
		at T_{amb}=-40°C	4.99			V
		at T_{amb}= 25°C	4.99	5		V
		at T_{amb}= 85°C	4.95			V
		V_{DD} = 10V				
		at T_{amb}=-40°C	9.99			V
		at T_{amb}= 25°C	9.99	10		V
		at T_{amb}= 85°C	9.95			V
V_{OL}	Output low voltage	V_{DD}= 5V or 10V				
		at T_{amb}=-40°C			0.01	V
		at T_{amb}= 25°C		0	0.01	V
		at T_{amb}= 85°C			0.05	V
V_{NH}	Noise immunity	V_{DD} = 5V V_o = 4.2V				
		at T_{amb}=-40°C	1.4			V
		at T_{amb}= 25°C	1.5	2.25		V
		at T_{amb}= 85°C	1.5			V
		V_{DD} = 10V V_o = 9V				
		at T_{amb}=-40°C	2.9			V
		at T_{amb}= 25°C	3	4.5		V
		at T_{amb}= 85°C	3			V
V_{NL}	Noise immunity	V_{DD} = 5V V_o = 0.8V				
		at T_{amb}=-40°C	1.5			V
		at T_{amb}= 25°C	1.5	2.25		V
		at T_{amb}= 85°C	1.4			V

STATIC ELECTRICAL CHARACTERISTICS (continued)

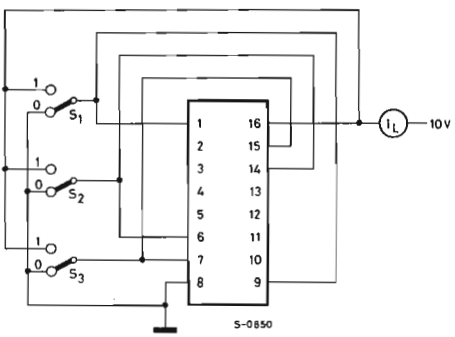
Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{NL}	Noise immunity	V_{DD} = 10V V_o = 1V				
		at T_{amb}=-40°C	3			V
		at T_{amb}= 25°C	3		4.5	V
		at T_{amb}= 85°C	2.9			V
I_DN	Output drive current N-channel	V_{DD} = 5V V_o = 0.5V				
		at T_{amb}=-40°C	0.072			mA
		at T_{amb}= 25°C	0.06		0.3	mA
		at T_{amb}= 85°C	0.05			mA
		V_{DD} = 10V V_o = 0.5V				
		at T_{amb}=-40°C	0.12			mA
		at T_{amb}= 25°C	0.1		0.5	mA
		at T_{amb}= 85°C	0.08			mA
I_DP	Output drive current P-channel	V_{DD} = 5V V_o = 4.5V				
		at T_{amb}=-40°C	-0.06			mA
		at T_{amb}= 25°C	-0.05		-0.16	mA
		at T_{amb}= 85°C	-0.04			mA
		V_{DD} = 10V V_o = 9.5V				
		at T_{amb}=-40°C	-0.12			mA
		at T_{amb}= 25°C	-0.1		-0.44	mA
		at T_{amb}= 85°C	-0.08			mA
I_i	Input current	T_{amb} = 25°C		10		pA



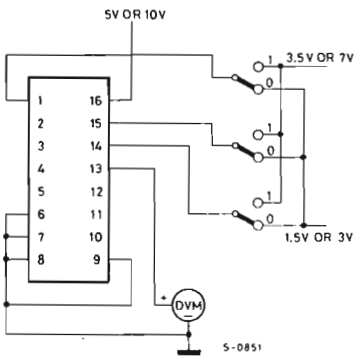
Typical power dissipation characteristics

TEST CIRCUITS

Quiescent device current



Noise immunity



Test performed with the following sequence of "1's" and "0's"

	S_1	S_2	S_3
Test	0	1	0
Don't Test	0	0	1
Don't Test	1	0	1
Don't Test	0	0	0
Don't Test	1	0	0
Don't Test	0	0	1
Test	1	0	1
Don't Test	0	0	0
Test	1	0	0

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}=25°C, C_L= 15pF, typical temperature coefficient for all V_{DD} = 0.3%/°C values)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
CLOCKED OPERATION					
t_{PLH}, t_{PHL} Propagation delay time	V_{DD} = 5 V				
	for **HBC** types		300	750	ns
	for **HBF** types		300	1000	ns
	V_{DD} = 10 V				
	for **HBC** types		100	225	ns
	for **HBF** types		100	300	ns

DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
t_{TLH}, t_{THL}	Transition time	V_{DD} = 5V				
		for **HBC** types		150	300	ns
		for **HBF** types		150	400	ns
		V_{DD} = 10V				
		for **HBC** types		75	125	ns
		for **HBF** types		75	150	ns
t_{pwH}, t_{pwL}	Minimum clock pulse width	V_{DD} = 5V				
		for **HBC** types		200	500	ns
		for **HBF** types		200	830	ns
		V_{DD} = 10V				
		for **HBC** types		100	175	ns
		for **HBF** types		100	200	ns
$t\phi_r$, $t\phi_f$	Clock rise and fall time	V_{DD} = 5V or 10V for **HBC** and **HBF** types			15	μs
t_s	Set-up time	V_{DD} = 5V				
		for **HBC** types		100	350	ns
		for **HBF** types		100	500	ns
		V_{DD} = 10V				
		for **HBC** types		50	80	ns
		for **HBF** types		50	100	ns
f_{max}	Maximum clock frequency	V_{DD} = 5V				
		for **HBC** types	1	2.5		MHz
		for **HBF** types	0.6	2.5		MHz
		V_{DD} = 10V				
		for **HBC** types	3	5		MHz
		for **HBF** types	2.5	5		MHz
C_I	Input capacitance	Any input for **HBC** and **HBF** types		5		pF

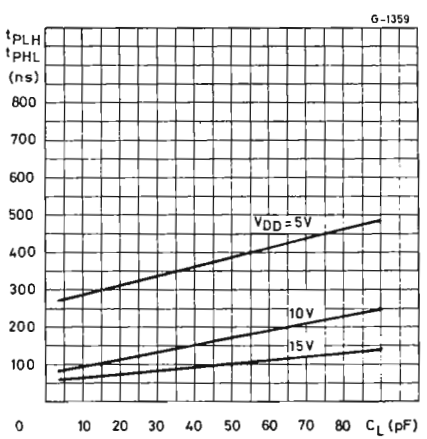
RESET OPERATION

t_{PHL}(R)	Propagation delay time	V_{DD} = 5V				
		for **HBC** types		300	750	ns
		for **HBF** types		300	1000	ns

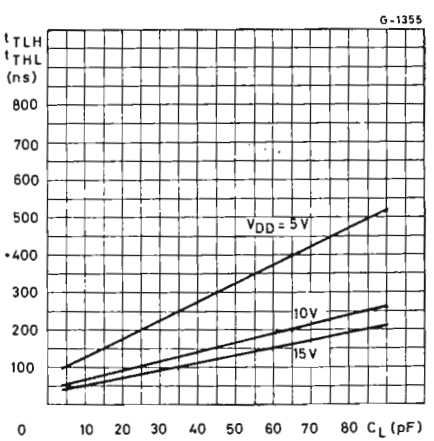
DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

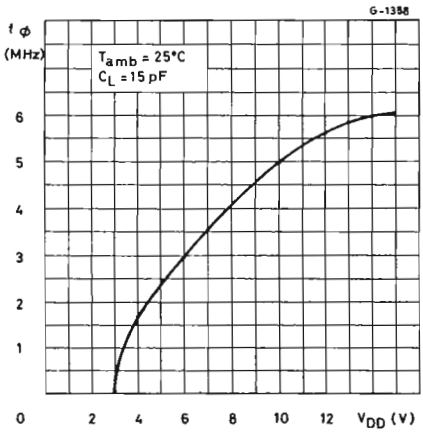
Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{PHL}(R) Propagation delay time	V_{DD} = 10V				
	for **HBC** types		100	225	ns
	for **HBF** types		100	300	ns
t_{pwH}(R) Minimum set and reset pulse width	V_{DD} = 5V				
	for **HBC** types		200	500	ns
	for **HBF** types		200	830	ns
	V_{DD} = 10V				
	for **HBC** types		100	175	ns
	for **HBF** types		100	200	ns

Typical propagation delay time vs. C_L



Typical transition time vs. C_L





Typical clock frequency vs. V_{DD}

COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

QUAD BILATERAL SWITCH

- LOW QUIESCENT POWER DISSIPATION
- WIDE RANGE of DIGITAL and ANALOG SIGNAL LEVELS: DIGITAL or ANALOG SIGNAL to 15V PEAK, ANALOG SIGNAL ± 7.5V PEAK
- LOW "ON" RESISTANCE: 300 Ω (TYP.) OVER 15V p.p. SIGNAL INPUT RANGE for V_{DD}-V_{SS} = 15V
- MATCHED SWITCH CHARACTERISTICS: 40 Ω (TYP.) DIFFERENCE BETWEEN R_{ON} VALUES at a FIXED BIAS POINT OVER 15V p.p. SIGNAL INPUT RANGE for V_{DD}-V_{SS} = 15V
- HIGH "ON-OFF" OUTPUT VOLTAGE RATIO: 65 dB (TYP.) at f_i = 10 kHz, R_L = 10 kΩ
- HIGH DEGREE of LINEARITY: < 0.5% DISTORTION (TYP.) at f_i = 1kHz, V_i = 5V p.p., V_{DD}-V_{SS} ⩾ 10V, R_L = 10 kΩ
- EXTREMELY LOW "OFF" SWITCH LEAKAGE RESULTING in VERY LOW OFFSET CURRENT and HIGH EFFECTIVE "OFF" RESISTANCE: 10 pA (TYP.), V_{DD}-V_{SS} = 10V, T_{amb} = 25°C
- EXTREMELY HIGH CONTROL INPUT IMPEDANCE (CONTROL CIRCUIT ISOLATED from SIGNAL CIRCUIT): 10^{12} Ω (TYP.)
- TRANSMITS FREQUENCIES UP to 10MHz
- MATCHED CONTROL-INPUT to SIGNAL-OUTPUT CAPACITANCE: REDUCES OUTPUT SIGNAL TRANSIENTS

The **HBC 4016**A (extended temperature range) and **HBF 4016A** (standard temperature range) are monolithic integrated circuits, available in 14-lead dual in-line plastic or ceramic package and ceramic flat package.

ABSOLUTE MAXIMUM RATINGS

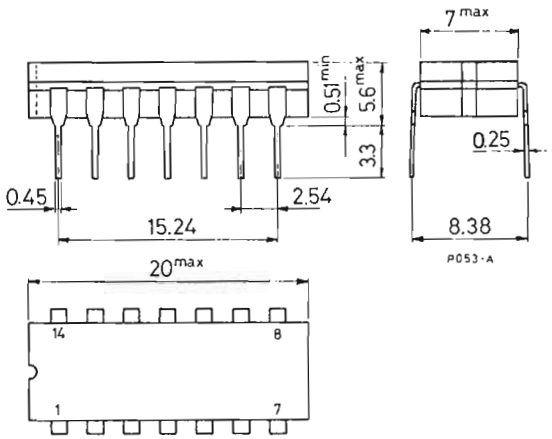
V_{DD}-V_{SS}	Supply voltage	-0.5 to 15	V
V_i	Input voltage	$V_{SS} \leqslant V_I \leqslant V_{DD}$	
P_{tot}	Total power dissipation (per package)	200	mW
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature: for **HBC** types	-55 to 125	°C
	for **HBF** types	-40 to 85	°C

ORDERING NUMBERS :

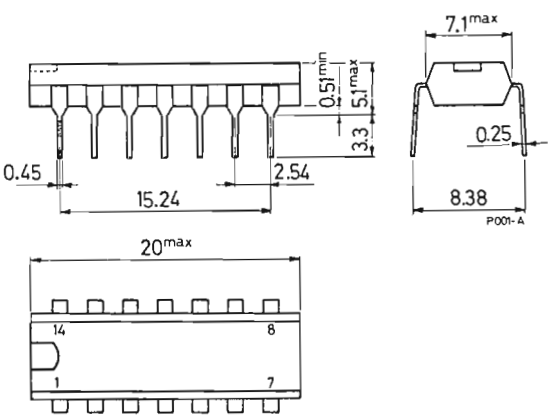
HBC 4016 AD for dual in-line ceramic package
HBC 4016 AF for dual in-line ceramic package frit seal, (extended temperature range)
HBC 4016 AK for ceramic flat package
HBF 4016 AE for dual in-line plastic package
HBF 4016 AF for dual in-line ceramic package frit seal, (standard temperature range)

MECHANICAL DATA (dimensions in mm)

Dual in-line ceramic package
for HBC 4016 AD and
HBC/HBF 4016 AF

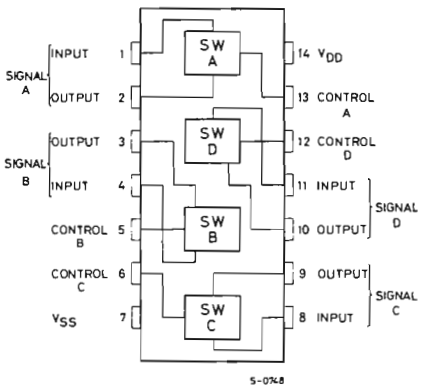


Dual in-line plastic package
(similar to TO-116)
for HBF 4016 AE

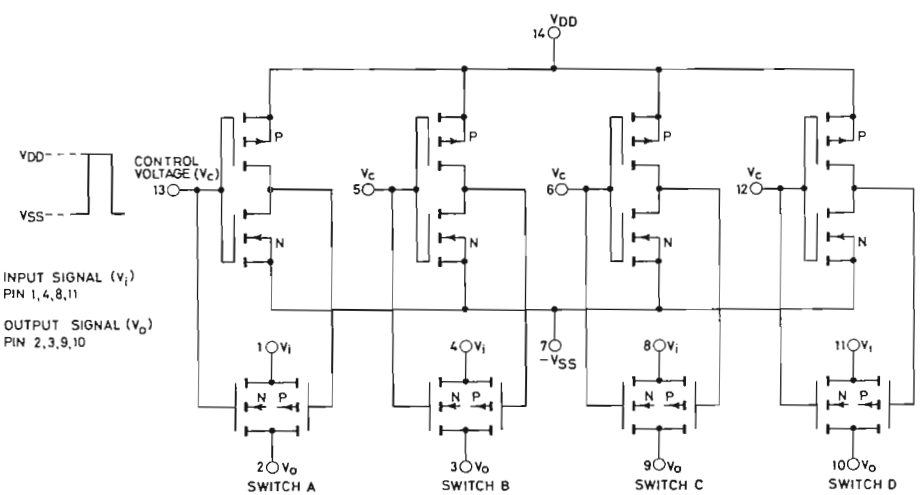


Ceramic flat package for HBC 4016 AK

CONNECTION DIAGRAM (top view)



SCHEMATIC DIAGRAM



NOTE: All switch P-channell substrates are internally connected to PIN 14
All switch N-channell substrates are internally connected to PIN 7

5-0741

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage		3 to 15 V
V_i*	Input voltage		V_{DD} to V_{SS}
	Control line biasing:	Switch "ON"	V_C "1" = V_{DD}
		Switch "OFF"	V_C "0" = V_{SS}
	Signal level range		$V_{SS} \leqslant V_i \leqslant V_{DD}$
T_{op}	Operating temperature range:	for **HBC** types	-55 to 125 °C
		for **HBF** types	-40 to 85 °C

*This is measured with respect to the V_{SS} pin voltage

STATIC ELECTRICAL CHARACTERISTICS

Parameter	Test conditions	Min.	Typ.	Max.	Unit
HBC types (extended temperature range)					
I_L Quiescent current (switch "ON" and "OFF")	V_{DD}= 10V				
	at T_{amb}= -55°C			0.5	μA
	at T_{amb}= 25°C		0.01	0.5	μA
	at T_{amb}= 125°C			30	μA
SWITCH					
R_{ON} "ON" resistance	V_C=V_{DD}=5V V_{SS}= -5V R_L= 10 kΩ V_i = ± 0.25V				
	at T_{amb}= -55°C		325	1870	Ω
	at T_{amb}= 25°C		580	2000	Ω
	at T_{amb}= 125°C		900	2600	Ω
	V_i = ± 5V				
	at T_{amb}= -55°C		130	600	Ω
	at T_{amb}= 25°C		250	660	Ω
	at T_{amb}= 125°C		400	960	Ω

STATIC ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
R_{ON} "ON" resistance	$V_C=V_{DD}=7.5V$ $V_{SS}=-7.5V$ $R_L=10\ k\Omega$ $V_I=\pm 0.25V$				
	at $T_{amb}=-55°C$		130	775	Ω
	at $T_{amb}=25°C$		280	850	Ω
	at $T_{amb}=125°C$		470	1230	Ω
	$V_I=\pm 7.5V$				
	at $T_{amb}=-55°C$		120	360	Ω
	at $T_{amb}=25°C$		200	400	Ω
	at $T_{amb}=125°C$		300	600	Ω
	$V_C=V_{DD}=10V$ $V_{SS}=0V$ $R_L=10\ k\Omega$ $V_I=0.25V$ or $10V$				
	at $T_{amb}=-55°C$		130	600	Ω
	at $T_{amb}=25°C$		250	660	Ω
	at $T_{amb}=125°C$		400	960	Ω
	$V_i=5.6V$				
	at $T_{amb}=-55°C$		300	1870	Ω
	at $T_{amb}=25°C$		560	2000	Ω
	at $T_{amb}=125°C$		880	2600	Ω
	$V_C=V_{DD}=15V$ $V_{SS}=0V$ $R_L=10\ k\Omega$ $V_i=0.25V$ or $15V$				
	at $T_{amb}=-55°C$		120	360	Ω
	at $T_{amb}=25°C$		200	400	Ω
	at $T_{amb}=125°C$		300	600	Ω
	$V_i=9.3V$				
	at $T_{amb}=-55°C$		150	775	Ω
	at $T_{amb}=25°C$		300	850	Ω
	at $T_{amb}=125°C$		490	1230	Ω

STATIC ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
ΔR_{ON} Δ "ON" resistance (between any 2 switches)	$V_C = V_{DD} = 5V$ $V_{SS} = -5V$ $R_L = 10k\Omega$ $V_i = \pm 5V$ at $T_{amb} = 25°C$		15		Ω
	$V_C = V_{DD} = 7.5V$ $V_{SS} = -7.5V$ $R_L = 10k\Omega$ $V_i = \pm 7.5V$ at $T_{amb} = 25°C$		10		Ω
R_{OFF} "OFF" resistance	$V_{DD} = 10V$ $V_C = V_{SS} = 0V$ at $T_{amb} = 25°C$		10^{11}		Ω
CONTROL					
V_{THO} Threshold voltage	$V_{DD} = 5V$ to $15V$ $V_{SS} = 0V$ $I_i = 10\mu A$				
	at $T_{amb} = -55°C$	0.7		2.9	V
	at $T_{amb} = 25°C$	0.5	1.5	2.7	V
	at $T_{amb} = 125°C$	0.2		2.4	V
I_i Input current	$V_{DD} = V_I = 10V$ $V_{SS} = 0V$ at $T_{amb} = 25°C$		±10		pA

HBF types (standard temperature range)

I_L Quiescent current (switch "ON" and "OFF")	$V_{DD} = 10V$				
	at $T_{amb} = -40°C$			0.5	μA
	at $T_{amb} = 25°C$		0.01	0.5	μA
	at $T_{amb} = 85°C$			8	μA

STATIC ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
SWITCH					
R_{ON} "ON" resistance	$V_C = V_{DD} = 5V$ $V_{SS} = -5V$ $R_L = 10k\Omega$ $V_i = \pm 0.25V$				
	at $T_{amb} = -40°C$		370	1900	Ω
	at $T_{amb} = 25°C$		580	2000	Ω
	at $T_{amb} = 85°C$		770	2380	Ω
	$V_i = \pm 5V$				
	at $T_{amb} = -40°C$		150	610	Ω
	at $T_{amb} = 25°C$		250	660	Ω
	at $T_{amb} = 85°C$		340	840	Ω
	$V_C = V_{DD} = 7.5V$ $V_{SS} = -7.5V$ $R_L = 10k\Omega$ $V_i = \pm 0.25V$				
	at $T_{amb} = -40°C$		160	790	Ω
	at $T_{amb} = 25°C$		280	850	Ω
	at $T_{amb} = 85°C$		400	1080	Ω
	$V_i = \pm 7.5V$				
	at $T_{amb} = -40°C$		130	370	Ω
	at $T_{amb} = 25°C$		200	400	Ω
	at $T_{amb} = 85°C$		260	520	Ω
	$V_C = V_{DD} = 10V$ $V_{SS} = 0V$ $R_L = 10k\Omega$ $V_i = 0.25V$				
	at $T_{amb} = -40°C$		150	610	Ω
	at $T_{amb} = 25°C$		250	660	Ω
	at $T_{amb} = 85°C$		340	840	Ω
	$V_i = 5.6V$				
	at $T_{amb} = -40°C$		350	1900	Ω
	at $T_{amb} = 25°C$		560	2000	Ω
	at $T_{amb} = 85°C$		750	2380	Ω
	$V_i = 10V$				
	at $T_{amb} = -40°C$		150	610	Ω
	at $T_{amb} = 25°C$		250	660	Ω
	at $T_{amb} = 85°C$		340	840	Ω

STATIC ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
ΔR_{ON} Δ "ON" resistance (between any 2 switches)	$V_C = V_{DD} = 5V$ $V_{SS} = -5V$ $R_L = 10k\,\Omega$ $V_i = \pm 5V$ at $T_{amb} = 25°C$		15		Ω
	$V_C = V_{DD} = 7.5V$ $V_{SS} = -7.5V$ $R_L = 10k\,\Omega$ $V_i = \pm 7.5V$ at $T_{amb} = 25°C$		10		Ω
R_{OFF} "OFF" resistance	$V_{DD} = 10V$ $V_C = V_{SS} = 0V$ at $T_{amb} = 25°C$		10^{11}		Ω
CONTROL					
V_{THO} Threshold voltage	$V_{DD} = 5V$ to $15V$ $V_{SS} = 0V$ $I_i = 10\,\mu A$ at $T_{amb} = 25°C$	0.5	1.5	2.7	V
I_i Input current	$V_{DD} = V_i = 10V$ $V_{SS} = 0V$ at $T_{amb} = 25°C$		± 10		pA

Fig. 1 - Test circuit

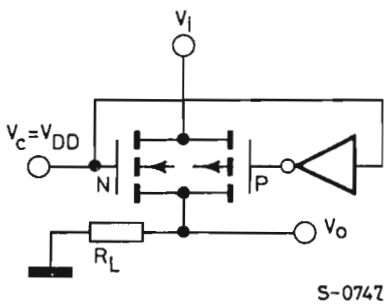


Fig. 2 - Typical "ON" characteristics for 1 of 4 switches with (V_{DD} = 15V, V_{SS} = 0V)

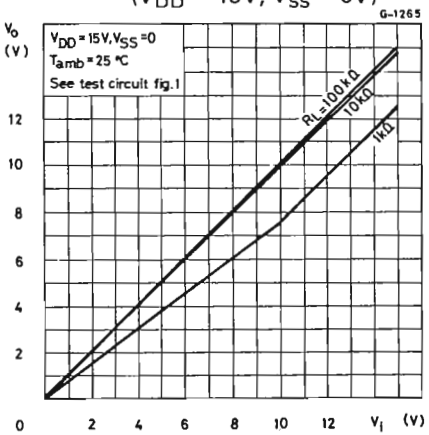


Fig. 3 - Typical "ON" characteristics for 1 of 4 switches with (V_{DD} = 10V, V_{SS} = 0V)

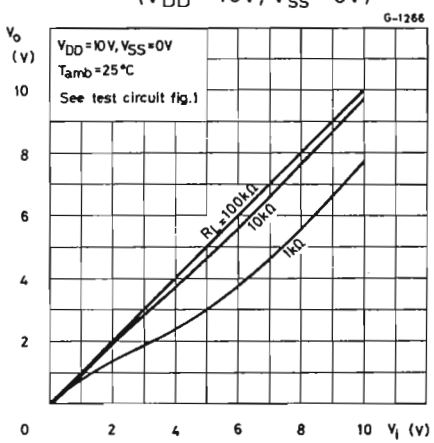


Fig. 4 - Typical "ON" characteristics for 1 of 4 switches with (V_{DD} = 5V, V_{SS} = 0V)

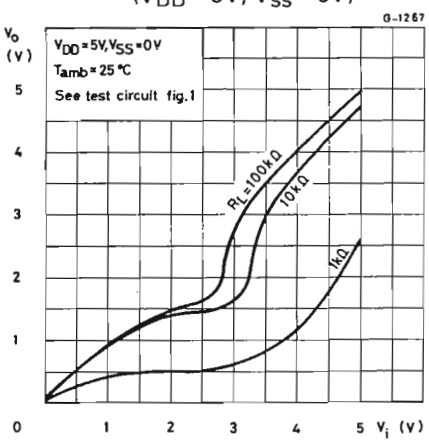


Fig. 5 - Typical "ON" characteristics for 1 of 4 switches with (V_{DD}= 7.5V, V_{SS}= -7.5V)

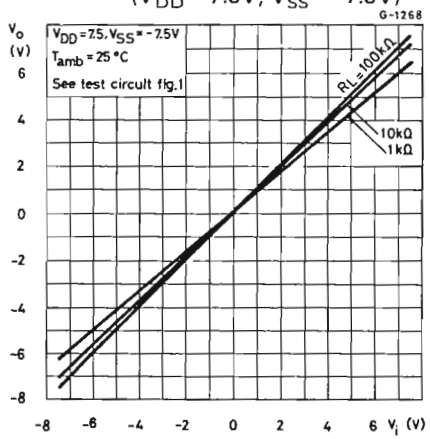


Fig. 6 - Typical "ON" characteristics for 1 of 4 switches with (V_{DD}= 5V, V_{SS}= -5V)

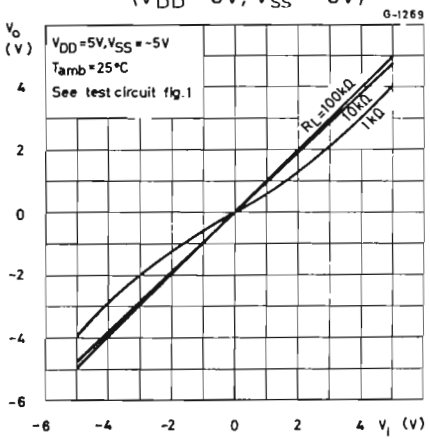


Fig. 7 - Typical "ON" characteristics for 1 of 4 switches with (V_{DD}= 2.5V, V_{SS}= -2.5V)

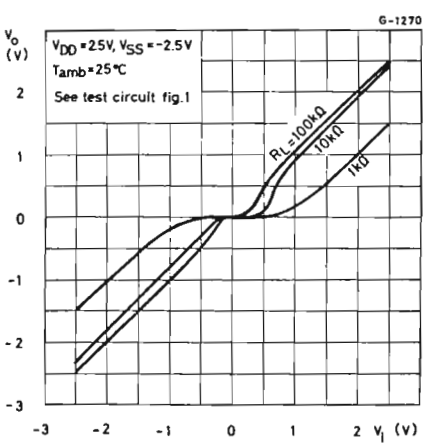
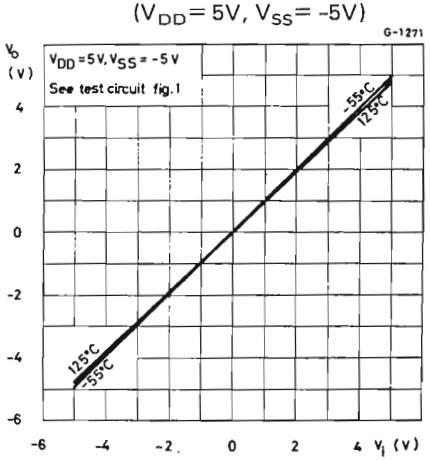


Fig. 8 - Typical "ON" characteristics as a function of temperature for 1 of 4 switches with (V_{DD}= 5V, V_{SS}= -5V)



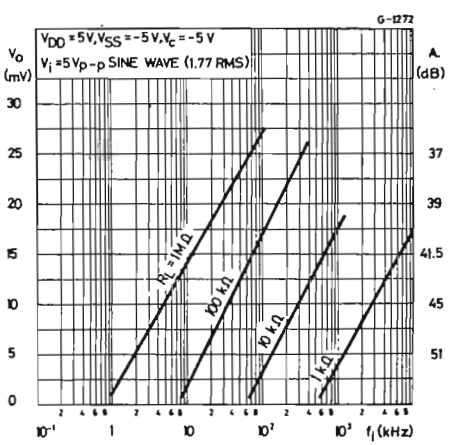
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 15pF, all input rise and fall time = 20 ns)

Parameter		Test conditions	Min.	Typ.	Max.	Unit	Fig.
HBC and **HBF** types							
SWITCH							
d	Sine wave distortion	V_C=V_{DD}=5V V_{SS}=-5V R_L = 10kΩ f = 1kHz V_{IM} = ± 2.5V		0.4		%	
B	Frequency response at -3dB ("ON" state)	V_C=V_{DD}=5V V_{SS}=-5V R_L = 1kΩ V_{iM} = ± 2.5V		40		MHz	11
B	Frequency response at -50dB ("OFF" state)	V_{DD}=5V V_C=V_{SS}=-5V R_L = 1kΩ V_{iM} = ± 2.5V		1.25		MHz	9
	Crosstalk (Between any 2 switches)	V_{DD} =5V V_{SS} = -5V R_L = 1kΩ f = 1MHz V_{iM} = ± 2.5V		45		dB	10
t_{pd}	Propagation delay time	V_C=V_{DD}=10V V_{SS}=0V V_i = 10V		10		ns	13
C_i	Input capacitance	V_{DD}=10V V_C=V_{SS}=0V		4		pF	
C_O	Output capacitance			4		pF	
C	Feedthrough capacitance			0.2		pF	

DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min. Typ. Max.	Unit	Fig.
CONTROL					
	Crosstalk (control input to switch output)	$V_C=V_{DD}=10V$ $V_{SS}=0V$ $R_L = 10k\Omega$ $R_g = 1k\Omega$	50	mV	12
t_{pd}	Propagation delay time (turn-"ON")	$V_I=V_{DD}=10V$ $V_{SS}=0V$ $R_L = 10k\Omega$ $V_C = 10V$ (square wave)	20	ns	14
f_{max}	Maximum frequency (control input)	$V_{DD}=10V$ $V_{SS}=0V$ $R_L = 1k\Omega$ $V_C = 10V$ (square wave)	10	MHz	15
C_i	Input capacitance		5	pF	

Fig. 9 - Typical feedthru vs. frequency and test circuit for switch "OFF"



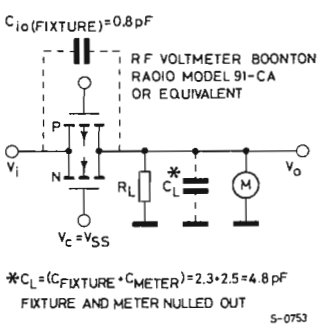


Fig. 10 - Typical crosstalk between two switches in the same package and the test circuit

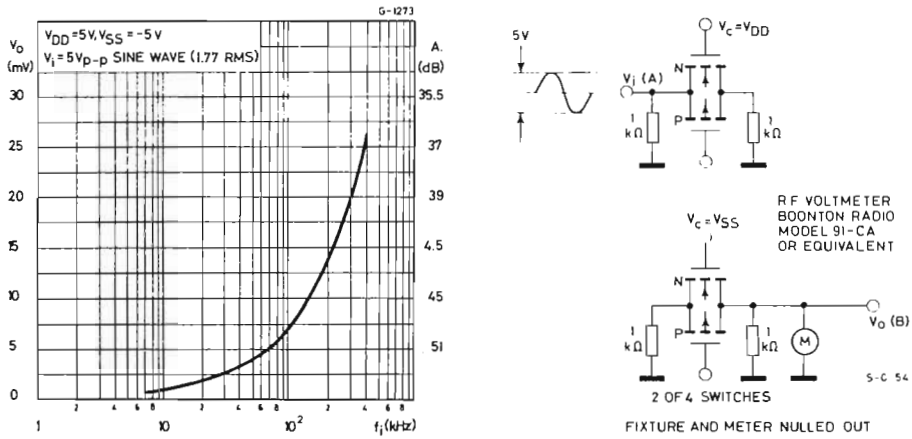
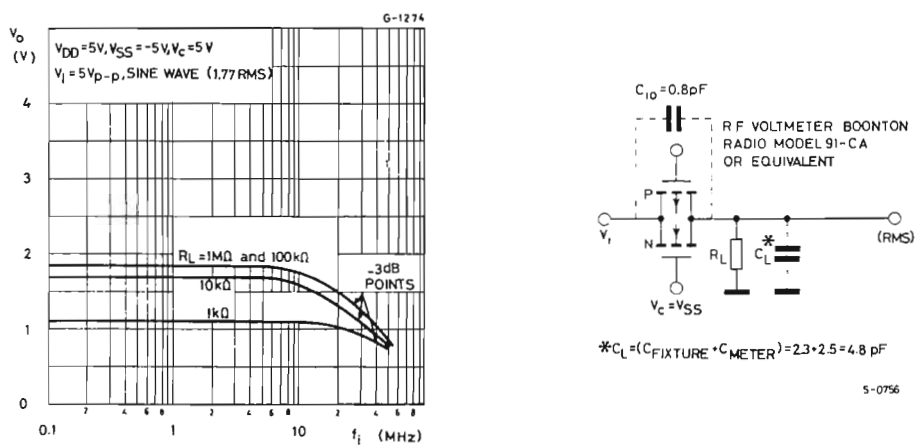


Fig. 11 - Typical switch frequency response and test circuit for switch "ON"



TYPICAL APPLICATIONS (all unused terminals are connected to V_{SS})

Fig. 12 - Crosstalk-control input to signal output

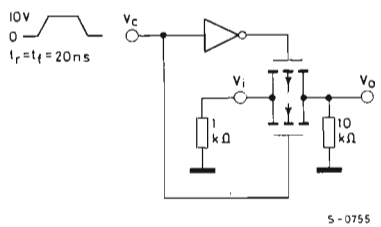


Fig. 13 - Propagation delay time signal input (V_I) to signal output (V_o)

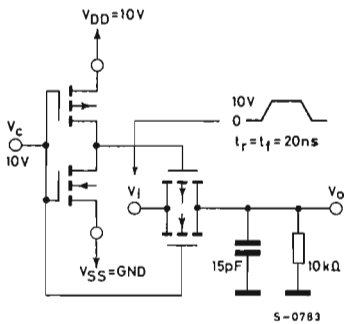


Fig. 14 - Turn-"ON" propagation delay-control input

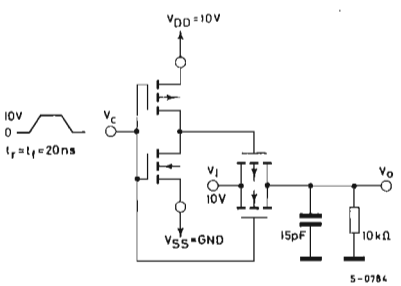
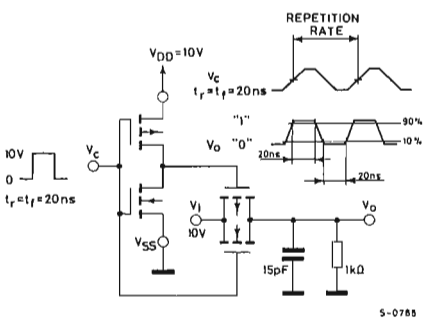


Fig. 15 - Maximum allowable control input repetition rate



COS/MOS INTEGRATED CIRCUIT

HBC/HBF 4017 A

PRELIMINARY DATA

DECADE COUNTER/DIVIDER PLUS 10 DECODED DECIMAL OUTPUTS

- LOW QUIESCENT POWER DISSIPATION
- WIDE SUPPLY VOLTAGE RANGE : 3 to 15 V
- HIGH NOISE IMMUNITY : 45% of V_{DD} (TYP.)
- MEDIUM SPEED OPERATION : 5 MHz (TYP.) at $V_{DD} - V_{SS} = 10V$
- INPUTS FULLY PROTECTED
- HIGH FANOUT
- FULLY STATIC OPERATION

The **HBC 4017A** (extended temperature range) and **HBF 4017A** (standard temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package. They consist of a 5-stage Johnson decade counter and an output decoder which converts the Johnson binary code to a decimal number. Inputs include a "Clock" a "Reset", and a "Clock Enable" signal. Use of the Johnson decade counter configuration permits high speed operation, 2-input decimal decode gating, and spike-free decoded outputs. The ten decoded outputs are normally low, and go high only at their appropriate decimal time period. The output changes occur on the positive-going edge of the clock pulse. This part can be used in frequency division applications as well as decade counter or decimal decode display applications.

ABSOLUTE MAXIMUM RATINGS

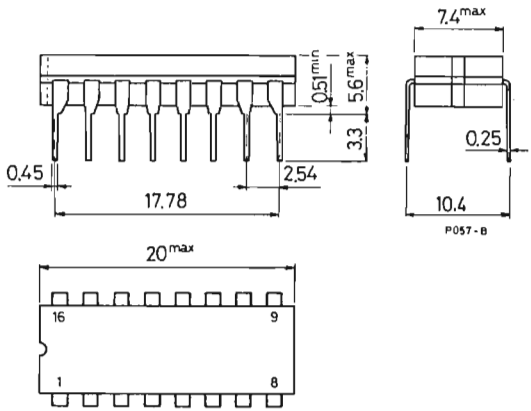
$V_{DD} - V_{SS}$	Supply voltage	-0.5 to 15	V
V_i	Input voltage (at any pin)	$V_{SS} \leqslant V_i \leqslant V_{DD}$	
P_{tot}	Total power dissipation (per package)	200	mW
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature : for **HBC** types	-55 to 125	°C
	for **HBF** types	-40 to 85	°C

ORDERING NUMBERS:

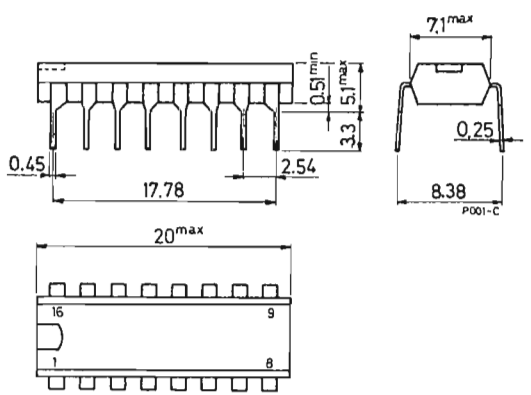
HBC 4017 **AD** for dual in-line ceramic package
HBC 4017 **AF** for dual in-line ceramic package, frit seal (extended temperature range)
HBC 4017 **AK** for ceramic flat package
HBF 4017 **AE** for dual in-line plastic package
HBF 4017 **AF** for dual in-line ceramic package, frit seal (standard temperature range)

MECHANICAL DATA (dimensions in mm)

Dual in-line ceramic package
for HBC 4017 AD and
HBC/HBF 4017 AF

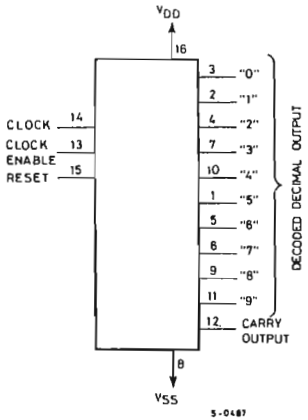


Dual in-line plastic package
for HBF 4017 AE

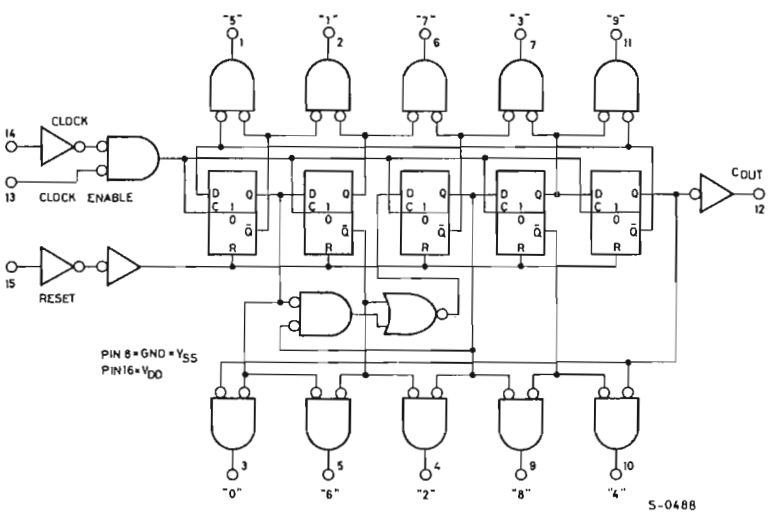


Ceramic flat package for HBC 4017 AK

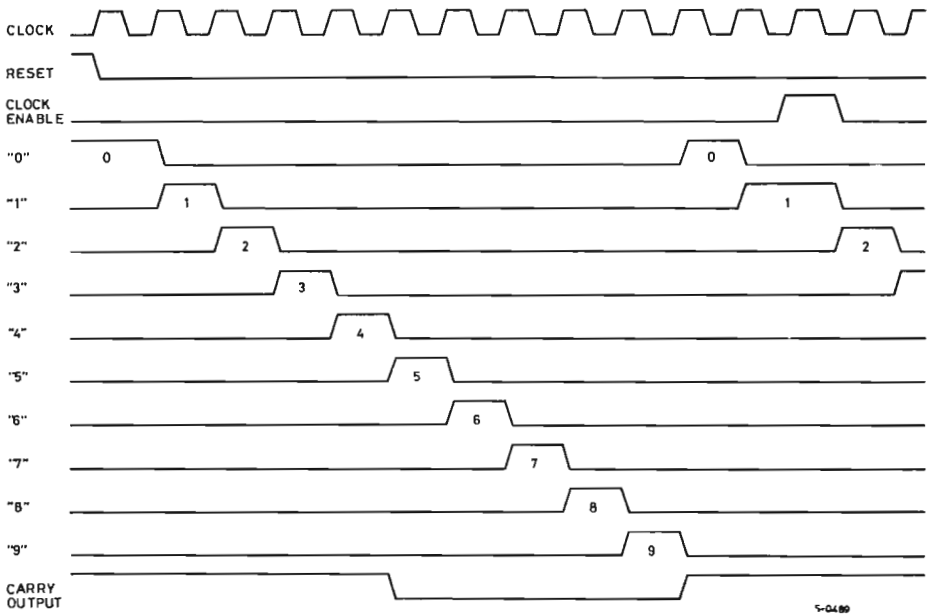
CONNECTION DIAGRAM



LOGIC DIAGRAM



TIMING DIAGRAM



RECOMMENDED OPERATING CONDITIONS

V_{DD} *	Supply voltage		3 to 15	V
V_i *	Input voltage		V_{DD} to V_{SS}	
T_{op}	Operating temperature :	for **HBC** types	-55 to 125	°C
		for **HBF** types	-40 to 85	°C

* This is measured with respect to the V_{SS} pin voltage

STATIC ELECTRICAL CHARACTERISTICS

Parameter		Test conditions	Min.	Typ.	Max.	Unit
HBC types (extended temperature range)						
I_L	Quiescent current	V_{DD} = 5V				
		at T_{amb} = -55°C			5	µA
		at T_{amb} = 25°C		0.3	5	µA
		at T_{amb} = 125°C			300	µA
		V_{DD} = 10V				
		at T_{amb} = -55°C			10	µA
		at T_{amb} = 25°C		0.5	10	µA
		at T_{amb} = 125°C			600	µA
V_{OH}	Output high voltage	I_o = 0				
		V_{DD} = 5V				
		at T_{amb} = -55°C	4.99			V
		at T_{amb} = 25°C	4.99	5		V
		at T_{amb} = 125°C	4.95			V
		V_{DD} = 10V				
		at T_{amb} = -55°C	9.99			V
		at T_{amb} = 25°C	9.99	10		V
		at T_{amb} = 125°C	9.95			V
V_{OL}	Output low voltage	I_o = 0				
		V_{DD} = 5V or 10V				
		at T_{amb} = -55°C			0.01	V
		at T_{amb} = 25°C		0	0.01	V
		at T_{amb} = 125°C			0.05	V
→ V_{NH}	Noise immunity	V_{DD} = 5V V_o = 4.2V				
		at T_{amb} = -55°C	1.4			V
		at T_{amb} = 25°C	1.5	2.25		V
		at T_{amb} = 125°C	1.5			V
		V_{DD} = 10V V_o = 9V				
		at T_{amb} = -55°C	2.9			V
		at T_{amb} = 25°C	3	4.5		V
		at T_{amb} = 125°C	3			V

STATIC ELECTRICAL CHARACTERISTICS (continued)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit
→ V_{NL}	Noise immunity	V_{DD} = 5V V_o = 0.8V				
		at T_{amb} = -55°C	1.5			V
		at T_{amb} = 25°C	1.5	2.25		V
		at T_{amb} = 125°C	1.4			V
		V_{DD} = 10V V_o = 1V				
		at T_{amb} = -55°C	3			V
		at T_{amb} = 25°C	3		4.5	V
		at T_{amb} = 125°C	2.9			V
I_DN	Output drive current N - channel	Decoded outputs				
		V_{DD} = 5V V_o = 0.5V				
		at T_{amb} = -55°C	0.06			mA
		at T_{amb} = 25°C	0.05		0.1	mA
		at T_{amb} = 125°C	0.035			mA
		V_{DD} = 10V V_o = 0.5V				
		at T_{amb} = -55°C	0.12			mA
		at T_{amb} = 25°C	0.1		0.4	mA
		at T_{amb} = 125°C	0.07			mA
		Carry output				
		V_{DD} = 5V V_o = 0.5V				
		at T_{amb} = -55°C	0.185			mA
		at T_{amb} = 25°C	0.15		0.4	mA
		at T_{amb} = 125°C	0.105			mA
		V_{DD} = 10V V_o = 0.5V				
		at T_{amb} = -55°C	0.45			mA
		at T_{amb} = 25°C	0.35		1	mA
		at T_{amb} = 125°C	0.25			mA
I_DP	Output drive current P - channel	Decoded outputs				
		V_{DD} = 5V V_o = 4.5V				
		at T_{amb} = -55°C	-0.0375			mA
		at T_{amb} = 25°C	-0.03		-0.075	mA
		at T_{amb} = 125°C	-0.021			mA
		V_{DD} = 10V V_o = 9.5V				
		at T_{amb} = -55°C	-0.12			mA
		at T_{amb} = 25°C	-0.1		-0.2	mA
		at T_{amb} = 125°C	-0.07			mA

STATIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_DP	Output drive current P - channel	Carry output				
		$V_{DD} = 5V$ $V_o = 4.5V$				
		at $T_{amb} = -55°C$		-0.185		mA
		at $T_{amb} = 25°C$		-0.15	-0.4	mA
		at $T_{amb} = 125°C$		-0.105		mA
		$V_{DD} = 10V$ $V_o = 9.5V$				
		at $T_{amb} = -55°C$		-0.45		mA
		at $T_{amb} = 25°C$		-0.35	-1	mA
		at $T_{amb} = 125°C$		-0.25		mA
I_i	Input current	$T_{amb} = 25°C$		10		pA

HBF types (standard temperature range)

I_L	Quiescent current	$V_{DD} = 5V$				
		at $T_{amb} = -40°C$			50	μA
		at $T_{amb} = 25°C$		0.5	50	μA
		at $T_{amb} = 85°C$			700	μA
		$V_{DD} = 10V$				
		at $T_{amb} = -40°C$			100	μA
		at $T_{amb} = 25°C$		1	100	μA
		at $T_{amb} = 85°C$			1400	μA
V_{OH}	Output high voltage	$I_o = 0$				
		$V_{DD} = 5V$				
		at $T_{amb} = -40°C$	4.99			V
		at $T_{amb} = 25°C$	4.99	5		V
		at $T_{amb} = 85°C$	4.95			V
		$V_{DD} = 10V$				
		at $T_{amb} = -40°C$	9.99			V
		at $T_{amb} = 25°C$	9.99	10		V
		at $T_{amb} = 85°C$	9.95			V
V_{OL}	Output low voltage	$I_o = 0$				
		$V_{DD} = 5V$ or $10V$				
		at $T_{amb} = -40°C$			0.01	V
		at $T_{amb} = 25°C$		0	0.01	V
		at $T_{amb} = 85°C$			0.05	V

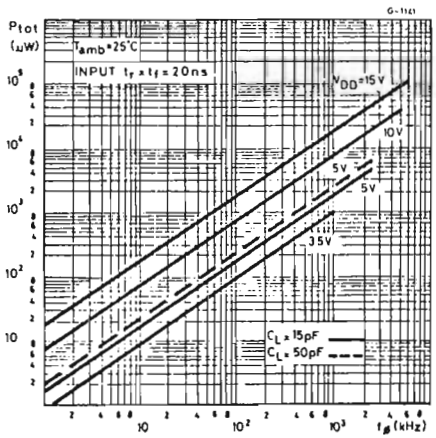
STATIC ELECTRICAL CHARACTERISTICS (continued)

	Parameter		Test conditions	Min.	Typ.	Max.	Unit
→	V_{NH}	Noise immunity	V_{DD} = 5V V_o = 4.2V				
			at T_{amb} = -40°C	1.4			V
			at T_{amb} = 25°C	1.5	2.25		V
			at T_{amb} = 85°C	1.5			V
			V_{DD} = 10V V_o = 9V				
			at T_{amb} = -40°C	2.9			V
			at T_{amb} = 25°C	3		4.5	V
			at T_{amb} = 85°C	3			V
→	V_{NL}	Noise immunity	V_{DD} = 5V V_o = 0.8V				
			at T_{amb} = -40°C	1.5			V
			at T_{amb} = 25°C	1.5	2.25		V
			at T_{amb} = 85°C	1.4			V
			V_{DD} = 10V V_o = 1V				
			at T_{amb} = -40°C	3			V
			at T_{amb} = 25°C	3		4.5	V
			at T_{amb} = 85°C	2.9			V
	I_DN	Output drive current N - channel	Decoded outputs				
			V_{DD} = 5V V_o = 0.5V				
			at T_{amb} = -40°C	0.03			mA
			at T_{amb} = 25°C	0.025	0.1		mA
			at T_{amb} = 85°C	0.02			mA
			V_{DD} = 10V V_o = 0.5V				
			at T_{amb} = -40°C	0.085			mA
			at T_{amb} = 25°C	0.07	0.4		mA
			at T_{amb} = 85°C	0.055			mA
			Carry output				
			V_{DD} = 5V V_o = 0.5V				
			at T_{amb} = -40°C	0.095			mA
			at T_{amb} = 25°C	0.08	0.4		mA
			at T_{amb} = 85°C	0.065			mA
			V_{DD} = 10V V_o = 0.5V				
			at T_{amb} = -40°C	0.3			mA
			at T_{amb} = 25°C	0.25		1	mA
			at T_{amb} = 85°C	0.2			mA

STATIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_DP	Output drive current P - channel	Decoded outputs				
		V_{DD} = 5V V_o = 4.5V				
		at T_{amb} = -40°C		-0.018		mA
		at T_{amb} = 25°C		-0.015	-0.075	mA
		at T_{amb} = 85°C		-0.012		mA
		V_{DD} = 10V V_o = 9.5V				
		at T_{amb} = -40°C		-0.085		mA
		at T_{amb} = 25°C		-0.07	-0.2	mA
		at T_{amb} = 85°C		-0.055		mA
		Carry output				
		V_{DD} = 5V V_o = 4.5V				
		at T_{amb} = -40°C		-0.095		mA
		at T_{amb} = 25°C		-0.08	-0.4	mA
		at T_{amb} = 85°C		-0.065		mA
		V_{DD} = 10V V_o = 9.5V				
		at T_{amb} = -40°C		-0.3		mA
		at T_{amb} = 25°C		-0.24	-1	mA
		at T_{amb} = 85°C		-0.20		mA
I_i	Input current	T_{amb} ≡ 25°C		10		pA

Typical power dissipation characteristics



DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 15 pF, typical temperature coefficient for all V_{DD} = 0.3%/°C values, all input rise and fall time = 20 ns, except $t_{\phi r}$ and $t_{\phi f}$)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
CLOCKED OPERATION					
t_{PLH}, t_{PHL} Propagation delay time	Decode output lines				
	V_{DD} = 5V				
	for **HBC** types		500	1200	ns
	for **HBF** types		500	1600	ns
	V_{DD} = 10V				
	for **HBC** types		200	400	ns
	for **HBF** types		200	500	ns
	Carry output line				
	V_{DD} = 5V				
	for **HBC** types		350	1000	ns
	for **HBF** types		350	1300	ns
	V_{DD} = 10V				
	for **HBC** types		125	250	ns
	for **HBF** types		125	300	ns
t_{TLH}, t_{THL} Transition time	Decode output lines				
	V_{DD} = 5V				
	for **HBC** types		300	900	ns
	for **HBF** types		300	1200	ns
	V_{DD} = 10V				
	for **HBC** types		125	350	ns
	for **HBF** types		125	450	ns
	Carry output line				
	V_{DD} = 5V				
	for **HBC** types		100	300	ns
	for **HBF** types		100	350	ns
	V_{DD} = 10V				
	for **HBC** types		50	150	ns
	for **HBF** types		50	200	ns
t_{pwH}, t_{pwL} Minimum clock pulse width	V_{DD} = 5V				
	for **HBC** types		200	500	ns
	for **HBF** types		200	830	ns
	V_{DD} = 10V				
	for **HBC** types		100	170	ns
	for **HBF** types		100	250	ns

DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
$t_{\phi r}$, $t_{\phi f}$	Clock rise and fall time	V_{DD} = 5V or 10V for **HBC** and **HBF** types			15	μs
t_s	Clock enable set-up time	V_{DD} = 5V				
		for **HBC** types		175	500	ns
		for **HBF** types		175	700	ns
		V_{DD} = 10V				
		for **HBC** types		75	200	ns
		for **HBF** types		75	300	ns
f_{max}	Maximum clock frequency	V_{DD} = 5V				
		for **HBC** types	1	2.5		MHz
		for **HBF** types	0.6	2.5		MHz
		V_{DD} = 10V				
		for **HBC** types	3	5		MHz
		for **HBF** types	2	5		MHz
C_i	Input capacitance	Any input for **HBC** and **HBF** types		5		pF

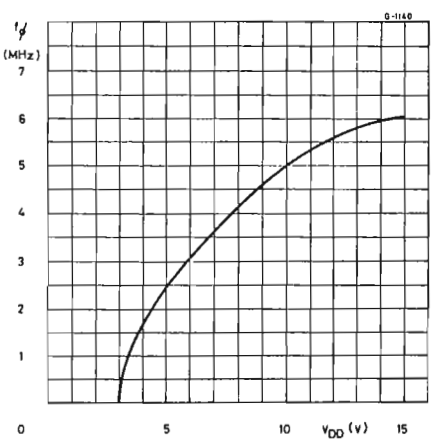
RESET OPERATION

t_{PHL}	Propagation delay time	To decode output lines				
		V_{DD} = 5V				
		for **HBC** types		450	1200	ns
		for **HBF** types		450	1600	ns
		V_{DD} = 10V				
		for **HBC** types		200	400	ns
		for **HBF** types		200	500	ns
		To carry output line				
		V_{DD} = 5V				
		for **HBC** types		350	1000	ns
		for **HBF** types		350	1300	ns
		V_{DD} = 10V				
		for **HBC** types		125	250	ns
		for **HBF** types		125	300	ns

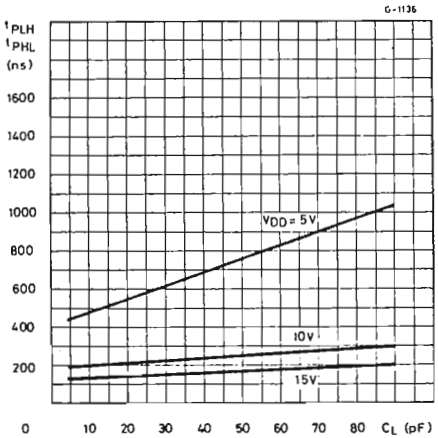
DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
t_{pwH}	Minimum reset pulse width	$V_{DD} = 5V$				
		for **HBC** types		200	500	ns
		for **HBF** types		200	830	ns
		$V_{DD} = 10V$				
		for **HBC** types		100	165	ns
		for **HBF** types		100	250	ns
t_{rem}	Removal time	$V_{DD} = 5V$				
		for **HBC** types		300	750	ns
		for **HBF** types		300	1000	ns
		$V_{DD} = 10V$				
		for **HBC** types		100	225	ns
		for **HBF** types		100	275	ns

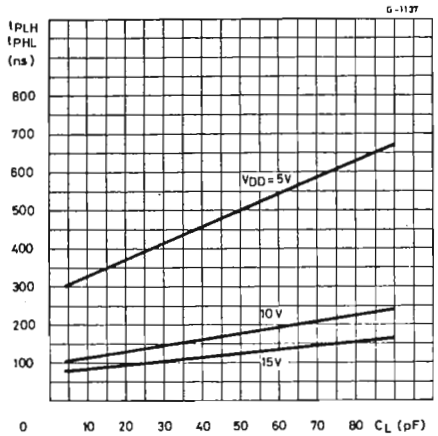
Typical clock frequency vs. V_{DD}



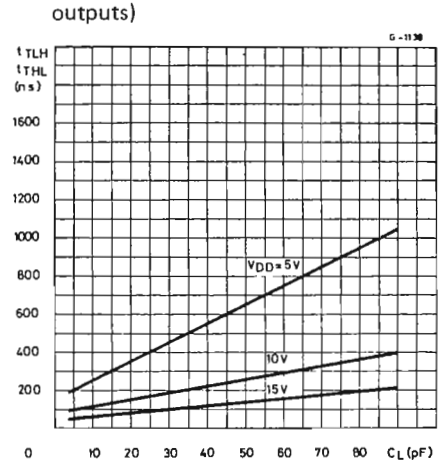
Typical propagation delay time vs. C_L (decoded outputs)



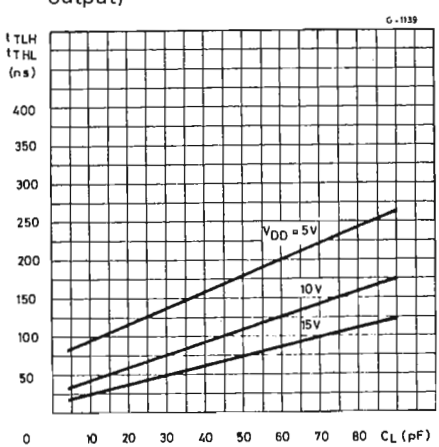
Typical propagation delay time vs. C_L (carry output)



Typical transition time vs. C_L (decoded outputs)



Typical transition time vs. C_L (carry output)



COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

QUAD AND-OR SELECTED GATE

- LOW QUIESCENT POWER DISSIPATION
- WIDE SUPPLY VOLTAGE RANGE: 3 to 15 V
- HIGH NOISE IMMUNITY: 45% of V_{DD} (TYP.)
- MEDIUM SPEED OPERATION: $t_{PHL} = t_{PLH} = 50$ ns (TYP.) at $C_L = 15$ pF
- INPUTS FULLY PROTECTED

The **HBC 4019A** (extended temperature range) and **HBF 4019A** (standard temperature range) are monolithic integrated circuits, available in 16-lead dual in line plastic or ceramic package and ceramic flat package.
The **HBC/HBF 4019A** types are comprised of four "AND-OR select" gate configurations, each consisting of two 2-input AND gates driving a single 2-input OR gate. Selection is accomplished by control bits K_a and K_b. In addition to selection of either channel A or channel B information, the control bits can be applied simultaneously to accomplish the logical A + B function.

ABSOLUTE MAXIMUM RATINGS

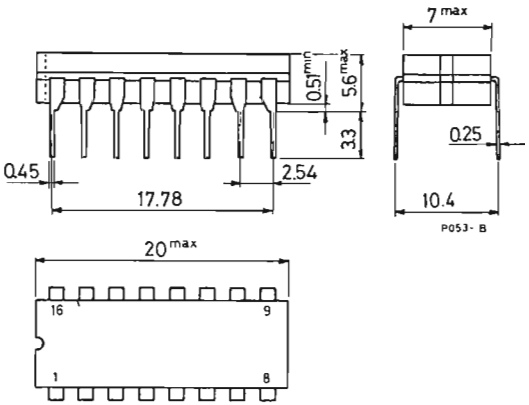
$V_{DD}-V_{SS}$	Supply voltage	-0.5 to 15	V
V_i	Input voltage (at any pin)	$V_{SS} \leqslant V_i \leqslant V_{DD}$	
P_{tot}	Total power dissipation (per package)	200	mW
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature: for **HBC** types	-55 to 125	°C
	for **HBF** types	-40 to 85	°C

ORDERING NUMBERS:

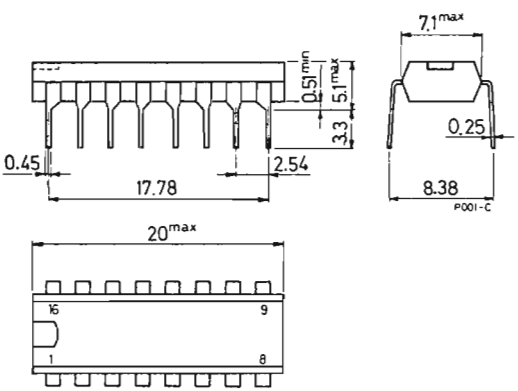
HBC 4019 AD for dual in-line ceramic package
HBC 4019 AF for dual in-line ceramic package, frit seal (extended temperature range)
HBC 4019 AK for ceramic flat package
HBF 4019 AE for dual in-line plastic package
HBF 4019 AF for dual in-line ceramic package, frit seal (standard temperature range)

MECHANICAL DATA (dimensions in mm)

Dual in-line ceramic package
for HBC 4019 AD and
HBC/HBF 4019 AF

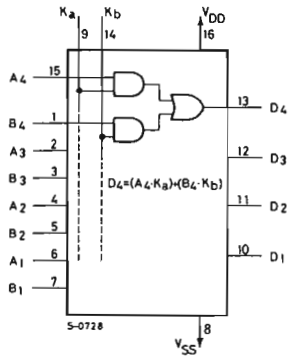


Dual in-line plastic package
for HBF 4019 AE



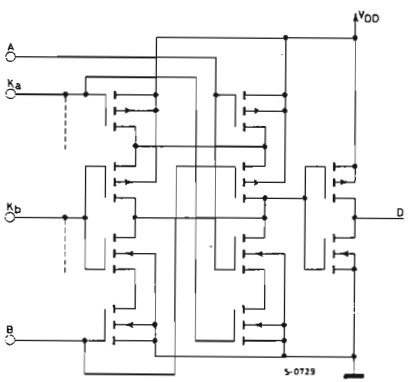
Ceramic flat package for HBC 4019 AK

CONNECTION DIAGRAM



SCHEMATIC DIAGRAM

For 1 of 4 identical stages



RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage		3 to 15	V
V_i*	Input voltage		V_{DD} to V_{SS}	
T_{op}	Operating temperature:	for **HBC** types	-55 to 125	°C
		for **HBF** types	-40 to 85	°C

*This is measured with respect to the V_{SS} pin voltage

STATIC ELECTRICAL CHARACTERISTICS

Parameter		Test conditions	Min.	Typ.	Max.	Unit
HBC types (extended temperature range)						
I_L	Quiescent current	$V_{DD} = 5V$				
		at $T_{amb} = -55°C$			5	μA
		at $T_{amb} = 25°C$		0.03	5	μA
		at $T_{amb} = 125°C$			300	μA
		$V_{DD} = 10V$				
		at $T_{amb} = -55°C$			10	μA
		at $T_{amb} = 25°C$		0.05	10	μA
		at $T_{amb} = 125°C$			600	μA
V_{OH}	Output high voltage	$I_o = 0$				
		$V_{DD} = 5V$				
		at $T_{amb} = -55°C$	4.99			V
		at $T_{amb} = 25°C$	4.99	5		V
		at $T_{amb} = 125°C$	4.95			V
		$V_{DD} = 10V$				
		at $T_{amb} = -55°C$	9.99			V
		at $T_{amb} = 25°C$	9.99	10		V
		at $T_{amb} = 125°C$	9.95			V
V_{OL}	Output low voltage	$I_o = 0$				
		$V_{DD} = 5V$ or $10V$				
		at $T_{amb} = -55°C$			0.01	V
		at $T_{amb} = 25°C$		0	0.01	V
		at $T_{amb} = 125°C$			0.05	V
V_{NH}	Noise immunity	$V_{DD} = 5V$ $V_o = 3.6V$				
		at $T_{amb} = -55°C$	1.4			V
		at $T_{amb} = 25°C$	1.5	2.25		V
		at $T_{amb} = 125°C$	1.5			V
		$V_{DD} = 10V$ $V_o = 7.2V$				
		at $T_{amb} = -55°C$	2.9			V
		at $T_{amb} = 25°C$	3	4.5		V
		at $T_{amb} = 125°C$	3			V

STATIC ELECTRICAL CHARACTERISTICS (continued)

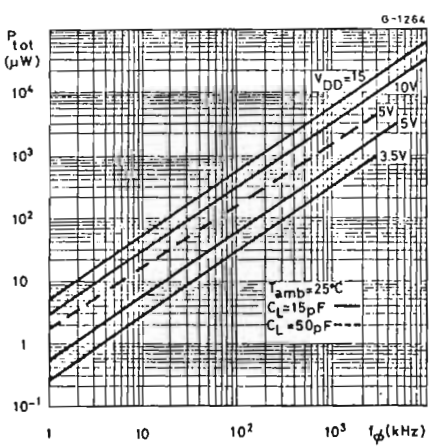
Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{NL}	Noise immunity	V_{DD}= 5V V_o = 0.95V				
		at T_{amb}= -55°C	1.5			V
		at T_{amb}= 25°C	1.5	2.25		V
		at T_{amb}= 125°C	1.4			V
		V_{DD}= 10V V_o = 2.9V				
		at T_{amb}= -55°C	3			V
		at T_{amb}= 25°C	3		4.5	V
		at T_{amb}= 125°C	2.9			V
I_DN	Output drive current N-channel	V_{DD} = 5V V_o = 0.5V				
		at T_{amb}= -55°C	0.6			mA
		at T_{amb}= 25°C	0.45	0.9		mA
		at T_{amb}= 125°C	0.30			mA
		V_{DD}=10V V_o = 0.5V				
		at T_{amb}= -55°C	0.9			mA
		at T_{amb}= 25°C	0.75	1.5		mA
		at T_{amb}= 125°C	0.55			mA
I_DP	Output drive current P-channel	V_{DD} = 5V V_o = 4.5V				
		at T_{amb}= -55°C	-0.31			mA
		at T_{amb}= 25°C	-0.25	-0.5		mA
		at T_{amb}= 125°C	-0.175			mA
		V_{DD} =10V V_o = 9.5V				
		at T_{amb}= -55°C	-0.95			mA
		at T_{amb}= 25°C	-0.7	-1.5		mA
		at T_{amb}= 125°C	-0.5			mA
I_i	Input current	T_{amb} = 25°C		10		pA

HBF types (standard temperature range)

I_L	Quiescent current	V_{DD} = 5V				
		at T_{amb}= -40°C			50	µA
		at T_{amb}= 25°C		0.1	50	µA
		at T_{amb}= 85°C			700	µA

STATIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{NL}	Noise immunity	V_{DD}=10V V_o = 2.9V				
		at T_{amb}= -40°C	3			V
		at T_{amb}= 25°C	3		4.5	V
		at T_{amb}= 85°C	2.9			V
I_DN	Output drive current N-channel	V_{DD} = 5V V_o = 0.5V				
		at T_{amb}= -40°C	0.37			mA
		at T_{amb}= 25°C	0.30		1	mA
		at T_{amb}= 85°C	0.23			mA
		V_{DD}=10V V_o = 0.5V				
		at T_{amb}= -40°C	0.8			mA
		at T_{amb}= 25°C	0.65		1.5	mA
		at T_{amb}= 85°C	0.5			mA
I_DP	Output drive current P-channel	V_{DD} = 5V V_o = 4.5V				
		at T_{amb}= -40°C	-0.145			mA
		at T_{amb}= 25°C	-0.12		-0.5	mA
		at T_{amb}= 85°C	-0.095			mA
		V_{DD}=10V V_o = 9.5V				
		at T_{amb}= -40°C	-0.6			mA
		at T_{amb}= 25°C	-0.5		-1.5	mA
		at T_{amb}= 85°C	-0.4			mA
I_I	Input current	T_{amb}= 25°C		10		pA



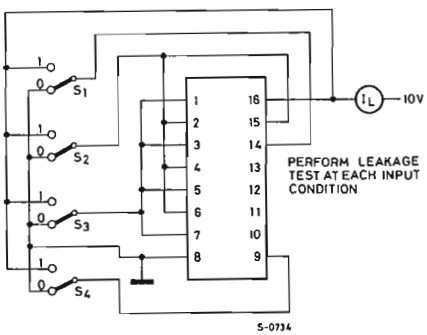
Typical power dissipation characteristics

STATIC ELECTRICAL CHARACTERISTICS (continued)

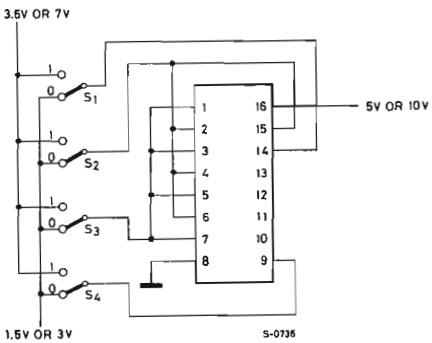
Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_L	Quiescent current	V_{DD} = 10V				
		at T_{amb}= -40°C			100	μA
		at T_{amb}= 25°C		0.2	100	μA
		at T_{amb}= 85°C			1400	μA
V_{OH}	Output high voltage	I_o = 0				
		V_{DD}=5V				
		at T_{amb}= -40°C	4.99			V
		at T_{amb}= 25°C	4.99	5		V
		at T_{amb}= 85°C	4.95			V
		V_{DD}= 10V				
		at T_{amb}= -40°C	9.99			V
		at T_{amb}= 25°C	9.99	10		V
		at T_{amb}= 85°C	9.95			V
V_{OL}	Output low voltage	I_o = 0				
		V_{DD} = 5V or 10V				
		at T_{amb}= -40°C			0.01	V
		at T_{amb}= 25°C		0	0.01	V
		at T_{amb}= 85°C			0.05	V
V_{NH}	Noise immunity	V_{DD} = 5V V_o = 3.6V				
		at T_{amb}= -40°C	1.4			V
		at T_{amb}= 25°C	1.5	2.25		V
		at T_{amb}= 85°C	1.5			V
		V_{DD}=10V V_o = 7.2V				
		at T_{amb}= -40°C	2.9			V
		at T_{amb}= 25°C	3	4.5		V
		at T_{amb}= 85°C	3			V
V_{NL}	Noise immunity	V_{DD}= 5V V_o = 0.95V				
		at T_{amb}= -40°C	1.5			V
		at T_{amb}= 25°C	1.5	2.25		V
		at T_{amb}= 85°C	1.4			V

TEST CIRCUITS

Quiescent device current



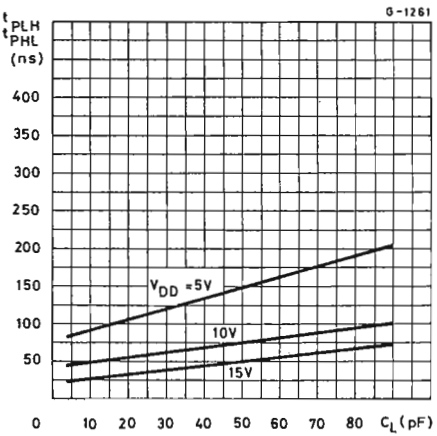
Noise immunity



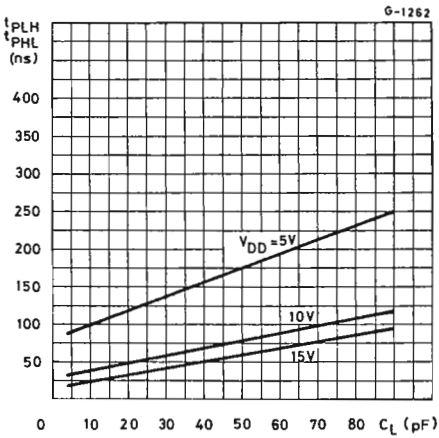
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}=25°C, C_L=15 pF, typical temperature coefficient for all V_{DD} = 0.3%/°C values)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
t_{PLH}, t_{PHL}	Propagation delay time	V_{DD}= 5V				
		for **HBC** types		100	225	ns
		for **HBF** types		100	300	ns
		V_{DD}=10V				
		for **HBC** types		50	100	ns
		for **HBF** types		50	125	ns
t_{TLH}, t_{THL}	Transition time	V_{DD} = 5V				
		for **HBC** types		100	200	ns
		for **HBF** types		100	275	ns
		V_{DD} = 10V				
		for **HBC** types		40	65	ns
		for **HBF** types		40	80	ns
C_i	Input capacitance	A and B inputs				
		for **HBC** and **HBF** types		5		pF
		K_a and K_b inputs				
		for **HBC** and **HBF** types		12		pF

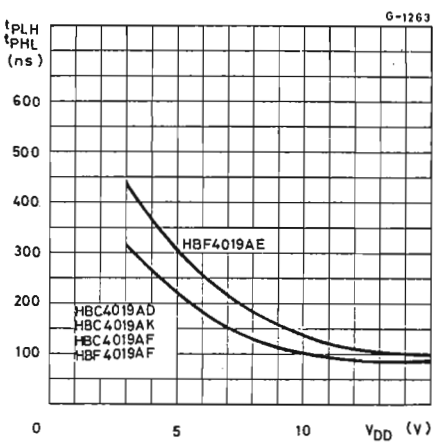
Typical propagation delay time vs. C_L



Typical transition time vs. C_L

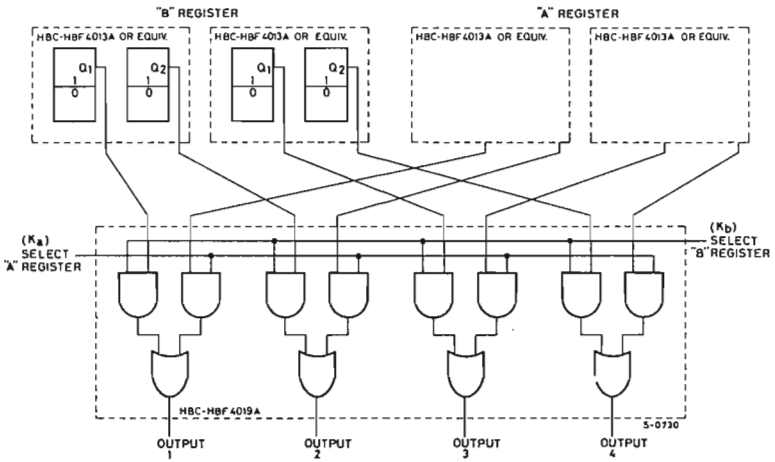


Maximum propagation delay time vs. V_{DD}

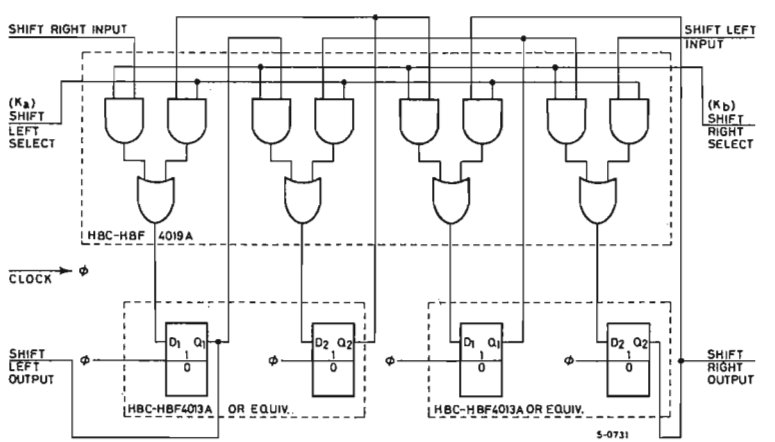


TYPICAL APPLICATIONS

AND–OR selected gating

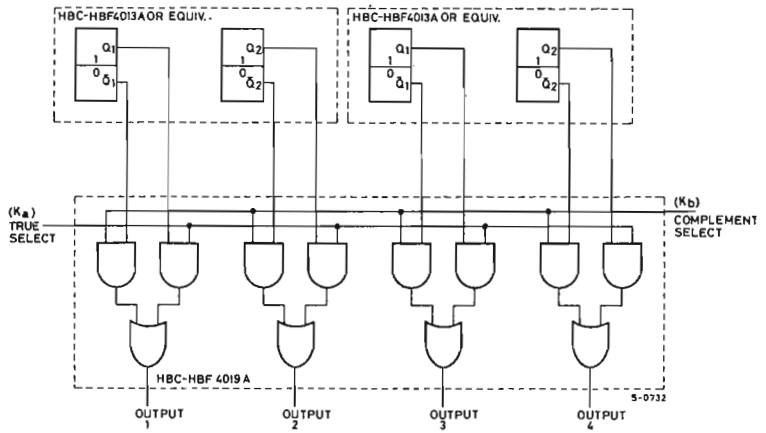


Shift left shift right register

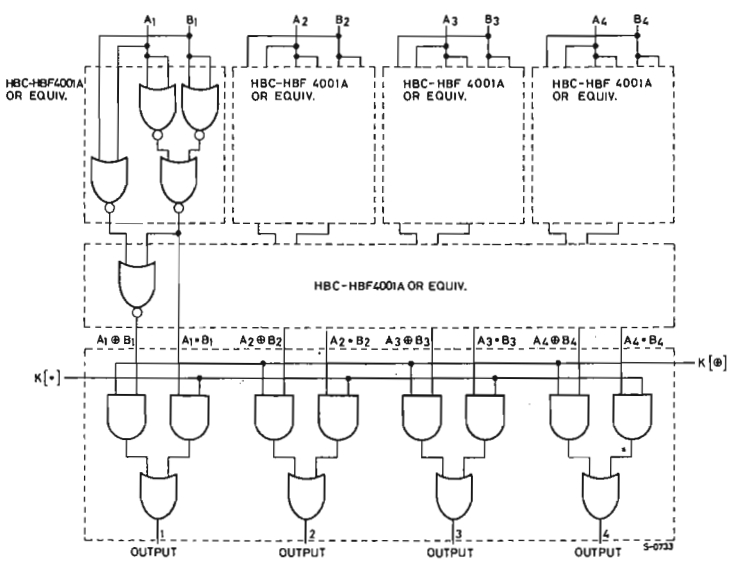


TYPICAL APPLICATIONS (continued)

True complement selector



AND-OR exclusive - OR selector



COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

14-STAGE RIPPLE-CARRY BINARY COUNTER/DIVIDER

- LOW QUIESCENT POWER DISSIPATION
- WIDE SUPPLY VOLTAGE RANGE: 3 to 15V
- HIGH NOISE IMMUNITY: 45% of V_{DD} (TYP.)
- MEDIUM SPEED OPERATION
- INPUTS FULLY PROTECTED
- LOW OUTPUT IMPEDANCE: 1000 Ω (TYP.) at V_{DD}-V_{SS} = 10V
- HIGH FANOUT

The **HBC 4020A** (extended temperature range) and **HBF 4020A** (standard temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package.
They consist of a 14 ripple-carry stage binary counter. Buffered outputs are externally available from stages 1, and 4 through 14. The counter is reset to its "all zeros" state by a high level on the reset input line.
Each counter stage is a static master-slave flip-flop. The counter is advanced one count on the negative-going transition of each input pulse.

ABSOLUTE MAXIMUM RATINGS

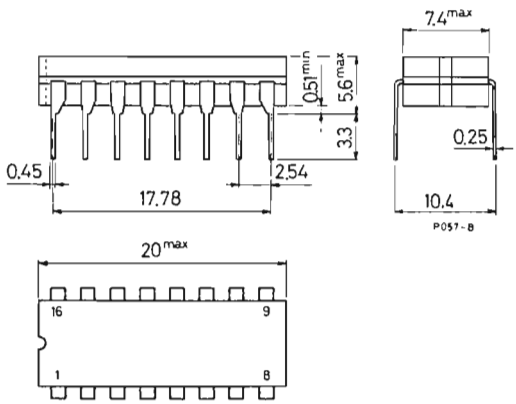
V_{DD}-V_{SS}	Supply voltage	-0.5 to 15 V
V_i	Input voltage (at any pin)	$V_{SS} \leqslant V_i \leqslant V_{DD}$
P_{tot}	Total power dissipation (per package)	200 mW
T_{stg}	Storage temperature	-65 to 150 °C
T_{op}	Operating temperature: for **HBC** types	-55 to 125 °C
	for **HBF** types	-40 to 85 °C

ORDERING NUMBERS:

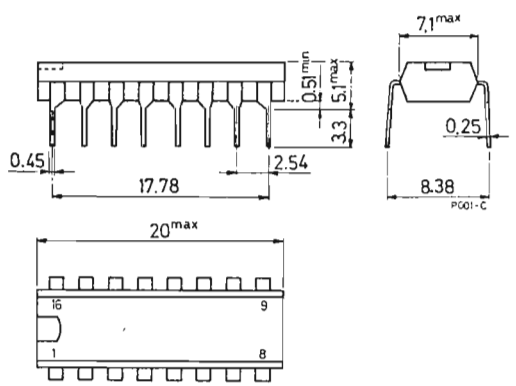
HBC 4020 AD for dual in-line ceramic package
HBC 4020 AF for dual in-line ceramic package frit seal (extended temperature range)
HBC 4020 AK for ceramic flat package
HBF 4020 AE for dual in-line plastic package
HBF 4020 AF for dual in-line ceramic package frit seal (standard temperature range)

MECHANICAL DATA (dimensions in mm)

Dual in-line ceramic package
for HBC 4020 AD and
HBC/HBF 4020 AF

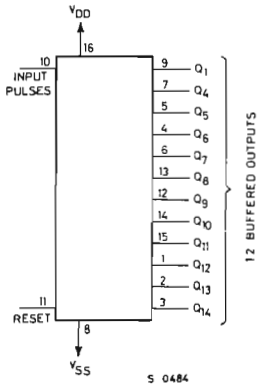


Dual in-line plastic package
for HBF 4020 AE

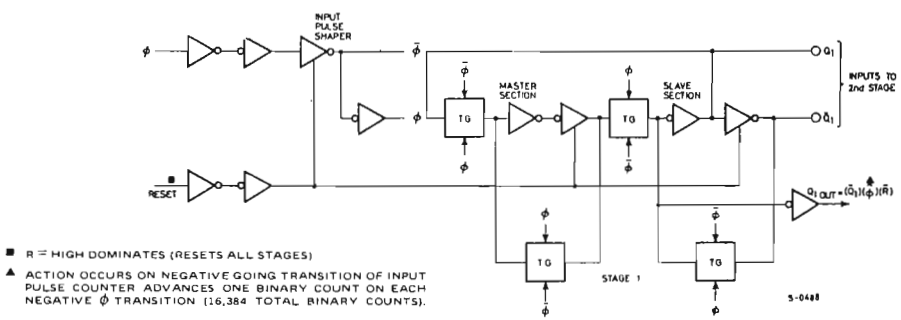


Ceramic flat package for HBC 4020 AK

CONNECTION DIAGRAM



LOGIC DIAGRAM



■ R = HIGH DOMINATES (RESETS ALL STAGES)

▲ ACTION OCCURS ON NEGATIVE GOING TRANSITION OF INPUT PULSE COUNTER ADVANCES ONE BINARY COUNT ON EACH NEGATIVE ϕ TRANSITION (16,384 TOTAL BINARY COUNTS).

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage	3 to 15	V
V_i*	Input voltage	V_{DD} to V_{SS}	
T_{op}	Operating temperature: for **HBC** types	-55 to 125	°C
	for **HBF** types	-40 to 85	°C

* This is measured with respect to the V_{SS} pin voltage

STATIC ELECTRICAL CHARACTERISTICS

Parameter		Test conditions	Min.	Typ.	Max.	Unit
HBC types (extended temperature range)						
I_L	Quiescent current	V_{DD} = 5V				
		at T_{amb} = -55°C			15	µA
		at T_{amb} = 25°C		0.5	15	µA
		at T_{amb} = 125°C			900	µA
		V_{DD} = 10V				
		at T_{amb} = -55°C			25	µA
		at T_{amb} = 25°C		1	25	µA
		at T_{amb} = 125°C			1500	µA
V_{OH}	Output high voltage	I_o = 0				
		V_{DD} = 5V				
		at T_{amb} = -55°C	4.99			V
		at T_{amb} = 25°C	4.99	5		V
		at T_{amb} = 125°C	4.95			V
		V_{DD} = 10V				
		at T_{amb} = -55°C	9.99			V
		at T_{amb} = 25°C	9.99	10		V
		at T_{amb} = 125°C	9.95			V
V_{OL}	Output low voltage	I_o = 0				
		V_{DD} = 5V or 10V				
		at T_{amb} = -55°C			0.01	V
		at T_{amb} = 25°C		0	0.01	V
		at T_{amb} = 125°C			0.05	V
→ V_{NH}	Noise immunity	V_{DD} = 5V V_o = 4.2V				
		at T_{amb} = -55°C	1.4			V
		at T_{amb} = 25°C	1.5	2.25		V
		at T_{amb} = 125°C	1.5			V
		V_{DD} = 10V V_o = 9V				
		at T_{amb} = -55°C	2.9			V
		at T_{amb} = 25°C	3	4.5		V
		at T_{amb} = 125°C	3			V

STATIC ELECTRICAL CHARACTERISTICS (continued)

	Parameter		Test conditions	Min.	Typ.	Max.	Unit
→	V_{NL}	Noise immunity	V_{DD} = 5V V_o = 0.8V				
			at T_{amb} = -55°C	1.5			V
			at T_{amb} = 25°C	1.5		2.25	V
			at T_{amb} = 125°C	1.4			V
			V_{DD} = 10V V_o = 1V				
			at T_{amb} = -55°C	3			V
			at T_{amb} = 25°C	3		4.5	V
			at T_{amb} = 125°C	2.9			V
→	I_DN	Output drive current N-channel	V_{DD} = 5V V_o = 0.5V				
			at T_{amb} = -55°C	0.09			mA
			at T_{amb} = 25°C	0.075		0.2	mA
			at T_{amb} = 125°C	0.05			mA
			V_{DD} = 10V V_o = 0.5V				
			at T_{amb} = -55°C	0.185			mA
			at T_{amb} = 25°C	0.15		0.4	mA
			at T_{amb} = 125°C	0.105			mA
	I_DP	Output drive current P-channel	V_{DD} = 5V V_o ≡ 4.5V				
			at T_{amb} = -55°C	-0.11			mA
			at T_{amb} = 25°C	-0.09		-0.25	mA
			at T_{amb} = 125°C	-0.065			mA
			V_{DD} = 10V V_o = 9.5V				
			at T_{amb} = -55°C	-0.25			mA
			at T_{amb} = 25°C	-0.20		-0.5	mA
			at T_{amb} = 125°C	-0.14			mA
	I_i	Input current	T_{amb} = 25°C		10		pA

HBF types (standard temperature range)

I_L	Quiescent current	V_{DD} = 5V			
		at T_{amb} = -40°C		50	µA
		at T_{amb} = 25°C	1	50	µA
		at T_{amb} = 85°C		700	µA

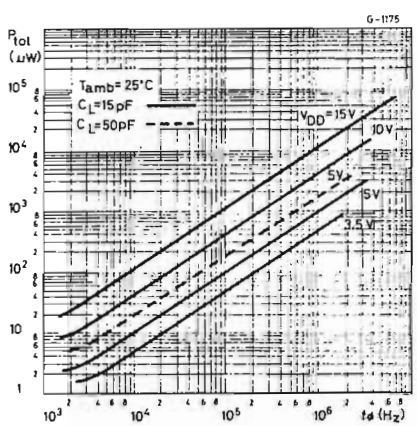
STATIC ELECTRICAL CHARACTERISTICS (continued)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_L	Quiescent current	V_{DD} = 10V				
		at T_{amb}= -40°C			100	μA
		at T_{amb}= 25°C		2	100	μA
		at T_{amb}= 85°C			1400	μA
V_{OH}	Output high voltage	I_o = 0				
		V_{DD} = 5V				
		at T_{amb}= -40°C	4.99			V
		at T_{amb}= 25°C	4.99	5		V
		at T_{amb}= 85°C	4.95			V
		V_{DD} = 10V				
		at T_{amb}= -40°C	9.99			V
		at T_{amb}= 25°C	9.99	10		V
		at T_{amb}= 85°C	9.95			V
V_{OL}	Output low voltage	I_o = 0				
		V_{DD}= 5V or 10V				
		at T_{amb}= -40°C			0.01	V
		at T_{amb}= 25°C		0	0.01	V
		at T_{amb}= 85°C			0.05	V
→ V_{NH}	Noise immunity	V_{DD} = 5V V_o = 4.2V				
		at T_{amb}= -40°C	1.4			V
		at T_{amb}= 25°C	1.5	2.25		V
		at T_{amb}= 85°C	1.5			V
		V_{DD}= 10V V_o = 9V				
		at T_{amb}= -40°C	2.9			V
		at T_{amb}= 25°C	3	4.5		V
		at T_{amb}= 85°C	3			V
→ V_{NL}	Noise immunity	V_{DD}= 5V V_o = 0.8V				
		at T_{amb}= -40°C	1.5			V
		at T_{amb}= 25°C	1.5	2.25		V
		at T_{amb}= 85°C	1.4			V

STATIC ELECTRICAL CHARACTERISTICS (continued)

	Parameter		Test conditions	Min.	Typ.	Max.	Unit
→	V_{NL}	Noise immunity	V_{DD} = 10V V_o = 1V				
			at T_{amb} = -40°C	3			V
			at T_{amb} = 25°C	3		4.5	V
			at T_{amb} = 85°C	2.9			V
→	I_DN	Output drive current N-channel	V_{DD} = 5V V_o = 0.5V				
			at T_{amb} = -40°C	0.09			mA
			at T_{amb} = 25°C	0.08		0.33	mA
			at T_{amb} = 85°C	0.065			mA
			V_{DD} = 10V V_o = 0.5V				
			at T_{amb} = -40°C	0.16			mA
			at T_{amb} = 25°C	0.13		0.5	mA
			at T_{amb} = 85°C	0.1			mA
	I_DP	Output drive current P-channel	V_{DD} = 5V V_o = 4.5V				
			at T_{amb} = -40°C	-0.09			mA
			at T_{amb} = 25°C	-0.06		-0.25	mA
			at T_{amb} = 85°C	-0.05			mA
			V_{DD} = 10V V_o = 9.5V				
			at T_{amb} = -40°C	-0.18			mA
			at T_{amb} = 25°C	-0.15		-0.5	mA
			at T_{amb} = 85°C	-0.12			mA
	I_i	Input current	T_{amb} = 25°C		10		pA

Typical power dissipation characteristics



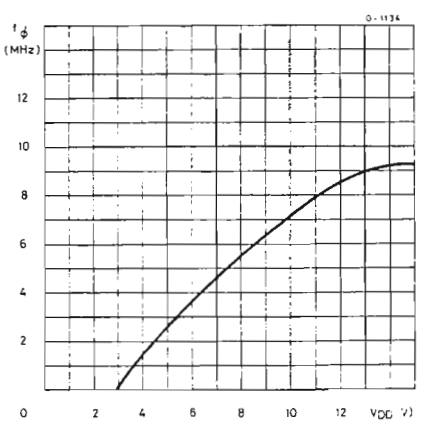
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 15 pF, typical temperature coefficient for all V_{DD} = 0.3%/°C values, all input rise and fall time = 20 ns, except $t_{\phi r}$ and $t_{\phi f}$)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
CLOCKED OPERATION					
t_{PLH}, t_{PHL} Propagation delay time	V_{DD} = 5V				
	for HBC types		450	600	ns
	for HBF types		450	650	ns
	V_{DD} = 10V				
	for HBC types		150	225	ns
	for HBF types		150	250	ns
t_{TLH}, t_{THL} Transition time	V_{DD} = 5V				
	for HBC types		450	600	ns
	for HBF types		450	650	ns
	V_{DD} = 10V				
	for HBC types		200	300	ns
	for HBF types		200	350	ns
t_{pwH}, t_{pwL} Minimum clock pulse width	V_{DD} = 5V				
	for HBC types		200	335	ns
	for HBF types		200	500	ns
	V_{DD} = 10V				
	for HBC types		70	125	ns
	for HBF types		70	165	ns
$t_{\phi r}$, $t_{\phi f}$ Clock rise and fall time	V_{DD} = 5V or 10V for HBC and HBF types			15	μs
f_{max} Maximum clock frequency	V_{DD} = 5V				
	for HBC types	1.5	2.5		MHz
	for HBF types	1	2.5		MHz
	V_{DD} = 10V				
	for HBC types	4	7		MHz
	for HBF types	3	7		MHz
C_i Input capacitance	Any input for HBC and HBF types			5	pF

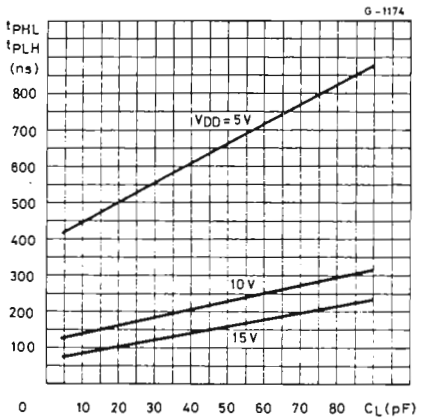
DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
RESET OPERATION						
t_{PHL}	Propagation delay time	V_{DD} = 5V				
		for HBC types		2000	3000	ns
		for HBF types		2000	3500	ns
		V_{DD} = 10V				
		for HBC types		500	775	ns
		for HBF types		500	900	ns
t_{pwH}	Minimum reset pulse width	V_{DD} = 5V				
		for HBC types		1800	2500	ns
		for HBF types		1800	3000	ns
		V_{DD} = 10V				
		for HBC types		300	475	ns
		for HBF types		300	550	ns

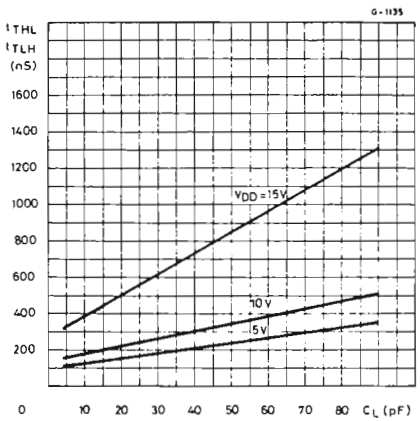
Typical clock frequency vs. V_{DD}



Typical propagation delay time vs. C_L



Typical transition time vs. C_L



COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

8-STAGE STATIC SHIFT REGISTER ASYNCHRONOUS PARALLEL INPUT/ SERIAL OUTPUT SYNCHRONOUS SERIAL INPUT/SERIAL OUTPUT

- LOW QUIESCENT POWER DISSIPATION
- WIDE SUPPLY VOLTAGE RANGE: 3 to 15V
- HIGH NOISE IMMUNITY: 45% of V_{DD} (TYP.)
- INPUTS FULLY PROTECTED
- HIGH FANOUT
- ASYNCHRONOUS PARALLEL or SYNCHRONOUS SERIAL OPERATION UNDER CONTROL of PARALLEL/SERIAL CONTROL INPUT
- INDIVIDUAL "JAM" INPUTS TO EACK REGISTER STAGE
- MASTER SLAVE FLIP-FLOP REGISTER STAGE
- FULLY STATIC OPERATION . . . . . DC to 5 MHz

The **HBC 4021A** (extended temperature range) and **HBF 4021A** (standard temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package. The **HBC/HBF 4021A** types are 8-stage parallel or serial-input/serial-output shift registers having common Clock and Parallel/Serial Control inputs, a single Serial Data input, and individual parallel "Jam" inputs to each register stage. Each register stage is a D-type, master-slave flip-flop. "Q" outputs are available from the sixth, seventh, and eighth stages. When the Parallel/Serial Control inputs is "low", data is serially shifted into the 8-stage register synchronously with the positive-going transition of the Clock pulse. When the Parallel/Serial Control input is "high", data is jammed into the 8-stage register via the parallel input lines asynchronously with the clock line.
Register expansion is possible using additional **HBC/HBF 4021A** package.

ABSOLUTE MAXIMUM RATINGS

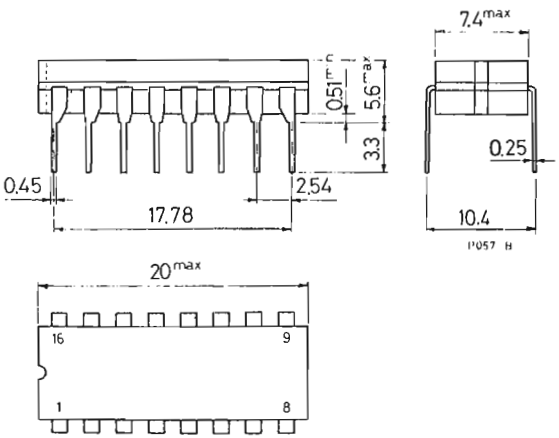
$V_{DD}-V_{SS}$	Supply voltage	-0.5 to 15	V
V_i	Input voltage (at any pin)	$V_{SS} \leqslant V_i \leqslant V_{DD}$	
P_{tot}	Total power dissipation (per package)	200	mW
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature: for **HBC** types	-55 to 125	°C
	for **HBF** types	-40 to 85	°C

ORDERING NUMBERS:

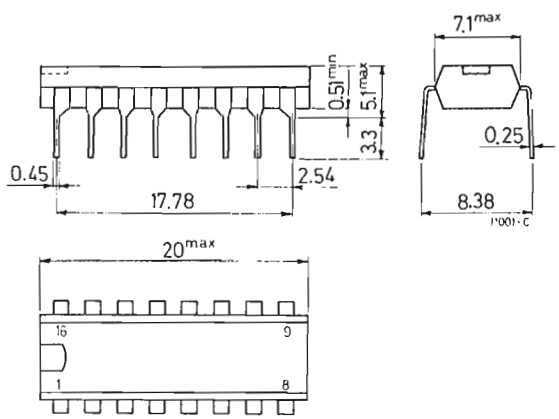
HBC 4021 AD for dual in-line ceramic package
HBC 4021 AF for dual in-line ceramic package, frit seal (extended temperature range)
HBC 4021 AK for ceramic flat package
HBF 4021 AE for dual in-line plastic package
HBF 4021 AF for dual in-line ceramic package, frit seal (standard temperature range)

MECHANICAL DATA (dimensions in mm)

Dual in-line ceramic package
for HBC 4021 AD and
HBC/HBF 4021 AF

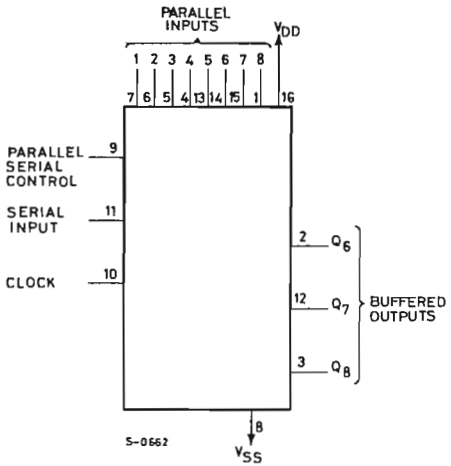


Dual in-line plastic package
for HBF 4021 AE

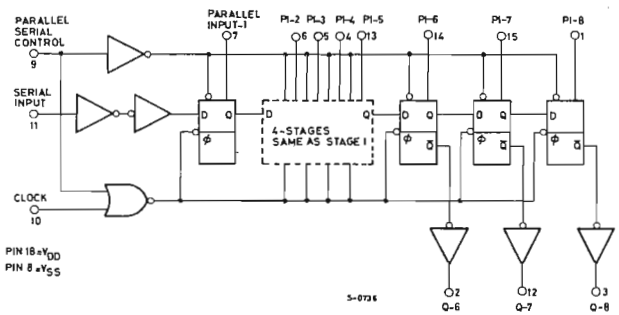


Ceramic flat package for HBC 4021 AK

CONNECTION DIAGRAM



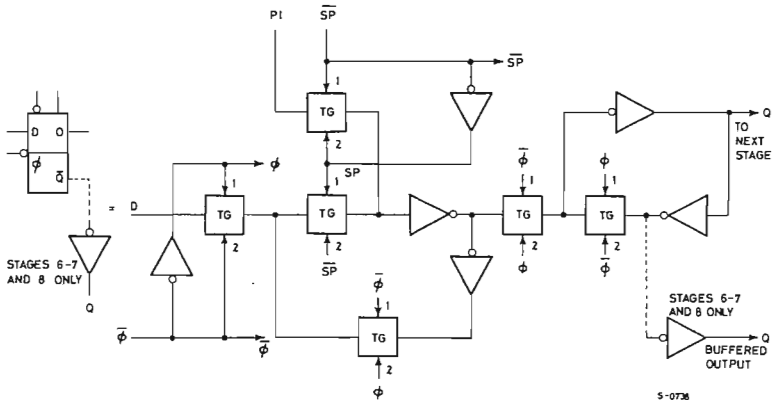
LOGIC DIAGRAM and TRUTH TABLE



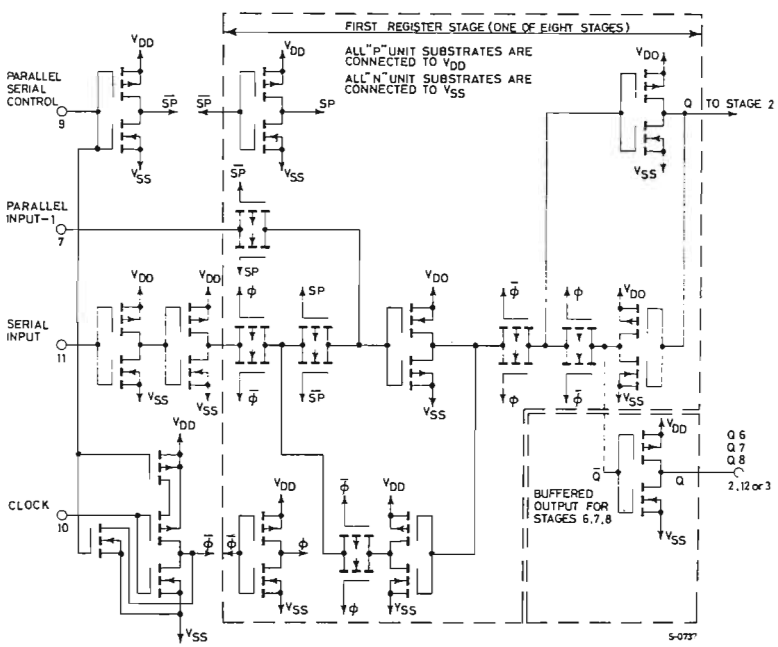
CLOCK ϕ *	Serial Input	Parallel Serial Control	Parallel Input-1	Parallel Input-n	Internal Q_1	Q_n
X	X	1	0	0	0	0
X	X	1	0	1	0	1
X	X	1	1	0	1	0
X	X	1	1	1	1	1
⌐	0	0	X	X	0	Q_{n-1}
⌐	1	0	X	X	1	Q_{n-1}
¬	X	0	X	X	Q_1	Q_n ← No change

* = Level change
X = Don't care case

ONE TYPICAL STAGE AND ITS EQUIVALENT DETAILED CIRCUIT



SCHEMATIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage	3 to 15	V
V_I*	Input voltage	V_{DD} to V_{SS}	
T_{op}	Operating temperature: for **HBC** types	-55 to 125	°C
	for **HBF** types	-40 to 85	°C

*This is measured with respect to the V_{SS} pin voltage

STATIC ELECTRICAL CHARACTERISTICS

Parameter	Test conditions	Min.	Typ.	Max.	Unit
HBC types (extended temperature range)					
I_L Quiescent current	V_{DD} = 5V				
	at T_{amb} = -55°C			5	μA
	at T_{amb} = 25°C		0.5	5	μA
	at T_{amb} = 125°C			300	μA
	V_{DD} = 10V				
	at T_{amb} = -55°C			10	μA
	at T_{amb} = 25°C		1	10	μA
	at T_{amb} = 125°C			600	μA
V_{OH} Output high voltage	I_o = 0				
	V_{DD} = 5V				
	at T_{amb} = -55°C	4.99			V
	at T_{amb} = 25°C	4.99	5		V
	at T_{amb} = 125°C	4.95			V
	I_o = 0				
	V_{DD}=10V				
	at T_{amb} = -55°C	9.99			V
	at T_{amb} = 25°C	9.99	10		V
	at T_{amb} = 125°C	9.95			V
V_{OL} Output low voltage	I_o = 0				
	V_{DD}= 5V or 10V				
	at T_{amb} = -55°C			0.01	V
	at T_{amb} = 25°C		0	0.01	V
	at T_{amb} = 125°C			0.05	V
V_{NH} Noise immunity	V_{DD}= 5V V_o = 4.2V				
	at T_{amb} = -55°C	1.4			V
	at T_{amb} = 25°C	1.5	2.25		V
	at T_{amb} = 125°C	1.5			V

STATIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{NH}	Noise immunity	V_{DD}=10V V_o = 9V				
		at T_{amb}= -55°C	2.9			V
		at T_{amb}= 25°C	3		4.5	V
		at T_{amb}= 125°C	3			V
V_{NL}	Noise immunity	V_{DD} = 5V V_o = 0.8V				
		at T_{amb}= -55°C	1.5			V
		at T_{amb}= 25°C	1.5		2.25	V
		at T_{amb}= 125°C	1.4			V
		V_{DD}=10V V_o = 1V				
		at T_{amb}= -55°C	3			V
		at T_{amb}= 25°C	3		4.5	V
		at T_{amb}= 125°C	2.9			V
I_DN	Output drive current N-channel	V_{DD}= 5V V_o = 0.5V				
		at T_{amb}= -55°C	0.15			mA
		at T_{amb}= 25°C	0.12		0.3	mA
		at T_{amb}= 125°C	0.085			mA
		V_{DD}=10V V_o = 0.5V				
		at T_{amb}= -55°C	0.31			mA
		at T_{amb}= 25°C	0.25		0.5	mA
		at T_{amb}= 125°C	0.175			mA
I_DP	Output drive current P-channel	V_{DD}= 5V V_o = 4.5V				
		at T_{amb}= -55°C	-0.1			mA
		at T_{amb}= 25°C	-0.08		-0.16	mA
		at T_{amb}= 125°C	-0.055			mA
		V_{DD}=10V V_o = 9.5V				
		at T_{amb}= -55°C	-0.25			mA
		at T_{amb}= 25°C	-0.20		-0.44	mA
		at T_{amb}= 125°C	-0.14			mA
I_I	Input current	T_{amb} = 25°C		10		pA

HBF types (standard temperature range)

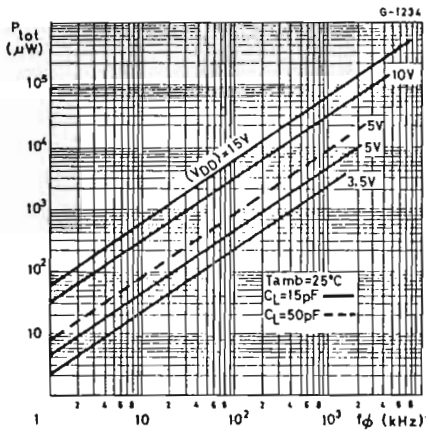
I_L	Quiescent current	V_{DD} = 5V				
		at T_{amb}= -40°C			50	μA
		at T_{amb}= 25°C		0.5	50	μA
		at T_{amb}= 85°C			700	μA

STATIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_L	Quiescent current	V_{DD}= 10V				
		at T_{amb}= -40°C			100	μA
		at T_{amb}= 25°C		1	100	μA
		at T_{amb}= 85°C			1400	μA
V_{OH}	Output high voltage	I_o = 0				
		V_{DD} = 5V				
		at T_{amb}= -40°C	4.99			V
		at T_{amb}= 25°C	4.99	5		V
		at T_{amb}= 85°C	4.95			V
		I_o = 0				
		V_{DD}=10V				
		at T_{amb}= -40°C	9.99			V
		at T_{amb}= 25°C	9.99	10		V
		at T_{amb}= 85°C	9.95			V
V_{OL}	Output low voltage	I_o = 0				
		V_{DD}= 5V or 10V				
		at T_{amb}= -40°C			0.01	V
		at T_{amb}= 25°C		0	0.01	V
		at T_{amb}= 85°C			0.05	V
V_{NH}	Noise immunity	V_{DD} = 5V V_o = 4.2V				
		at T_{amb}= -40°C	1.4			V
		at T_{amb}= 25°C	1.5	2.25		V
		at T_{amb}= 85°C	1.5			V
		V_{DD}=10V V_o= 9V				
		at T_{amb}= -40°C	2.9			V
		at T_{amb}= 25°C	3	4.5		V
		at T_{amb}= 85°C	3			V
V_{NL}	Noise immunity	V_{DD} = 5V V_o = 0.8V				
		at T_{amb}= -40°C	1.5			V
		at T_{amb}= 25°C	1.5	2.25		V
		at T_{amb}= 85°C	1.4			V
		V_{DD}=10V V_o = 1V				
		at T_{amb}= -40°C	3			V
		at T_{amb}= 25°C	3	4.5		V
		at T_{amb}= 85°C	2.9			V

STATIC ELECTRICAL CHARACTERISTICS (continued)

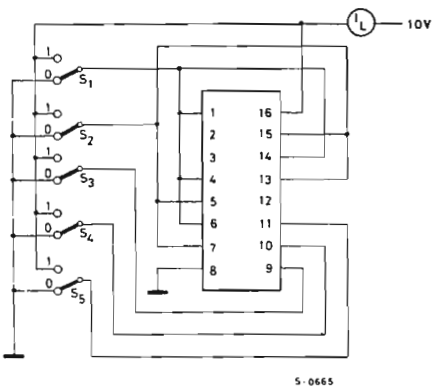
Parameter		Test conditions		Min.	Typ.	Max.	Unit
I_DN	Output drive current N-channel	V_{DD}= 5V	V_o = 0.5V				
			at T_{amb}= -40°C	0.072			mA
			at T_{amb}= 25°C	0.06		0.3	mA
			at T_{amb}= 85°C	0.05			mA
		V_{DD}=10V	V_o = 0.5V				
			at T_{amb}= -40°C	0.12			mA
			at T_{amb}= 25°C	0.1		0.5	mA
			at T_{amb}= 85°C	0.08			mA
I_DP	Output drive current P-channel	V_{DD}= 5V	V_o = 4.5V				
			at T_{amb}= -40°C	-0.06			mA
			at T_{amb}= 25°C	-0.05		-0.16	mA
			at T_{amb}= 85°C	-0.04			mA
		V_{DD}=10V	V_o = 9.5V				
			at T_{amb}= -40°C	-0.12			mA
			at T_{amb}= 25°C	-0.1		-0.44	mA
			at T_{amb}= 85°C	-0.08			mA
I_I	Input current	T_{amb} = 25°C			10		pA



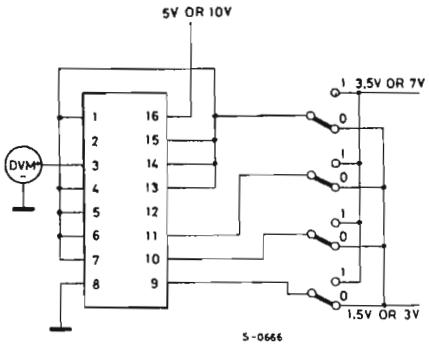
Typical power dissipation characteristics

TEST CIRCUITS

Quiescent device current



Noise immunity



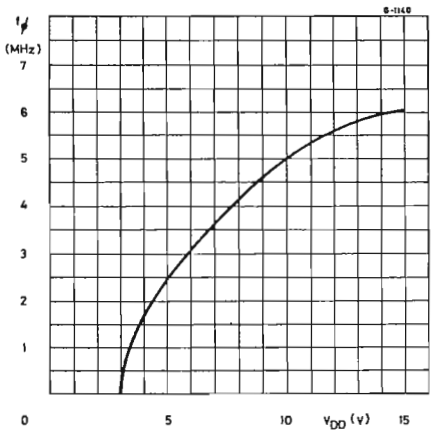
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, C_L= 15 pF, typical temperature coefficient for all V_{DD}= 0.3%/°C values, all input rise and fall time = 20 ns, except $t_{\phi r}$ and $t_{\phi f}$)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{PLH}, t_{PHL} Propagation delay time	V_{DD} = 5V				
	for **HBC** types		300	750	ns
	for **HBF** types		300	1000	ns
	V_{DD} = 10V				
	for **HBC** types		100	225	ns
	for **HBF** types		100	300	ns
t_{TLH}, t_{THL} Transition time	V_{DD} = 5V				
	for **HBC** types		150	300	ns
	for **HBC** types		150	400	ns
	V_{DD} = 10V				
	for **HBC** types		75	125	ns
	for **HBF** types		75	150	ns

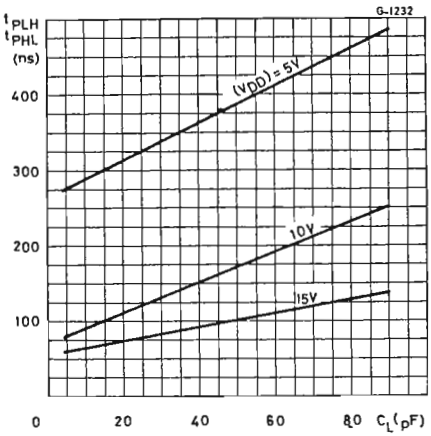
DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
t_{pwH}, t_{pwL}	Minimum clock pulse width	V_{DD} = 5V				
		for **HBC** types		200	500	ns
		for **HBF** types		200	830	ns
		V_{DD} = 10V				
		for **HBC** types		100	175	ns
		for **HBF** types		100	200	ns
t_{pwH}	Minimum high-level Parallel/Serial Control pulse width	V_{DD} = 5V				
		for **HBC** types		200	500	ns
		for **HBF** types		200	830	ns
		V_{DD}= 10V				
		for **HBC** types		100	175	ns
		for **HBF** types		100	200	ns
$t_{\phi r}$, $t_{\phi f}$	Clock rise and fall time	V_{DD} = 5V or 10V for **HBC** and **HBF** types			15	μs
t_s	Set-up time	V_{DD} = 5V				
		for **HBC** types		100	350	ns
		for **HBF** types		100	500	ns
		V_{DD}= 10V				
		for **HBC** types		50	80	ns
		for **HBF** types		50	100	ns
f_{max}	Maximum clock frequency	V_{DD} = 5V				
		for **HBC** types	1	2.5		MHz
		for **HBF** types	0.6	2.5		MHz
		V_{DD}= 10V				
		for **HBC** types	3	5		MHz
		for **HBF** types	2.5	5		MHz
C_i	Input capacitance	Any input for **HBC** and **HBF** types		5		pF

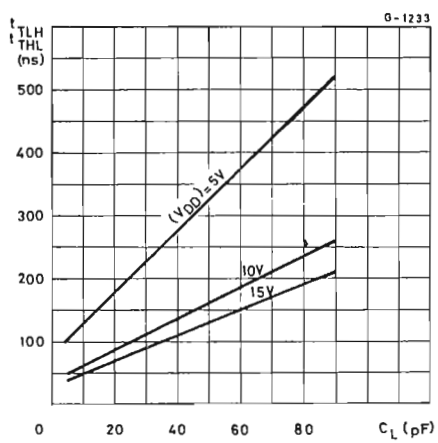
Typical clock frequency vs. V_{DD}



Typical propagation delay time vs. C_L



Typical transition time vs. C_L



COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

7-STAGE BINARY COUNTER WITH BUFFERED RESET

- LOW QUIESCENT POWER DISSIPATION
- WIDE SUPPLY VOLTAGE RANGE: 3 to 15V
- HIGH NOISE IMMUNITY: 45% of V_{DD} (TYP.)
- MEDIUM SPEED OPERATION: 7 MHz (TYP.) INPUT PULSE RATE at V_{DD}-V_{SS} =10V
- INPUTS FULLY PROTECTED
- LOW OUTPUT IMPEDANCE
- HIGH FANOUT
- STATIC COUNTER OPERATION - COUNTER RETAINS STATE INDEFINITELY WITH INPUT PULSE LEVEL "LOW" or "HIGH"
- GATE INPUT LOADING on BOTH RESET and INPUT-PULSE LINES

The **HBC 4024A** (extended temperature range) and **HBF 4024A** (standard temperature range) are monolithic integrated circuits, available in 14-lead dual in-line plastic or ceramic package and ceramic flat package. They consist of an input pulse shaping circuit, reset line driver circuitry, and seven binary counter stages. The counter is reset to "zero" by a high level on the reset input. Each counter stage is a static master-slave flip-flop. The counter state is advanced one count on the negative-going transition of each input pulse.

ABSOLUTE MAXIMUM RATINGS

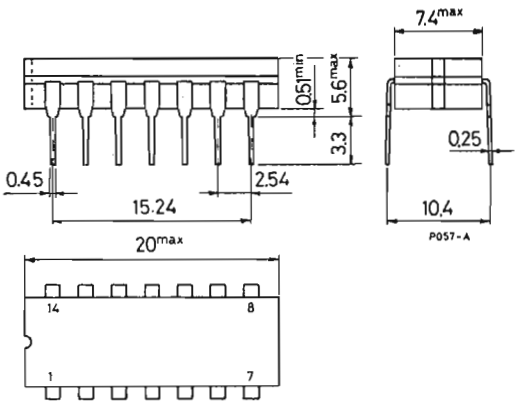
V_{DD}-V_{SS}	Supply voltage	-0.5 to 15	V
V_I	Input voltage (at any pin)	$V_{SS} \leqslant V_i \leqslant V_{DD}$	
P_{tot}	Total power dissipation (per package)	200	mW
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature: for **HBC** types	-55 to 125	°C
	for **HBF** types	-40 to 85	°C

ORDERING NUMBERS:

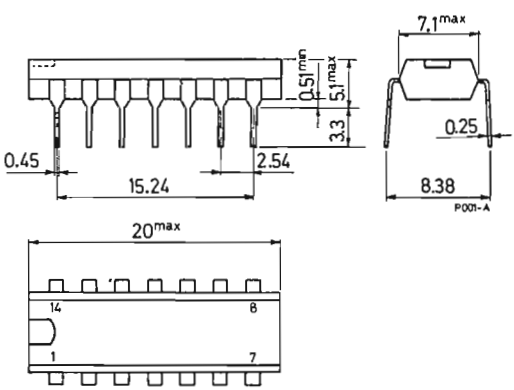
HBC 4024 AD for dual in-line ceramic package
HBC 4024 AF for dual in-line ceramic package, frit seal (extended temperature range)
HBC 4024 AK for ceramic flat package
HBF 4024 AE for dual in-line plastic package
HBF 4024 AF for dual in-line ceramic package, frit seal (standard temperature range)

MECHANICAL DATA (dimensions in mm)

Dual in-line ceramic package
for HBC 4024 AD and
HBC/HBF 4024 AF

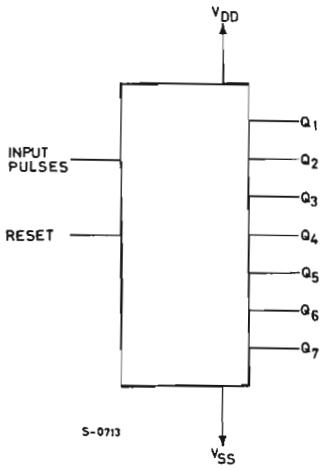


Dual in-line plastic package
for HBF 4024 AE



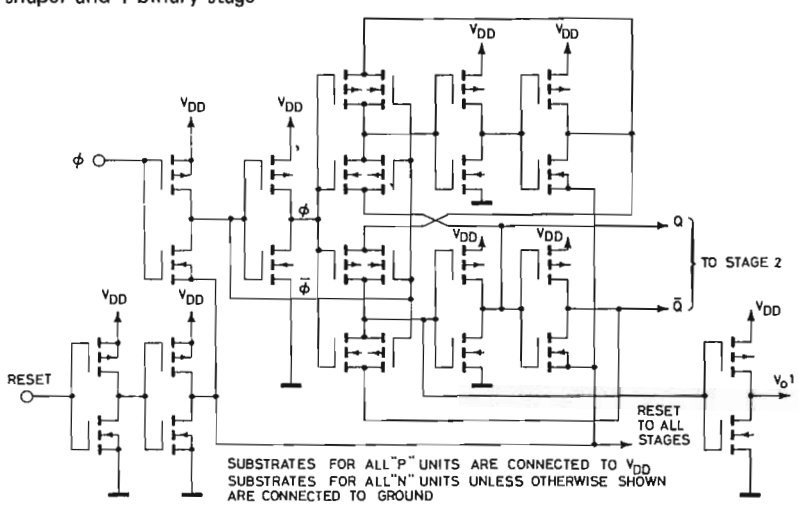
Ceramic flat package for HBC 4024 AK

CONNECTION DIAGRAM



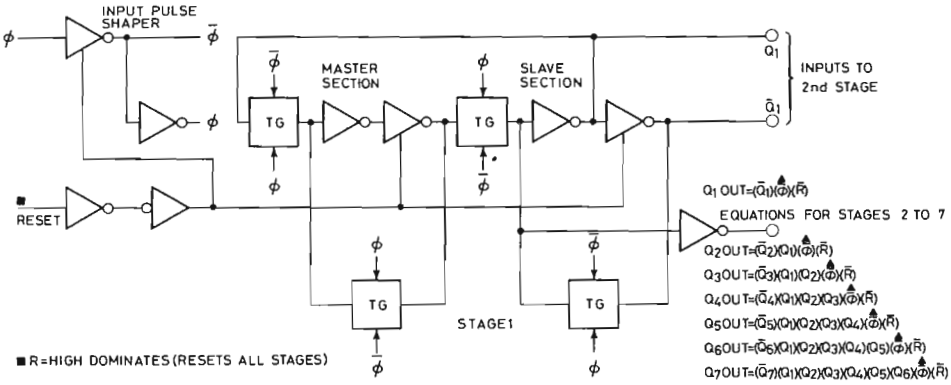
SCHEMATIC DIAGRAM

Pulse shaper and 1 binary stage

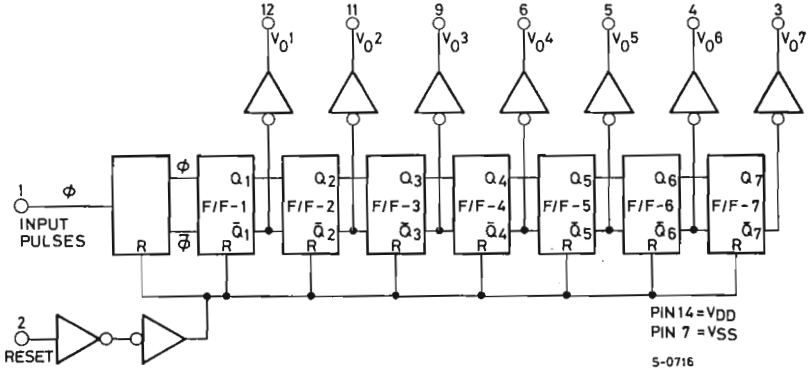


LOGIC BLOCK DIAGRAM

Pulse shaper and 1 binary stage



FUNCTIONAL DIAGRAM



RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage	3 to 15	V
V_i*	Input voltage	V_{DD} to V_{SS}	
T_{op}	Operating temperature: for **HBC** types	-55 to 125	°C
	for **HBF** types	-40 to 85	°C

* This is measured with respect to the V_{SS} pin voltage

STATIC ELECTRICAL CHARACTERISTICS

Parameter		Test conditions	Min.	Typ.	Max.	Unit
HBC types (extended temperature range)						
I_L	Quiescent current	V_{DD} = 5V				
		at T_{amb} = -55°C			5	μA
		at T_{amb} = 25°C		0.3	5	μA
		at T_{amb} = 125°C			300	μA
		V_{DD} = 10V				
		at T_{amb} = -55°C			10	μA
		at T_{amb} = 25°C		0.5	10	μA
		at T_{amb} = 125°C			600	μA
V_{OH}	Output high voltage	I_o = 0				
		V_{DD} = 5V				
		at T_{amb} = -55°C	4.99			V
		at T_{amb} = 25°C	4.99	5		V
		at T_{amb} = 125°C	4.95			V
		V_{DD} = 10V				
		at T_{amb} = -55°C	9.99			V
		at T_{amb} = 25°C	9.99	10		V
		at T_{amb} = 125°C	9.95			V
V_{OL}	Output low voltage	I_o = 0				
		V_{DD} = 5V or 10V				
		at T_{amb} = -55°C			0.01	V
		at T_{amb} = 25°C		0	0.01	V
		at T_{amb} = 125°C			0.05	V
V_{NH}	Noise immunity	V_{DD} = 5V V_o = 4.2V				
		at T_{amb} = -55°C	1.4			V
		at T_{amb} = 25°C	1.5	2.25		V
		at T_{amb} = 125°C	1.5			V
		V_{DD} = 10V V_o = 9V				
		at T_{amb} = -55°C	2.9			V
		at T_{amb} = 25°C	3	4.5		V
		at T_{amb} = 125°C	3			V
V_{NL}	Noise immunity	V_{DD} = 5V V_o = 0.8V				
		at T_{amb} = -55°C	1.5			V
		at T_{amb} = 25°C	1.5	2.25		V
		at T_{amb} = 125°C	1.4			V

STATIC ELECTRICAL CHARACTERISTICS (continued)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{NL}	Noise immunity	$V_{DD} = 10V$ $V_o = 1V$				
		at $T_{amb} = -55°C$	3			V
		at $T_{amb} = 25°C$	3	4.5		V
		at $T_{amb} = 125°C$	2.9			V
I_DN	Output drive current N-channel	$V_{DD} = 5V$ $V_o = 0.5V$				
		at $T_{amb} = -55°C$	0.31			mA
		at $T_{amb} = 25°C$	0.25	0.5		mA
		at $T_{amb} = 125°C$	0.175			mA
		$V_{DD} = 10V$ $V_o = 0.5V$				
		at $T_{amb} = -55°C$	0.62			mA
		at $T_{amb} = 25°C$	0.5	1		mA
		at $T_{amb} = 125°C$	0.35			mA
I_DP	Output drive current P-channel	$V_{DD} = 5V$ $V_o = 4.5V$				
		at $T_{amb} = -55°C$	-0.19			mA
		at $T_{amb} = 25°C$	-0.15	-0.3		mA
		at $T_{amb} = 125°C$	-0.105			mA
		$V_{DD} = 10V$ $V_o = 9.5V$				
		at $T_{amb} = -55°C$	-0.45			mA
		at $T_{amb} = 25°C$	-0.35	-0.7		mA
		at $T_{amb} = 125°C$	-0.25			mA
I_I	Input current	$T_{amb} = 25°C$		10		pA

HBF types (standard temperature range)

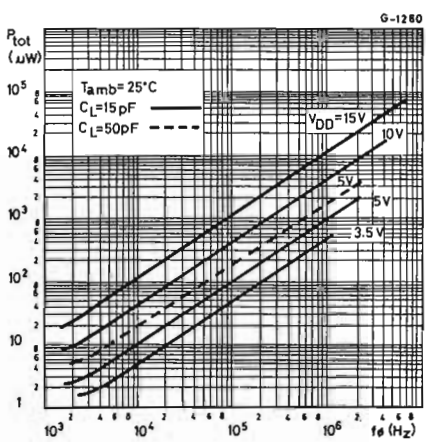
I_L	Quiescent current	$V_{DD} = 5V$				
		at $T_{amb} = -40°C$			50	μA
		at $T_{amb} = 25°C$		0.5	50	μA
		at $T_{amb} = 85°C$			700	μA
		$V_{DD} = 10V$				
		at $T_{amb} = -40°C$			100	μA
		at $T_{amb} = 25°C$		1	100	μA
		at $T_{amb} = 85°C$			1400	μA
V_{OH}	Output high voltage	$I_o = 0$				
		$V_{DD} = 5V$				
		at $T_{amb} = -40°C$	4.99			V
		at $T_{amb} = 25°C$	4.99	5		V
		at $T_{amb} = 85°C$	4.95			V

STATIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{OH}	Output high voltage	V_{DD} = 10V				
		at T_{amb}= -40°C	9.99			V
		at T_{amb}= 25°C	9.99	10		V
		at T_{amb}= 85°C	9.95			V
V_{OL}	Output low voltage	I_o = 0				
		V_{DD} = 5V or 10V				
		at T_{amb}= -40°C			0.01	V
		at T_{amb}= 25°C		0	0.01	V
		at T_{amb}= 85°C			0.05	V
V_{NH}	Noise immunity	V_{DD} = 5V V_o = 4.2V				
		at T_{amb}= -40°C	1.4			V
		at T_{amb}= 25°C	1.5	2.25		V
		at T_{amb}= 85°C	1.5			V
		V_{DD} = 10V V_o = 9V				
		at T_{amb}= -40°C	2.9			V
		at T_{amb}= 25°C	3	4.5		V
		at T_{amb}= 85°C	3			V
V_{NL}	Noise immunity	V_{DD}= 5V V_o = 0.8V				
		at T_{amb}= -40°C	1.5			V
		at T_{amb}= 25°C	1.5	2.25		V
		at T_{amb}= 85°C	1.4			V
		V_{DD} = 10V V_o = 1V				
		at T_{amb}= -40°C	3			V
		at T_{amb}= 25°C	3	4.5		V
		at T_{amb}= 85°C	2.9			V
I_DN	Output drive current N-channel	V_{DD}= 5V V_o = 0.5V				
		at T_{amb}= -40°C	0.15			mA
		at T_{amb}= 25°C	0.12	0.5		mA
		at T_{amb}= 85°C	0.095			mA
		V_{DD} = 10V V_o = 0.5V				
		at T_{amb}= -40°C	0.31			mA
		at T_{amb}= 25°C	0.25	0.7		mA
		at T_{amb}= 85°C	0.2			mA

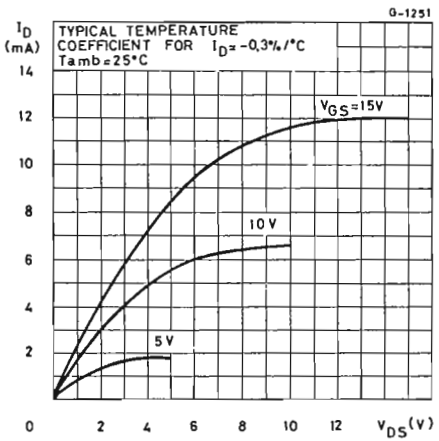
STATIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_DP	Output drive current P-channel	V_{DD} = 5V V_o = 2.5V				
		at T_{amb} = -40°C		-0.145		mA
		at T_{amb} = 25°C		-0.12	-0.3	mA
		at T_{amb} = 85°C		-0.95		mA
		V_{DD} =10V V_o = 9.5V				
		at T_{amb} = -40°C		-0.31		mA
		at T_{amb} = 25°C		-0.25	-0.7	mA
		at T_{amb} = 85°C		-0.2		mA
I_i	Input current	T_{amb} = 25°C		10		pA

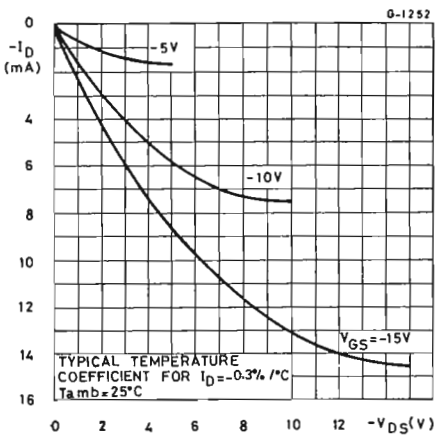


Typical power dissipation characteristics

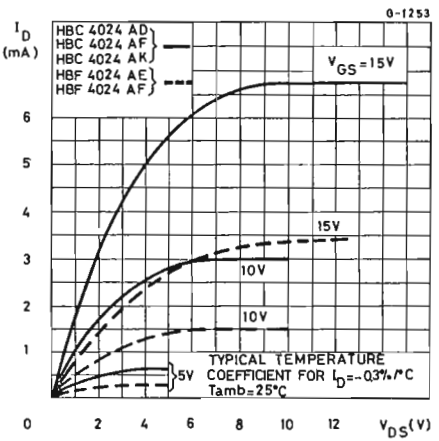
Typical N-channel drain characteristics



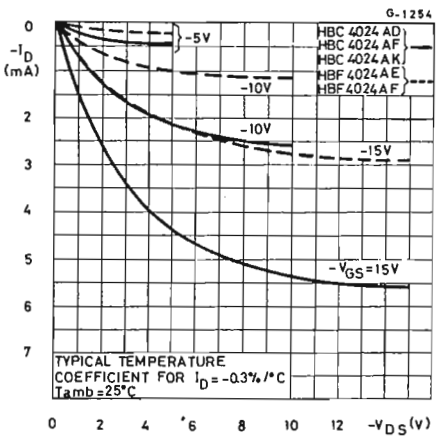
Typical P-channel drain characteristics



Minimum N-channel drain characteristics

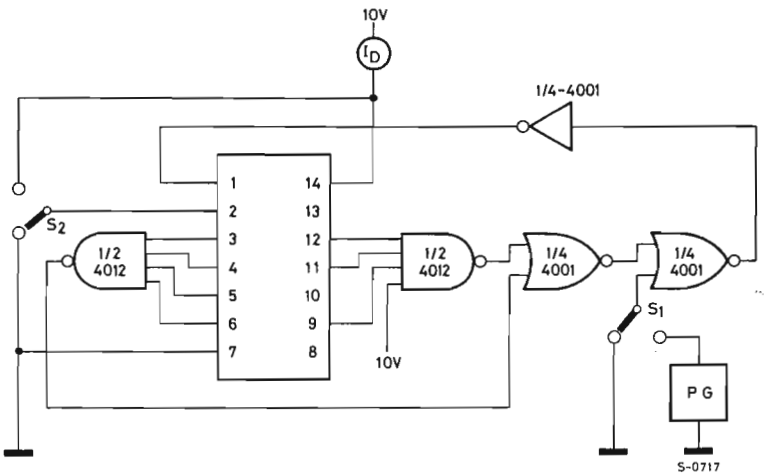


Minimum P-channel drain characteristics

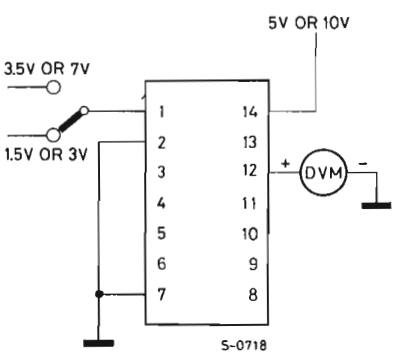


TEST CIRCUITS

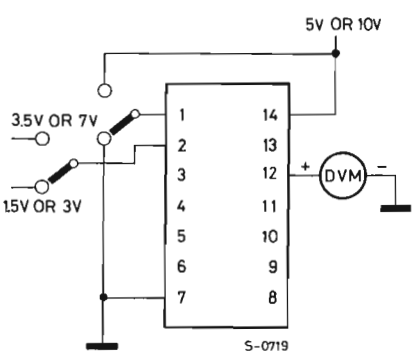
Quiescent device current



Noise immunity



Reset noise immunity

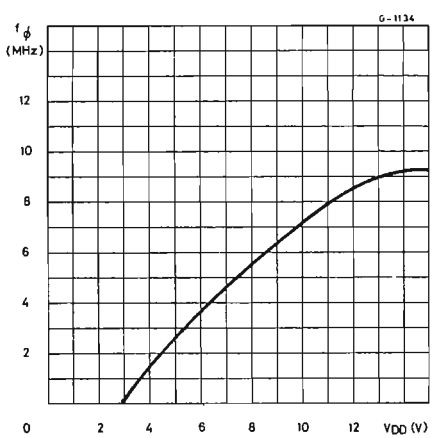


DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}=25°C, C_L=15 pF, typical temperature coefficient for all V_{DD} = 0.3%/°C values, all input rise and fall time = 20 ns, except $t_{\phi r}$ and $t_{\phi f}$)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
INPUT OPERATION						
t_{PLH}, t_{PHL}	Propagation delay time (clock input to Q_1 output)	V_{DD} = 5V				
		for **HBC** types		175	350	ns
		for **HBF** types		175	400	ns
		V_{DD} = 10V				
		for **HBC** types		80	125	ns
		for **HBF** types		80	150	ns
t_{TLH}, t_{THL}	Transition time	V_{DD} = 5V				
		for **HBC** types		175	225	ns
		for **HBF** types		175	250	ns
		V_{DD} = 10V				
		for **HBC** types		80	125	ns
		for **HBF** types		80	150	ns
t_{pwH}, t_{pwL}	Minimum clock pulse width	V_{DD} = 5V				
		for **HBC** types		200	330	ns
		for **HBF** types		200	500	ns
		V_{DD} = 10V				
		for **HBC** types		140	125	ns
		for **HBF** types		140	165	ns
$t_{\phi r}$, $t_{\phi f}$	Clock rise and fall time	V_{DD} = 5V				
		for **HBC** types			15	μs
		for **HBF** types			15	μs
		V_{DD} = 10V				
		for **HBC** types			10	μs
		for **HBF** types			10	μs
f_{max}	Maximum clock frequency	V_{DD} = 5V				
		for **HBC** types	1.5	2.5		MHz
		for **HBF** types	1	2.5		MHz
		V_{DD} = 10V				
		for **HBC** types	4	7		MHz
		for **HBF** types	3	7		MHz
C_i	Input capacitance	Any input for **HBC** and **HBF** types		5		pF

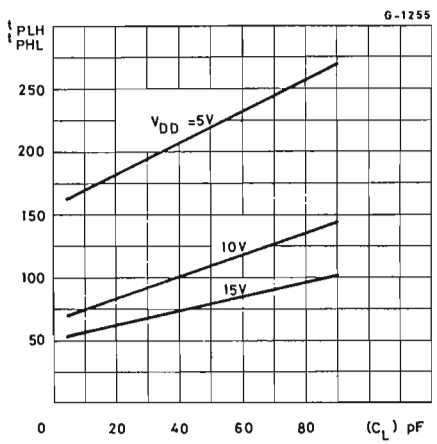
DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
RESET OPERATION						
t_{PHL}	Propagation delay time	$V_{DD} = 5V$				
		for **HBC** types		500	700	ns
		for **HBF** types		500	800	ns
		$V_{DD} = 10V$				
		for **HBC** types		250	350	ns
		for **HBF** types		250	400	ns
t_{pwH}	Minimum reset pulse width	$V_{DD} = 5V$				
		for **HBC** types		375	500	ns
		for **HBF** types		375	600	ns
		$V_{DD} = 10V$				
		for **HBC** types		200	300	ns
		for **HBF** types		200	350	ns

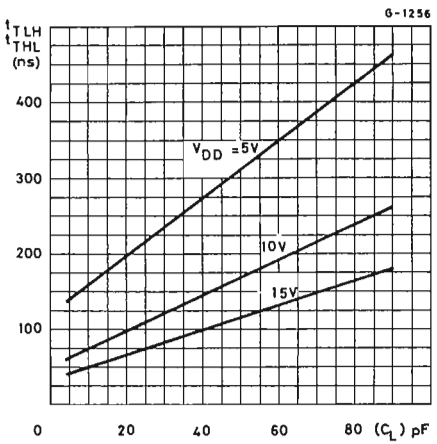


Typical input pulse frequency vs. V_{DD}

Typical propagation delay time vs. C_L



Typical transition time vs. C_L



COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

DUAL J-K MASTER-SLAVE FLIP-FLOP

- LOW QUIESCENT POWER DISSIPATION
- WIDE SUPPLY VOLTAGE RANGE: 3 to 15V
- HIGH NOISE IMMUNITY: 45% of V_{DD} (TYP.)
- MEDIUM SPEED OPERATION: 8MHz (TYP.) CLOCK TOGGLE RATE at V_{DD}-V_{SS}= 10V
- INPUTS FULLY PROTECTED
- LOW OUTPUT IMPEDANCE
- HIGH FANOUT

The **HBC 4027A** (extended temperature range) and **HBF 4027A** (standard temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package.
The dual J-K flip-flop is constructed with MOS N-channel and P-channel enhancement mode transistors.
Each flip-flop has independent "J", "K", "clock", "set" and "reset" inputs.
These devices may be used in control registers or toggle functions. They find primary use where very low power dissipation and/or high immunity inherent in COS/MOS offers system advantage.

ABSOLUTE MAXIMUM RATINGS

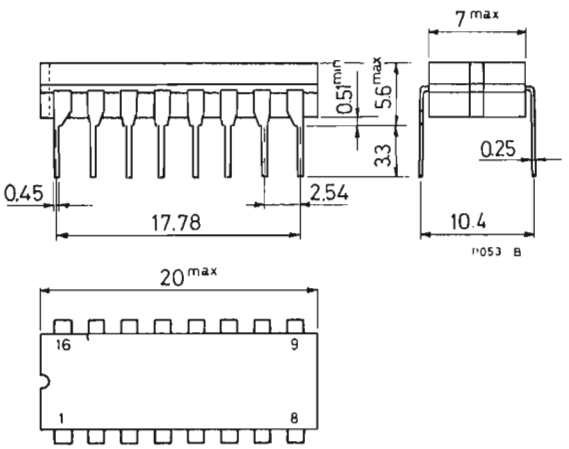
V_{DD}-V_{SS}	Supply voltage	-0.5 to 15	V
V_i	Input voltage (at any pin)	$V_{SS} \leqslant V_I \leqslant V_{DD}$	
P_{tot}	Total power dissipation (per package)	200	mW
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature: for **HBC** types	-55 to 125	°C
	for **HBF** types	-40 to 85	°C

ORDERING NUMBERS:

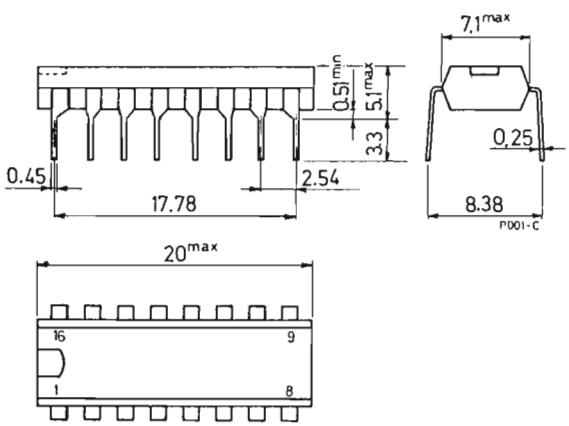
HBC 4027 AD for dual in-line ceramic package
HBC 4027 AF for dual in-line ceramic package, frit seal (extended temperature range)
HBC 4027 AK for ceramic flat package
HBF 4027 AE for dual in-line plastic package
HBF 4027 AF for dual in-line ceramic package, frit seal (standard temperature range)

MECHANICAL DATA (dimensions in mm)

Dual in-line ceramic package
for HBC 4027 AD and
HBC/HBF 4027 AF

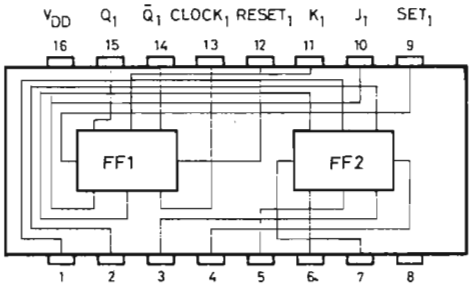


Dual in-line plastic package
for HBF 4027 AE



Ceramic flat package for HBC 4027 AK

CONNECTION DIAGRAM (top view)



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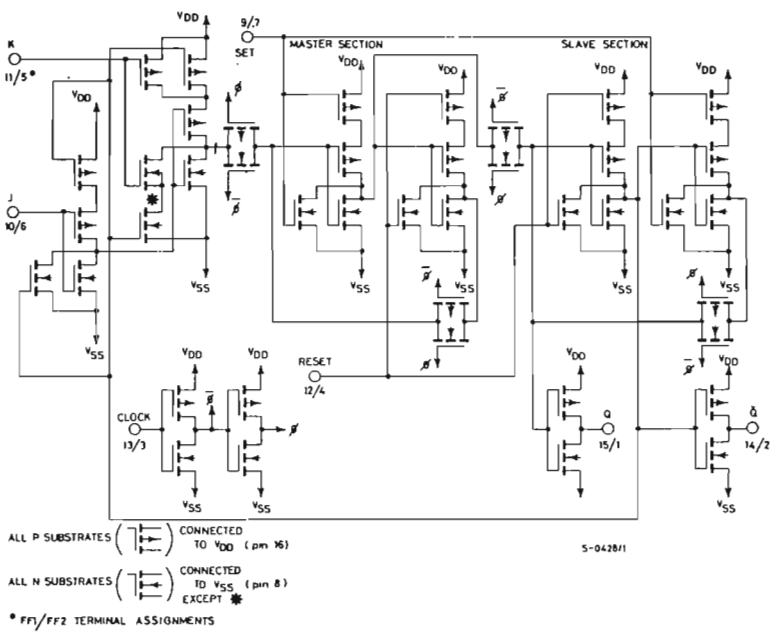
SCHEMATIC DIAGRAM



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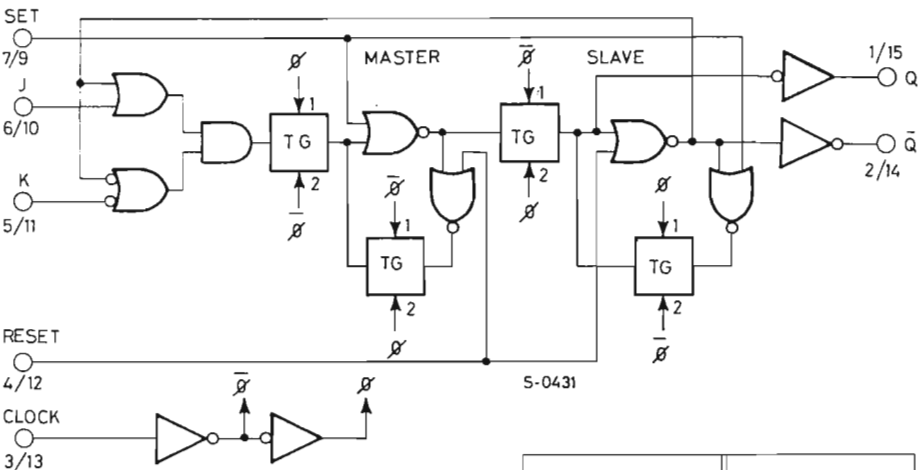
FUNCTIONAL LOGIC DIAGRAM and TRUTH TABLE



t_{n-1} INPUTS (1)						t_n OUTPUTS (2)		
ϕ	J	K	S	R	Q	Q	$\bar{Q}$	
⌒	1	X	0	0	0	1	0	
⌒	X	0	0	0	1	1	0	
⌒	0	X	0	0	0	0	1	
⌒	X	1	0	0	1	0	1	
⌒	X	X	0	0	X			← (No Change)
X	X	X	1	0	X	1	0	
X	X	X	0	1	X	0	1	
X	X	X	1	1	X	*	*	

X DON'T CARE

* INVALID CONDITION

(1) t_{n-1} REFERS TO THE TIME INTERVAL PRIOR TO THE POSITIVE CLOCK PULSE TRANSITION

(2) t_n REFERS TO THE TIME INTERVALS AFTER THE POSITIVE CLOCK PULSE TRANSITION

WHERE 1 = HIGH LEVEL
0 = LOW LEVEL

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage	3 to 15 V
V_i*	Input voltage	V_{DD} to V_{SS}
T_{op}	Operating temperature: for **HBC** types	-55 to 125 °C
	for **HBF** types	-40 to 85 °C

* This is measured with respect to the V_{SS} pin voltage

STATIC ELECTRICAL CHARACTERISTICS

Parameter		Test conditions	Min.	Typ.	Max.	Unit
HBC types (extended temperature range)						
I_L	Quiescent current	V_{DD}= 5V				
		at T_{amb}= -55°C			1	μA
		at T_{amb}= 25°C		0.005	1	μA
		at T_{amb}= 125°C			60	μA
		V_{DD}= 10V				
		at T_{amb}= -55°C			2	μA
		at T_{amb}= 25°C		0.005	2	μA
		at T_{amb}= 125°C			120	μA
V_{OH}	Output high voltage	I_o = O				
		V_{DD}= 5V				
		at T_{amb}= -55°C	4.99			V
		at T_{amb}= 25°C	4.99	5		V
		at T_{amb}= 125°C	4.95			V
		V_{DD}= 10V				
		at T_{amb}= -55°C	9.99			V
		at T_{amb}= 25°C	9.99	10		V
		at T_{amb}= 125°C	9.95			V
V_{OL}	Output low voltage	I_o = O				
		V_{DD}= 5V or 10V				
		at T_{amb}= -55°C			0.01	V
		at T_{amb}= 25°C		0	0.01	V
		at T_{amb}= 125°C			0.05	V
→ V_{NH}	Noise immunity	V_{DD}= 5V V_o = 4.2V				
		at T_{amb}= -55°C	1.4			V
		at T_{amb}= 25°C	1.5	2.25		V
		at T_{amb}= 125°C	1.5			V
		V_{DD}=10V V_o= 9V				
		at T_{amb}= -55°C	2.9			V
		at T_{amb}= 25°C	3	4.5		V
		at T_{amb}= 125°C	3			V

STATIC ELECTRICAL CHARACTERISTICS (continued)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit
→ V_{NL}	Noise immunity	V_{DD}= 5V V_o = 0.8V				
		at T_{amb}= -55°C	1.5			V
		at T_{amb}= 25°C	1.5	2.25		V
		at T_{amb}= 125°C	1.4			V
		V_{DD}=10V V_o = 1V				
		at T_{amb}= -55°C	3			V
		at T_{amb}= 25°C	3		4.5	V
		at T_{amb}= 125°C	2.9			V
I_DN	Output drive current N-channel	V_{DD}= 5V V_o = 0.5V				
		at T_{amb}= -55°C	0.63			mA
		at T_{amb}= 25°C	0.5		1	mA
		at T_{amb}= 125°C	0.33			mA
		V_{DD}= 10V V_o = 0.5V				
		at T_{amb}= -55°C	1.25			mA
		at T_{amb}= 25°C	1		2.5	mA
		at T_{amb}= 125°C	0.7			mA
I_DP	Output drive current P-channel	V_{DD}= 5V V_o = 4.5V				
		at T_{amb}= -55°C	-0.31			mA
		at T_{amb}= 25°C	-0.25		-0.5	mA
		at T_{amb}= 125°C	-0.175			mA
		V_{DD}=10V V_o = 9.5V				
		at T_{amb}= -55°C	-0.8			mA
		at T_{amb}= 25°C	-0.65		-1.3	mA
		at T_{amb}= 125°C	-0.45			mA
I_i	Input current	T_{amb} = 25°C			10	pA

HBF types (standard temperature range)

I_L	Quiescent current	V_{DD}= 5V				
		at T_{amb}= -40°C			10	μA
		at T_{amb}= 25°C		0.01	10	μA
		at T_{amb}= 85°C			140	μA

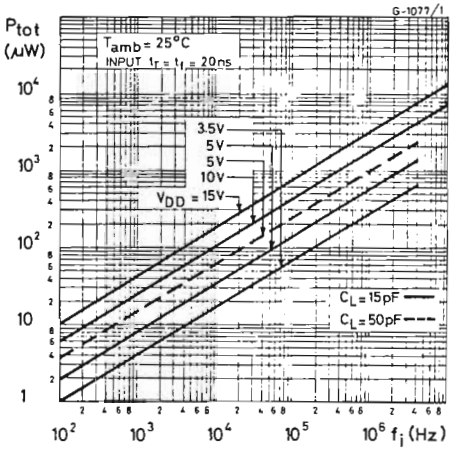
STATIC ELECTRICAL CHARACTERISTICS (continued)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_L	Quiescent current	V_{DD} = 10V				
		at T_{amb}= -40°C			20	µA
		at T_{amb}= 25°C		0.05	20	µA
		at T_{amb}= 85°C			280	µA
V_{OH}	Output high voltage	I_o = 0				
		V_{DD} = 5V				
		at T_{amb}= -40°C	4.99			V
		at T_{amb}= 25°C	4.99	5		V
		at T_{amb}= 85°C	4.95			V
		V_{DD}= 10V				
		at T_{amb}= -40°C	9.99			V
		at T_{amb}= 25°C	9.99	10		V
		at T_{amb}= 85°C	9.95			V
V_{OL}	Output low voltage	I_o = 0				
		V_{DD} = 5V or 10V				
		at T_{amb}= -40°C			0.01	V
		at T_{amb}= 25°C		0	0.01	V
		at T_{amb}= 85°C			0.05	V
→ V_{NH}	Noise immunity	V_{DD} = 5V V_o = 4.2V				
		at T_{amb}= -40°C	1.4			V
		at T_{amb}= 25°C	1.5	2.25		V
		at T_{amb}= 85°C	1.5			V
		V_{DD}= 10V V_o = 9V				
		at T_{amb}= -40°C	2.9			V
		at T_{amb}= 25°C	3	4.5		V
		at T_{amb}= 85°C	3			V
→ V_{NL}	Noise immunity	V_{DD}= 5V V_o = 0.8V				
		at T_{amb}= -40°C	1.5			V
		at T_{amb}= 25°C	1.5	2.25		V
		at T_{amb}= 85°C	1.4			V

STATIC ELECTRICAL CHARACTERISTICS (continued)

	Parameter		Test conditions	Min.	Typ.	Max.	Unit
→	V_{NL}	Noise immunity	V_{DD}=10V V_o = 1V				
			at T_{amb}= -40°C	3			V
			at T_{amb}= 25°C	3		4.5	V
			at T_{amb}= 85°C	2.9			V
	I_DN	Output drive current N-channel	V_{DD}= 5V V_o = 0.5V				
			at T_{amb}= -40°C	0.3			mA
			at T_{amb}= 25°C	0.3		1	mA
			at T_{amb}= 85°C	0.24			mA
			V_{DD}=10V V_o = 0.5V				
			at T_{amb}= -40°C	0.72			mA
			at T_{amb}= 25°C	0.6		2.5	mA
			at T_{amb}= 85°C	0.5			mA
	I_DP	Output drive current P-channel	V_{DD} = 5V V_o = 4.5V				
			at T_{amb}= -40°C		- 0.17		mA
			at T_{amb}= 25°C		- 0.14	-0.5	mA
			at T_{amb}= 85°C		- 0.063		mA
			V_{DD}=10V V_o = 9.5V				
			at T_{amb}= -40°C		- 0.4		mA
			at T_{amb}= 25°C		- 0.33	-1.3	mA
			at T_{amb}= 85°C		- 0.27		mA
	I_i	Input current	T_{amb}= 25°C		10		pA

Typical power dissipation characteristics



DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 15 pF, typical coefficient temperature for all values of V_{DD} = 0.3%/°C, input t_r and t_f = 20 ns except $t_{\phi r}$ and $t_{\phi f}$)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{PLH}, t_{PHL} Propagation delay time	V_{DD} = 5V				
	for **HBC** types		150	300	ns
	for **HBF** types		150	400	ns
	V_{DD} = 10V				
	for **HBC** types		75	110	ns
	for **HBF** types		75	150	ns
t_{TLH}, t_{THL} Transition time	V_{DD} = 5V				
	for **HBC** types		75	125	ns
	for **HBF** types		75	250	ns
	V_{DD} = 10V				
	for **HBC** types		50	70	ns
	for **HBF** types		50	140	ns

DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
t_{pwH}, t_{pwL}	Minimum clock pulse width	V_{DD} = 5V				
		for **HBC** types		165	330	ns
		for **HBF** types		165	500	ns
		V_{DD} = 10V				
		for **HBC** types		65	110	ns
		for **HBF** types		65	165	ns
$t_{\phi r}$, $t_{\phi f}$	Clock rise and fall time	V_{DD} = 5V				
		for **HBC** and **HBF** types			15	μs
		V_{DD} = 10V				
		for **HBC** and **HBF** types			5	μs
t_s	Set-up time	V_{DD} = 5V				
		for **HBC** types		70	150	ns
		for **HBF** types		70	200	ns
		V_{DD} = 10V				
		for **HBC** types		25	50	ns
		for **HBF** types		25	75	ns
f_{max}	Maximum clock frequency (toggle mode)	V_{DD}= 5V				
		for **HBC** types	1.5	3		MHz
		for **HBF** types	1	3		MHz
		V_{DD} = 10V				
		for **HBC** types	4.5	8		MHz
		for **HBF** types	3	8		MHz
C_I	Input capacitance	Any input for **HBC** and **HBF** types		5		pF

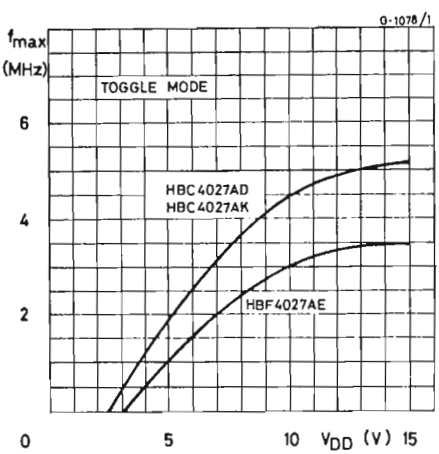
SET and RESET OPERATION

t_{PLH}(S), t_{PHL}(R)	Propagation delay time	V_{DD} = 5V				
		for **HBC** types		175	225	ns
		for **HBF** types		175	350	ns

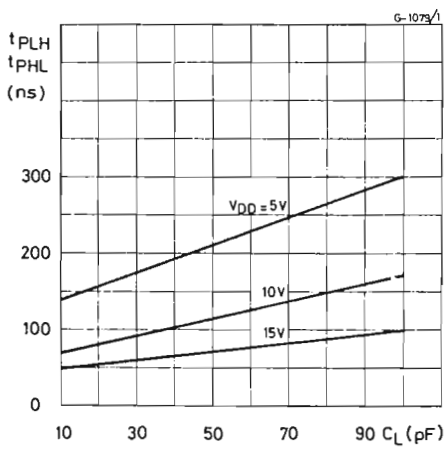
DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{PLH}(S), Propagation delay time t_{PHL}(R)	V_{DD} = 10V				
	for **HBC** types		75	110	ns
	for **HBF** types		75	150	ns
t_{pwH}(S), Minimum set and t_{pwL}(R) reset pulse widths	V_{DD} = 5V				
	for **HBC** types		125	200	ns
	for **HBF** types		125	300	ns
	V_{DD} = 10V				
	for **HBC** types		50	80	ns
	for **HBF** types		50	120	ns

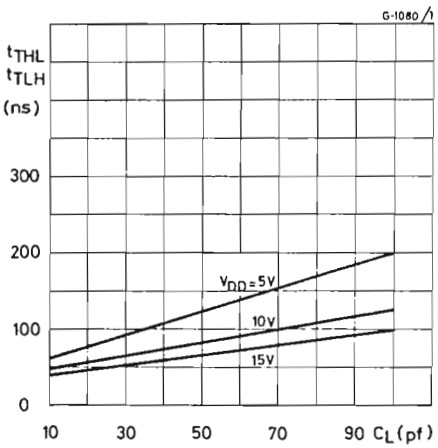
Maximum clock frequency vs. V_{DD}



Typical propagation delay time vs. C_L



Typical transition time vs. C_L



COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

BCD-TO-DECIMAL DECODER

- LOW QUIESCENT POWER DISSIPATION
- WIDE SUPPLY VOLTAGE RANGE: 3 to 15V
- HIGH NOISE IMMUNITY: 45% of V_{DD} (TYP.)
- MEDIUM SPEED OPERATION: $t_{THL} = t_{TLH} = 30$ ns (TYP.) at $V_{DD} = 10V$
- INPUTS FULLY PROTECTED
- LOW OUTPUT IMPEDANCE
- HIGH FAN-OUT
- HIGH DECODED OUTPUT DRIVE CAPABILITY

The HBC 4028A (extended temperature range) and HBF 4028A (standard temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package. These decoders are constructed so that an 8421 BCD code on the four inputs provides a decimal (one-of-ten) decoded output, while a 3-bit binary inputs provides a decoded octal (one-of-eight) code output with D input forced to logic "0". A logic "1" signal at the D input inhibits octal decoding and causes outputs 0 through 7 to go low.

ABSOLUTE MAXIMUM RATINGS

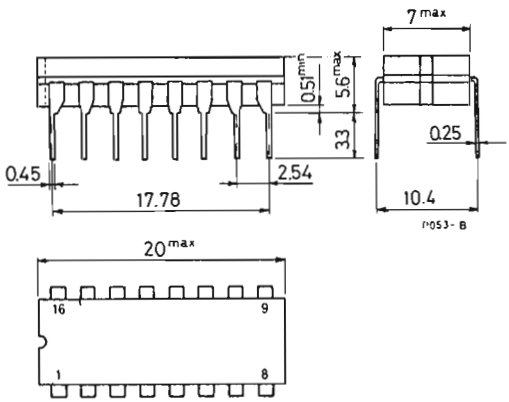
V_{DD}-V_{SS}	Supply voltage	-0.5 to 15 V
V_i	Input voltage (at any pin)	$V_{SS} \leqslant V_I \leqslant V_{DD}$
P_{tot}	Total power dissipation (per package)	200 mW
T_{stg}	Storage temperature	-65 to 150 °C
T_{op}	Operating temperature: for **HBC** types	-55 to 125 °C
	for **HBF** types	-40 to 85 °C

ORDERING NUMBERS:

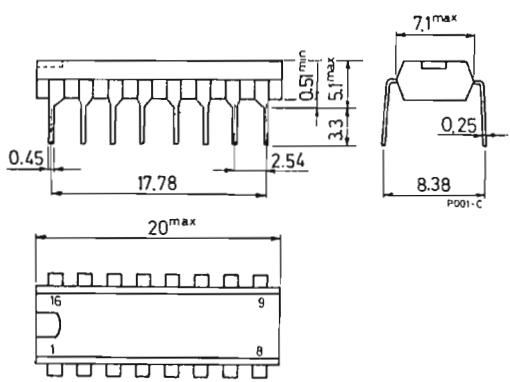
HBC 4028 AD for dual in-line ceramic package
HBC 4028 AF for dual in-line ceramic package frit seal (extended temperature range)
HBC 4028 AK for ceramic flat package
HBF 4028 AE for dual in-line plastic package
HBF 4028 AF for dual in-line ceramic package frit seal (standard temperature range)

MECHANICAL DATA (dimensions in mm)

Dual in-line ceramic package
for HBC 4028 AD and
HBC/HBF 4028 AF

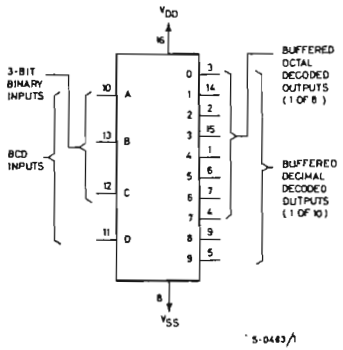


Dual in-line plastic package
for HBF 4028 AE

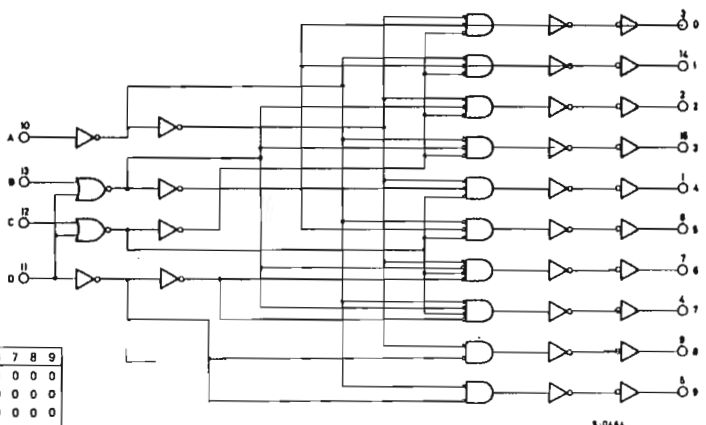


Ceramic flat package for HBC 4028 AK

CONNECTION DIAGRAM



FUNCTIONAL LOGIC DIAGRAM and TRUTH TABLE



D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0
0	1	1	1	0	0	0	0	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1

WHERE 1=HIGH LEVEL
0=LOW LEVEL

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage	3 to 15	V
V_I *	Input voltage	V_{DD} to V_{SS}	
T_{op}	Operating temperature : for HBC types	-55 to 125	°C
	for HBF types	-40 to 85	°C

*This is measured with respect to the V_{SS} pin voltage

STATIC ELECTRICAL CHARACTERISTICS

Parameter		Test conditions	Min.	Typ.	Max.	Unit
HBC types (extended temperature range)						
I_L	Quiescent current	V_{DD} = 5V				
		at T_{amb} = -55°C			5	µA
		at T_{amb} = 25°C		0.5	5	µA
		at T_{amb} = 125°C			300	µA
		V_{DD} = 10V				
		at T_{amb} = -55°C			10	µA
		at T_{amb} = 25°C		1	10	µA
		at T_{amb} = 125°C			600	µA
V_{OH}	Output high voltage	I_o = 0				
		V_{DD} = 5V				
		at T_{amb} = -55°C	4.99			V
		at T_{amb} = 25°C	4.99	5		V
		at T_{amb} = 125°C	4.95			V
		V_{DD} = 10V				
		at T_{amb} = -55°C	9.99			V
		at T_{amb} = 25°C	9.99	10		V
		at T_{amb} = 125°C	9.95			V
V_{OL}	Output low voltage	I_o = 0				
		V_{DD} = 5V or 10V				
		at T_{amb} = -55°C			0.01	V
		at T_{amb} = 25°C		0	0.01	V
		at T_{amb} = 125°C			0.05	V

STATIC ELECTRICAL CHARACTERISTICS (continued)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit
→	V_{NH} Noise immunity	V_{DD} = 5V V_o = 3.6V				
		at T_{amb} = -55°C	1.4			V
		at T_{amb} = 25°C	1.5	2.25		V
		at T_{amb} = 125°C	1.5			V
		V_{DD} = 10V V_o = 7.2V				
		at T_{amb} = -55°C	2.9			V
		at T_{amb} = 25°C	3		4.5	V
		at T_{amb} = 125°C	3			V
→	V_{NL} Noise immunity	V_{DD} = 5V V_o = 0.95V				
		at T_{amb} = -55°C	1.5			V
		at T_{amb} = 25°C	1.5	2.25		V
		at T_{amb} = 125°C	1.4			V
		V_{DD} = 10V V_o = 2.9V				
		at T_{amb} = -55°C	3			V
		at T_{amb} = 25°C	3		4.5	V
		at T_{amb} = 125°C	2.9			V
	I_DN Output drive current N-channel	V_{DD} = 5V V_o = 0.5V				
		at T_{amb} = -55°C	0.75			mA
		at T_{amb} = 25°C	0.6	1.2		mA
		at T_{amb} = 125°C	0.45			mA
		V_{DD} = 10V V_o = 0.5V				
		at T_{amb} = -55°C	1.5			mA
		at T_{amb} = 25°C	1.2	2.4		mA
		at T_{amb} = 125°C	0.9			mA
	I_DP Output drive current P-channel	V_{DD} = 5V V_o = 9.5V				
		at T_{amb} = -55°C	-0.7			mA
		at T_{amb} = 25°C	-0.45	-0.9		mA
		at T_{amb} = 125°C	-0.32			mA
		V_{DD} = 10V V_o = 4.5V				
		at T_{amb} = -55°C	-1.4			mA
		at T_{amb} = 25°C	-0.95	-1.9		mA
		at T_{amb} = 125°C	-0.65			mA

STATIC ELECTRICAL CHARACTERISTICS (continued)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_I	Input current	T_{amb} = 25°C		10		pA

HBF types (standard temperature range)

I_L	Quiescent current	V_{DD}= 5V				
		at T_{amb}= -40°C			50	μA
		at T_{amb}= 25°C		5	50	μA
		at T_{amb}= 85°C			700	μA
		V_{DD}= 10V				
		at T_{amb}= -40°C			100	μA
		at T_{amb}= 25°C		10	100	μA
		at T_{amb}= 85°C			1400	μA
V_{OH}	Output high voltage	I_o = 0				
		V_{DD}= 5V				
		at T_{amb}= -40°C	4.99			V
		at T_{amb}= 25°C	4.99	5		V
		at T_{amb}= 85°C	4.95			V
		V_{DD}= 10V				
		at T_{amb}= -40°C	9.99			V
		at T_{amb}= 25°C	9.99	10		V
		at T_{amb}= 85°C	9.95			V
V_{OL}	Output low voltage	I_o = 0				
		V_{DD}= 5V or 10V				
		at T_{amb}= -40°C			0.01	V
		at T_{amb}= 25°C		0	0.01	V
		at T_{amb}= 85°C			0.05	V
→ V_{NH}	Noise immunity	V_{DD}= 5V V_o = 3.6V				
		at T_{amb}= -40°C	1.4			V
		at T_{amb}= 25°C	1.5	2.25		V
		at T_{amb}= 85°C	1.5			V
		V_{DD}=10V V_o = 7.2V				
		at T_{amb}= -40°C	2.9			V
		at T_{amb}= 25°C	3	4.5		V
		at T_{amb}= 85°C	3			V

STATIC ELECTRICAL CHARACTERISTICS (continued)

	Parameter		Test conditions	Min.	Typ.	Max.	Unit
→	V_{NL}	Noise immunity	V_{DD}= 5V V_o = 0.95V				
			at T_{amb}= -40°C	1.5			V
			at T_{amb}= 25°C	1.5	2.25		V
			at T_{amb}= 85°C	1.4			V
			V_{DD}= 10V V_o = 2.9V				
			at T_{amb}= -40°C	3			V
			at T_{amb}= 25°C	3	4.5		V
			at T_{amb}= 85°C	2.9			V
	I_DN	Output drive current N-channel	V_{DD}= 5V V_o = 0.5V				
			at T_{amb}= -40°C	0.35			mA
			at T_{amb}= 25°C	0.3	1.2		mA
			at T_{amb}= 85°C	0.25			mA
			V_{DD}=10V V_o= 0.5V				
			at T_{amb}= -40°C	0.7			mA
			at T_{amb}= 25°C	0.6	2.4		mA
			at T_{amb}= 85°C	0.5			mA
	I_DP	Output drive current P-channel	V_{DD}= 5V V_o = 4.5V				
			at T_{amb}= -40°C	-0.32			mA
			at T_{amb}= 25°C	-0.22	-0.9		mA
			at T_{amb}= 85°C	-0.18			mA
			V_{DD}=10V V_o = 9.5V				
			at T_{amb}= -40°C	-0.65			mA
			at T_{amb}= 25°C	-0.48	-1.9		mA
			at T_{amb}= 85°C	-0.4			mA
	I_i	Input current	T_{amb} = 25°C		10		pA

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 15 pF, typical coefficient temperature for all values of V_{DD} = 0.3%/°C, and all input rise and fall times = 20 ns)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
t_{PLH}	Propagation delay time (low to high level)	V_{DD} = 5V				
		for **HBC** types		250	480	ns
		for **HBF** types		250	700	ns
		V_{DD} = 10V				
		for **HBC** types		100	180	ns
		for **HBF** types		100	290	ns
t_{PHL}	Propagation delay time (high to low level)	V_{DD} = 5V				
		for **HBC** types		250	480	ns
		for **HBF** types		250	700	ns
		V_{DD} = 10V				
		for **HBC** types		100	180	ns
		for **HBF** types		100	290	ns
t_{TLH}	Transition time (low to high level)	V_{DD} = 5V				
		for **HBC** types		60	150	ns
		for **HBF** types		60	300	ns
		V_{DD} = 10V				
		for **HBC** types		30	75	ns
		for **HBF** types		30	150	ns
t_{THL}	Transition time (high to low level)	V_{DD} = 5V				
		for **HBC** types		60	150	ns
		for **HBF** types		60	300	ns
		V_{DD} = 10V				
		for **HBC** types		30	75	ns
		for **HBF** types		30	150	ns
C_I	Input capacitance	Any input for **HBC** and **HBF** types		5		pF

Fig. 1 - Typical propagation delay time versus C_L

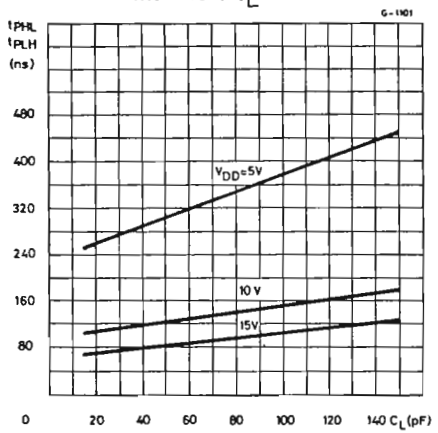


Fig. 2 - Typical transition time versus C_L

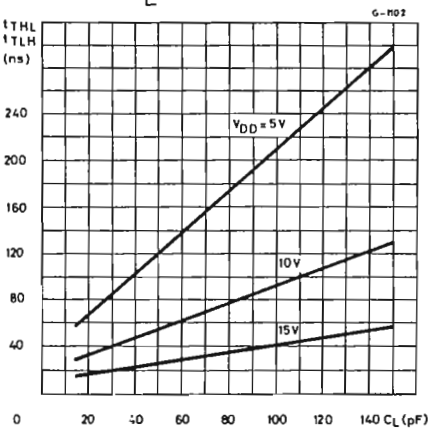


Fig. 3 - Maximum propagation delay time versus V_{DD}

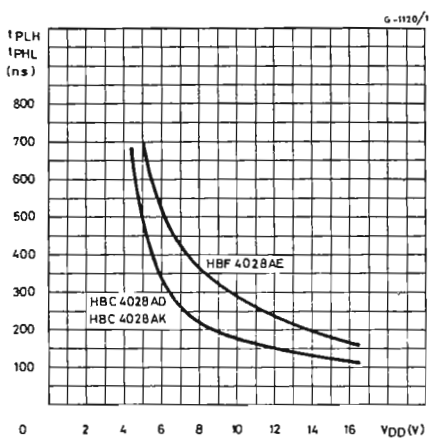
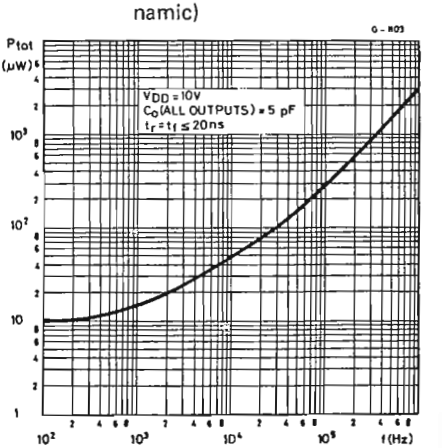


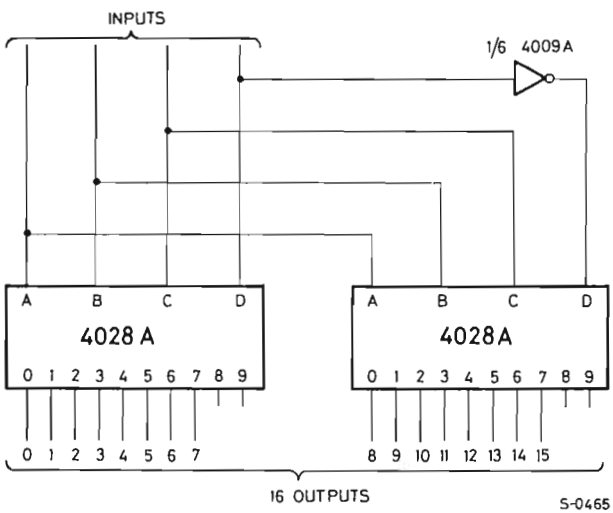
Fig. 4 - Total power dissipation characteristics (quiescent + dynamic)



TYPICAL APPLICATIONS

The circuit shown in fig. 5 converts any 4-bit code to a decimal or hexadecimal code. Fig.6 shows a number of codes and the decimal or hexadecimal number in these codes which must be applied to the input pins of the HBC/HBF 4028A to select a particular output. For example: in order to get a "high" on output n. 8 the input must be either an 8 expressed in 4-bit binary code, a 15 expressed in 4-bit Gray code, or a 5 expressed in Excess-3 code.

Fig. 5 - Code conversion circuit

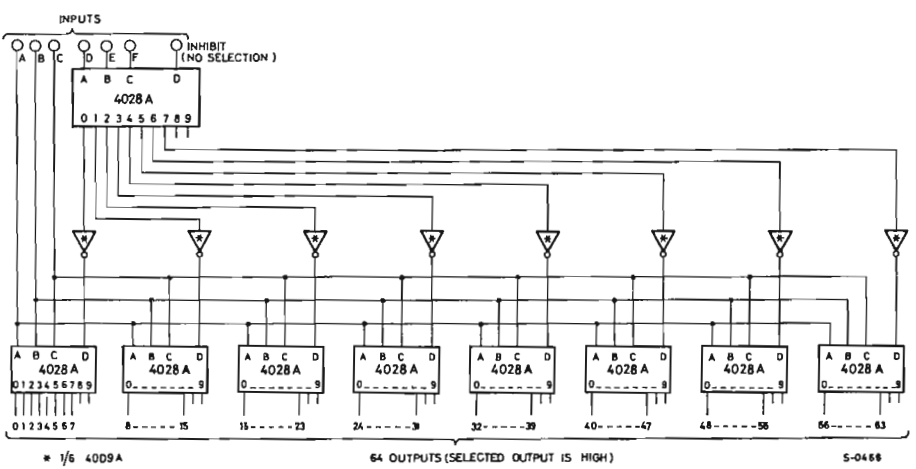


TYPICAL APPLICATIONS (continued)

Fig. 6 - Code conversion chart

INPUTS				INPUT CODES							OUTPUT NUMBER																
				Hexa Decimal		Decimal																					
D	C	B	A	4 BIT BINARY	4 BIT GRAY	EXCESS 3	EXCESS 3 GRAY	AIKEN	4221		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0			0	0		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	1			1	1		0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	2	3		0	2	2		0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	3	2	0	3	3			0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	4	7	1	4	4			0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	1	0	1	5	6	2			3		0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	1	1	0	6	4	3	1		4		0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	1	1	1	7	5	4	2				0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	0	8	15	5					0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	9	14	6			5		0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
1	0	1	0	10	12	7	9		6		0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
1	0	1	1	11	13	8		5			0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1	1	0	0	12	8	9	5	6			0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
1	1	0	1	13	9		6	7	7		0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
1	1	1	0	14	11		8	8	8		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
1	1	1	1	15	10		7	9	9		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Fig. 7 - 6-bit binary to 1 of 64 address decoder



COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

PRESETTABLE UP/DOWN COUNTER

- LOW QUIESCENT POWER DISSIPATION
- WIDE SUPPLY VOLTAGE RANGE : 3 to 15V
- HIGH NOISE IMMUNITY : 45% of V_{DD} (TYP.)
- MEDIUM SPEED OPERATION: 5MHz (TYP.) at $C_L = 15pF$ and $V_{DD}-V_{SS}=10V$
- INPUTS FULLY PROTECTED
- LOW OUTPUT IMPEDANCE
- BINARY OR DECADE UP/DOWN COUNTING

The **HBC 4029A** (extended temperature range) and **HBF 4029A** (standard temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package, containing N-channel and P-channel enhancement mode transistors. The device consists of a four-stage binary or BCD-decade up/down counter with provisions for "look-ahead" carry in both counting modes. The inputs consist of a single Clock, Carry-in (Clock Enable), Binary/Decade, Up/Down, Preset Enable, and four individual Jam signals. Four separate buffered Q signals and Carry Out signal are provided as outputs.

ABSOLUTE MAXIMUM RATINGS

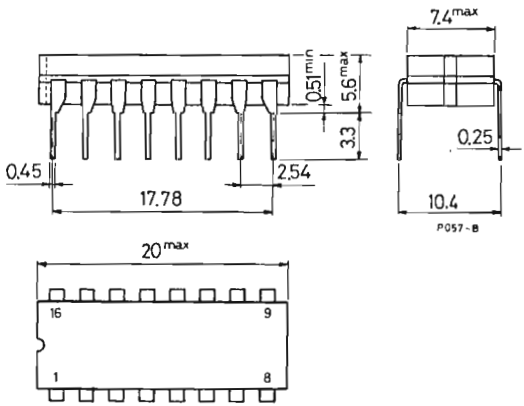
$V_{DD}-V_{SS}$	Supply voltage		-0.5 to 15 V
V_i	Input voltage (at any pin)		$V_{SS} \leqslant V_i \leqslant V_{DD}$
P_{tot}	Total power dissipation (per package)		200 mW
T_{stg}	Storage temperature		-65 to 150 °C
T_{op}	Operating temperature :	for **HBC** types	-55 to 125 °C
		for **HBF** types	-40 to 85 °C

ORDERING NUMBERS:

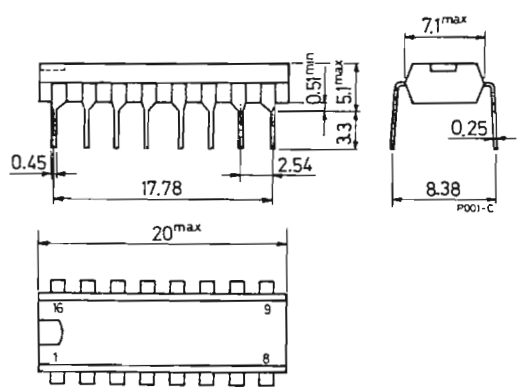
HBC 4029 AD for dual in-line ceramic package
HBC 4029 AF for dual in-line ceramic package, frit seal (extended temperature range)
HBC 4029 AK for ceramic flat package
HBF 4029 AE for dual in-line plastic package
HBF 4029 AF for dual in-line ceramic package, frit seal (standard temperature range)

MECHANICAL DATA (dimensions in mm)

Dual in-line ceramic package
for HBC 4029 AD and
HBC/HBF 4029 AF

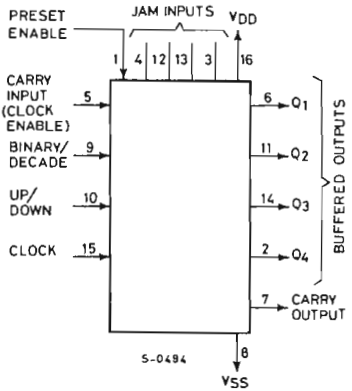


Dual in-line plastic package
for HBF 4029 AE



Ceramic flat package for HBC 4029 AK

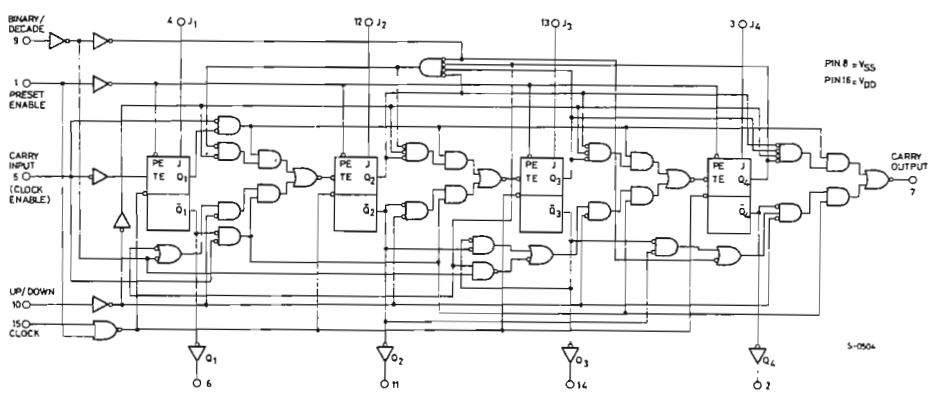
CONNECTION DIAGRAM



TRUTH TABLE

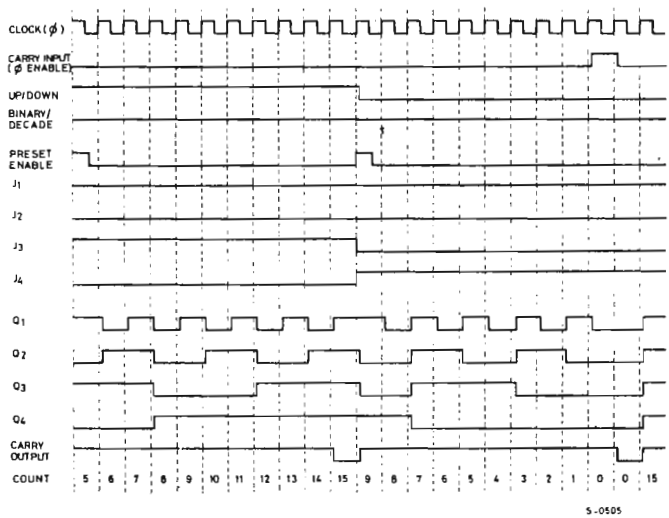
CONTROL INPUT	LOGIC LEVEL	ACTION
BIN/DEC. (B/D)	1 0	BINARY COUNT DECADE COUNT
UP/DOWN (U/D)	1 0	UP COUNT DOWN COUNT
PRESET ENABLE (PE)	1 0	JAM IN NO JAM
CARRY IN (CI) (CLOCK ENABLE)	1 0	NO COUNTER ADVANCE AT POS. CLOCK TRANSITION ADVANCE COUNTER AT POS. CLOCK TRANSITION

SCHEMATIC DIAGRAM

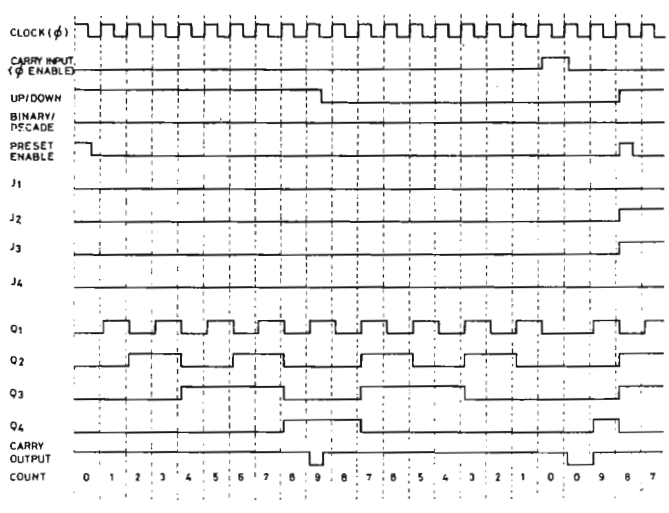


TIMING DIAGRAMS

Binary mode



Decade mode



RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage		3 to 15 V
V_i*	Input voltage		V_{DD} to V_{SS}
T_{op}	Operating temperature :	for **HBC** types	-55 to 125 °C
		for **HBF** types	-40 to 85 °C

* This is measured with respect to the V_{SS} pin voltage

STATIC ELECTRICAL CHARACTERISTICS

Parameter		Test conditions	Min.	Typ.	Max.	Unit
HBC types (extended temperature range)						
I_L	Quiescent current	V_{DD} = 5V				
		at T_{amb} = -55°C			5	µA
		at T_{amb} = 25°C		0.3	5	µA
		at T_{amb} = 125°C			300	µA
		V_{DD} = 10V				
		at T_{amb} = -55°C			10	µA
		at T_{amb} = 25°C		0.5	10	µA
		at T_{amb} = 125°C			600	µA
V_{OH}	Output high voltage	I_o = 0				
		V_{DD} = 5V				
		at T_{amb} = -55°C	4.99			V
		at T_{amb} = 25°C	4.99	5		V
		at T_{amb} = 125°C	4.95			V
		V_{DD} = 10V				
		at T_{amb} = -55°C	9.99			V
		at T_{amb} = 25°C	9.99	10		V
		at T_{amb} = 125°C	9.95			V
V_{OL}	Output low voltage	I_o = 0				
		V_{DD} = 5V or 10V				
		at T_{amb} = -55°C			0.01	V
		at T_{amb} = 25°C			0.01	V
		at T_{amb} = 125°C			0.05	V

STATIC ELECTRICAL CHARACTERISTICS (continued)

	Parameter		Test conditions	Min.	Typ.	Max.	Unit
→	V_{NH}	Noise immunity	V_{DD} = 5V V_o = 4.2V				
			at T_{amb} = -55°C	1.4			V
			at T_{amb} = 25°C	1.5	2.25		V
			at T_{amb} = 125°C	1.5			V
			V_{DD} = 10V V_o = 9V				
			at T_{amb} = -55°C	2.9			V
			at T_{amb} = 25°C	3	4.5		V
			at T_{amb} = 125°C	3			V
→	V_{NL}	Noise immunity	V_{DD} = 5V V_o = 0.8V				
			at T_{amb} = -55°C	1.5			V
			at T_{amb} = 25°C	1.5	2.25		V
			at T_{amb} = 125°C	1.4			V
			V_{DD} = 10V V_o = 1V				
			at T_{amb} = -55°C	3			V
			at T_{amb} = 25°C	3	4.5		V
			at T_{amb} = 125°C	2.9			V
	I_DN	Drive current N-channel	Q outputs				
			V_{DD} = 5V V_o = 0.5V				
			at T_{amb} = -55°C	0.5			mA
			at T_{amb} = 25°C	0.4	0.8		mA
			at T_{amb} = 125°C	0.28			mA
			V_{DD} = 10V V_o = 0.5V				
			at T_{amb} = -55°C	0.74			mA
			at T_{amb} = 25°C	0.6	1.2		mA
			at T_{amb} = 125°C	0.42			mA
			Carry output				
			V_{DD} = 5V V_o = 0.5V				
			at T_{amb} = -55°C	0.1			mA
			at T_{amb} = 25°C	0.08	0.16		mA
			at T_{amb} = 125°C	0.06			mA
			V_{DD} = 10V V_o = 0.5V				
			at T_{amb} = -55°C	0.4			mA
			at T_{amb} = 25°C	0.32	0.64		mA
			at T_{amb} = 125°C	0.22			mA

STATIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_DP	Drive current P-channel	Q outputs				
		$V_{DD} = 5V$ $V_o = 4.5V$				
		at $T_{amb} = -55°C$	-0.18			mA
		at $T_{amb} = 25°C$	-0.12	-0.24		mA
		at $T_{amb} = 125°C$	-0.08			mA
		$V_{DD} = 10V$ $V_o = 9.5V$				
		at $T_{amb} = -55°C$	-0.3			mA
		at $T_{amb} = 25°C$	-0.2	-0.4		mA
		at $T_{amb} = 125°C$	-0.14			mA
		Carry output				
		$V_{DD} = 5V$ $V_o = 4.5V$				
		at $T_{amb} = -55°C$	-0.09			mA
		at $T_{amb} = 25°C$	-0.06	-0.12		mA
		at $T_{amb} = 125°C$	-0.04			mA
		$V_{DD} = 10V$ $V_o = 9.5V$				
		at $T_{amb} = -55°C$	-0.15			mA
		at $T_{amb} = 25°C$	-0.1	-0.2		mA
		at $T_{amb} = 125°C$	-0.07			mA
I_I	Input current	$T_{amb} = 25°C$		10		pA

HBF types (standard temperature range)

I_L	Quiescent current	$V_{DD} = 5V$				
		at $T_{amb} = -40°C$			50	μA
		at $T_{amb} = 25°C$		0.5	50	μA
		at $T_{amb} = 85°C$			700	μA
		$V_{DD} = 10V$				
		at $T_{amb} = -40°C$			100	μA
		at $T_{amb} = 25°C$		1	100	μA
		at $T_{amb} = 85°C$			1400	μA
V_{OH}	Output high voltage	$I_o = 0$ $V_{DD} = 5V$				
		at $T_{amb} = -40°C$	4.99			V
		at $T_{amb} = 25°C$	4.99	5		V
		at $T_{amb} = 85°C$	4.95			V

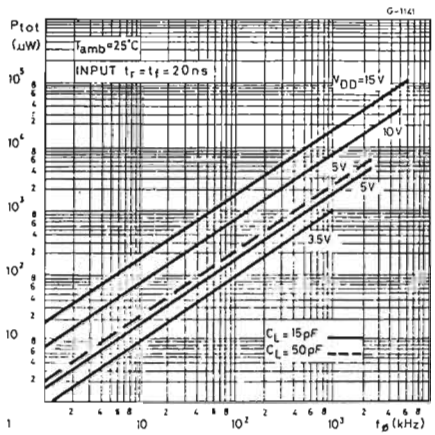
STATIC ELECTRICAL CHARACTERISTICS (continued)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OH}	Output high voltage	$I_o = 0$				
		$V_{DD} = 10V$				
		at T_{amb}= -40°C	9.99			V
		at T_{amb}= 25°C	9.99	10		V
		at T_{amb}= 85°C	9.95			V
V_{OL}	Output low voltage	$I_o = 0$				
		V_{DD} = 5V or 10V				
		at T_{amb}= -40°C			0.01	V
		at T_{amb}= 25°C			0.01	V
		at T_{amb}= 85°C			0.05	V
→ V_{NH}	Noise immunity	V_{DD} = 5V V_o = 4.2V				
		at T_{amb}= -40°C	1.4			V
		at T_{amb}= 25°C	1.5	2.25		V
		at T_{amb}= 85°C	1.5			V
		V_{DD} = 10V V_o = 9V				
		at T_{amb}= -40°C	2.9			V
		at T_{amb}= 25°C	3	4.5		V
		at T_{amb}= 85°C	3			V
→ V_{NL}	Noise immunity	V_{DD} = 5V V_o = 0.8V				
		at T_{amb}= -40°C	1.5			V
		at T_{amb}= 25°C	1.5	2.25		V
		at T_{amb}= 85°C	1.4			V
		V_{DD} = 10V V_o = 1V				
		at T_{amb}= -40°C	3			V
		at T_{amb}= 25°C	3	4.5		V
		at T_{amb}= 85°C	2.9			V
I_DN	Drive current N-channel	Q outputs				
		V_{DD} = 5V V_o = 0.5V				
		at T_{amb}= -40°C	0.24			mA
		at T_{amb}= 25°C	0.2	0.8		mA
		at T_{amb}= 85°C	0.16			mA
		V_{DD} = 10V V_o = 0.5V				
		at T_{amb}= -40°C	0.36			mA
		at T_{amb}= 25°C	0.3	1.2		mA
		at T_{amb}= 85°C	0.24			mA

STATIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
$I_D N$	Drive current N-channel	Carry output				
		$V_{DD} = 5V$ $V_o = 0.5V$				
		at $T_{amb} = -40°C$	0.05			mA
		at $T_{amb} = 25°C$	0.04		0.16	mA
		at $T_{amb} = 85°C$	0.03			mA
		$V_{DD} = 10V$ $V_o = 0.5V$				
		at $T_{amb} = -40°C$	0.19			mA
		at $T_{amb} = 25°C$	0.16		0.64	mA
		at $T_{amb} = 85°C$	0.13			mA
$I_D P$	Drive current P-channel	Q outputs				
		$V_{DD} = 5V$ $V_o = 4.5V$				
		at $T_{amb} = -40°C$	-0.07			mA
		at $T_{amb} = 25°C$	-0.06		-0.24	mA
		at $T_{amb} = 85°C$	-0.05			mA
		$V_{DD} = 10V$ $V_o = 9.5V$				
		at $T_{amb} = -40°C$	-0.14			mA
		at $T_{amb} = 25°C$	-0.1		-0.4	mA
		at $T_{amb} = 85°C$	-0.08			mA
		Carry output				
		$V_{DD} = 5V$ $V_o = 4.5V$				
		at $T_{amb} = -40°C$	-0.04			mA
		at $T_{amb} = 25°C$	-0.03		-0.12	mA
		at $T_{amb} = 85°C$	-0.02			mA
		$V_{DD} = 10V$ $V_o = 9.5V$				
		at $T_{amb} = -40°C$	-0.07			mA
		at $T_{amb} = 25°C$	-0.05		-0.2	mA
		at $T_{amb} = 85°C$	-0.04			mA
I_i	Input current	$T_{amb} = 25°C$		10		pA

Typical power dissipation characteristics



DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, C_L= 15 pF, typical temperature coefficient for all V_{DD}= 0.3%/°C values, all input rise and fall time = 20 ns, except $t_{\phi r}$ and $t_{\phi f}$)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
CLOCKED OPERATION					
t_{PLH}, t_{PHL} Propagation delay time	Q outputs				
	V_{DD} = 5V				
	for **HBC** types		325	650	ns
	for **HBF** types		325	1300	ns
	V_{DD} = 10V				
	for **HBC** types		115	230	ns
	for **HBF** types		115	460	ns
	Carry output				
	V_{DD} = 5V				
	for **HBC** types		425	850	ns
	for **HBF** types		425	1700	ns
	V_{DD} = 10V				
	for **HBC** types		150	300	ns
	for **HBF** types		150	600	ns

DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
t_{TLH}, t_{THL}	Transition time	Q outputs				
		V_{DD} = 5V				
		for **HBC** types		100	200	ns
		for **HBF** types		100	400	ns
		V_{DD} = 10V				
		for **HBC** types		50	100	ns
		for **HBF** types		50	200	ns
		Carry output				
		V_{DD} = 5V				
		for **HBC** types		200	400	ns
		for **HBF** types		200	800	ns
		V_{DD} = 10V				
		for **HBC** types		100	200	ns
		for **HBF** types		100	400	ns
t_{pwH}, t_{pwL}	Minimum clock pulse width	V_{DD} = 5V				
		for **HBC** types		200	340	ns
		for **HBF** types		200	500	ns
		V_{DD} = 10V				
		for **HBC** types		100	170	ns
		for **HBF** types		100	250	ns
$t\phi_r$,* $t\phi_f$	Clock rise and fall time	V_{DD} = 5V or 10V for **HBC** and **HBF** types			15	μs
t_s **	Set-up time	V_{DD} = 5V				
		for **HBC** types		325	650	ns
		for **HBF** types		325	1300	ns
		V_{DD} = 10V				
		for **HBC** types		115	230	ns
		for **HBF** types		115	460	ns

DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
f_{max}	Maximum clock frequency	$V_{DD} = 5V$				
		for **HBC** types	1.5	2.5		MHz
		for **HBF** types	1	2.5		MHz
		$V_{DD} = 10V$				
		for **HBC** types	3	5		MHz
		for **HBF** types	2	5		MHz
C_i	Input capacitance	Any input for **HBC** and **HBF** types		5		pF

PRESET ENABLE

t_{PLH}, t_{PHL}	Propagation delay time	Q outputs			
		$V_{DD} = 5V$			
		for **HBC** types	325	650	ns
		for **HBF** types	325	1300	ns
		$V_{DD} = 10V$			
		for **HBC** types	115	230	ns
		for **HBF** types	115	460	ns
		Carry output			
		$V_{DD} = 5V$			
		for **HBC** types	425	850	ns
		for **HBF** types	425	1700	ns
		$V_{DD} = 10V$			
		for **HBC** types	150	300	ns
		for **HBF** types	150	600	ns
t_{pwH}	Pulse width	$V_{DD} = 5V$			
		for **HBC** types	115	330	ns
		for **HBF** types	115	660	ns
		$V_{DD} = 10V$			
		for **HBC** types	80	160	ns
		for **HBF** types	80	320	ns
t_{rem}	Removal time	$V_{DD} = 5V$			
		for **HBC** types	325	650	ns
		for **HBF** types	325	1300	ns
		$V_{DD} = 10V$			
		for **HBC** types	115	230	ns
		for **HBF** types	115	460	ns

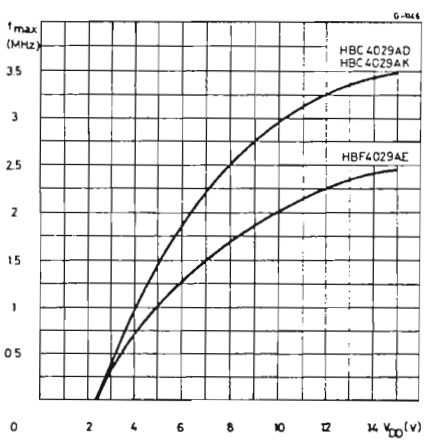
DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
CARRY INPUT					
t_{PLH}, t_{PHL} Propagation delay time	Carry output $V_{DD} = 5V$				
	for **HBC** types		175	350	ns
	for **HBF** types		175	700	ns
	$V_{DD} = 10V$				
	for **HBC** types		50	100	ns
	for **HBF** types		50	200	ns

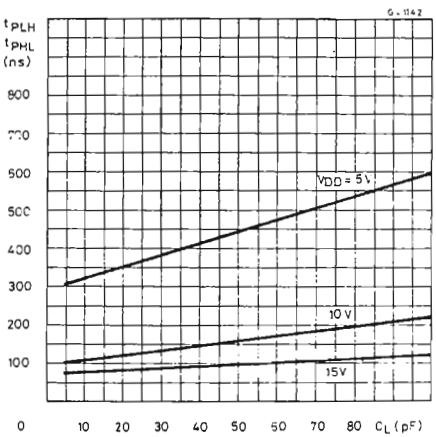
* If more than one unit is cascaded in the parallel clocked application, $t_{\phi r}$ should be made less than or equal to the sum of the fixed propagation delay at 15 pF and the transition time of the carry output driving stage for the estimated capacitive load

** From Up/Down, Binary/Decade or Carry Input Control inputs to Clock input

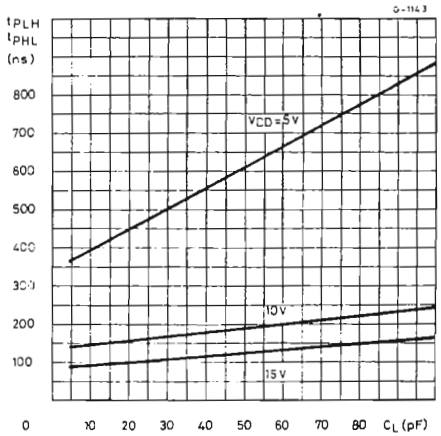
Maximum clock frequency vs. V_{DD}



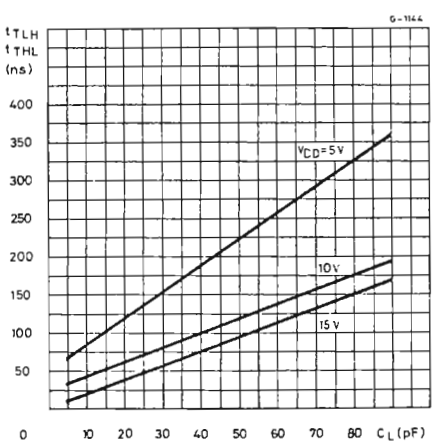
Typical propagation delay time vs. C_L (Q outputs)



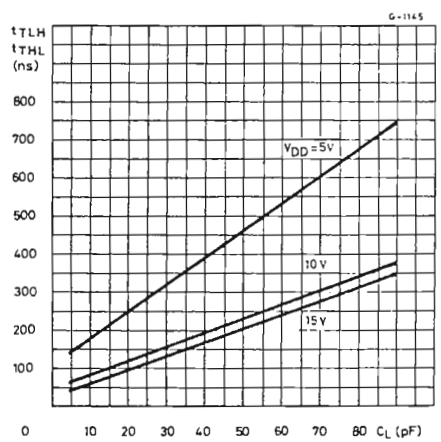
Typical propagation delay time vs. C_L (carry output)



Typical transition time vs. C_L (Q outputs)



Typical transition time vs. C_L (carry output)

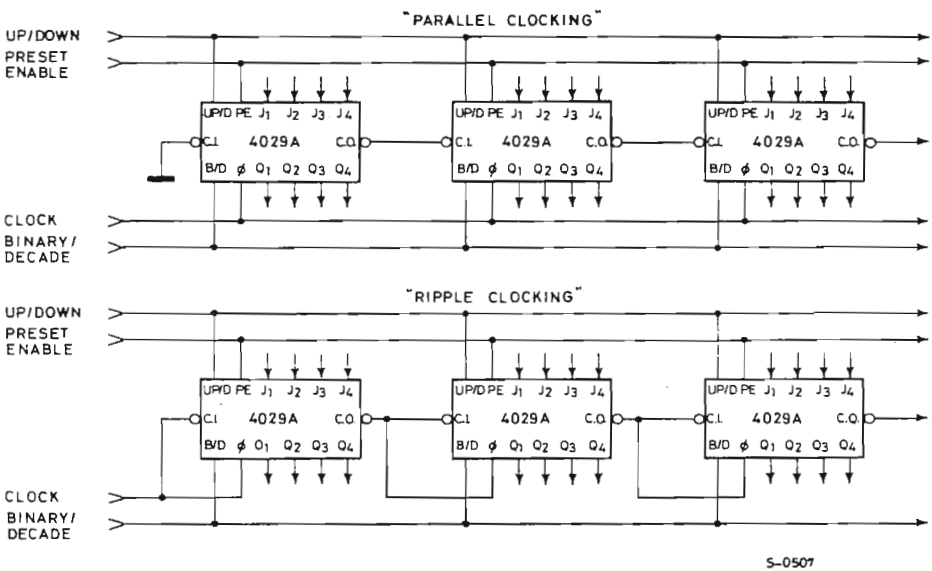


APPLICATIONS

Cascading counter system

Multiple packages can be connected in either a parallel-clocking or a ripple-clocking arrangement. Parallel clocking provides synchronous control and hence faster response from all counting outputs. Ripple-clocking allows for longer clock input rise and fall times.

Cascading counter packages

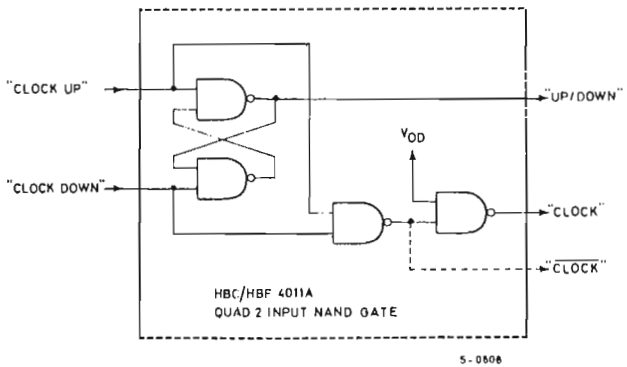


Conversion of "CLOCK UP", "CLOCK DOWN" input signals to "CLOCK" and "UP/DOWN" input signals.

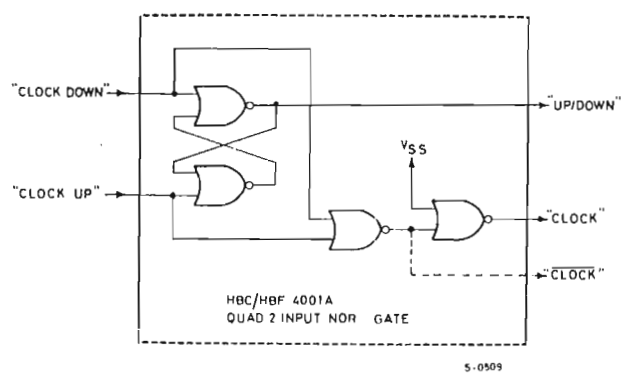
The **HBC/HBF4029A** "Clock" and "Up/Down" inputs are used directly in most applications. In applications where "Clock Up" and "Clock Down" inputs are provided, conversion to the **HBC/HBF 4029A** "Clock" and "Up/Down" inputs can easily be realized by use of the circuits shown below.

APPLICATIONS (continued)

Conversion of "Clock Up", "Clock Down" input signals (must be maintained high) to "Clock" and "Up/Down" input signals



Conversion of "Clock Up", "Clock Down" input signals (must be maintained low) to "Clock" and "Up/Down" input signals



COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

QUAD EXCLUSIVE - OR GATE

- LOW QUIESCENT POWER DISSIPATION
- WIDE SUPPLY VOLTAGE
- HIGH NOISE IMMUNITY: 45% of V_{DD} (TYP.)
- MEDIUM SPEED OPERATION: $t_{PHL} = t_{PLH} = 40$ ns (TYP.) $C_L = 15$ pF
- LOW OUTPUT IMPEDANCE: 500Ω (TYP.) at $V_{DD} - V_{SS} = 10V$
- INPUT FULLY PROTECTED

The **HBC 4030 A** (extended temperature range) and **HBF 4030 A** (standard temperature range) are monolithic integrated circuits, available in 14-lead dual in-line plastic or ceramic package and ceramic flat package.
HBC/HBF 4030 A types each contains four independent Exclusive - OR gate integrated on a single monolithic silicon chip.
Each Exclusive - OR gate consist of four N-channel and four P-channel enhancement - type transistors.
All inputs and outputs are protected against electrostatic effects.

ABSOLUTE MAXIMUM RATINGS

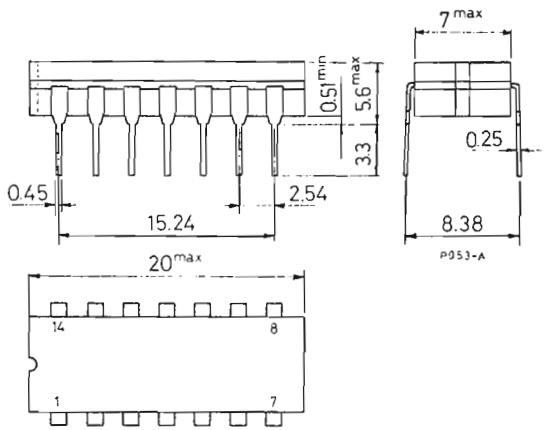
$V_{DD}-V_{SS}$	Supply voltage	-0.5 to 15 V
V_I	Input voltage (at any pin)	$V_{SS} \leqslant V_I \leqslant V_{DD}$
P_{tot}	Total power dissipation (per package)	200 mW
T_{stg}	Storage temperature	-65 to 150 °C
T_{op}	Operating temperature : for **HBC** types	-55 to 125 °C
	for **HBF** types	-40 to 85 °C

ORDERING NUMBERS :

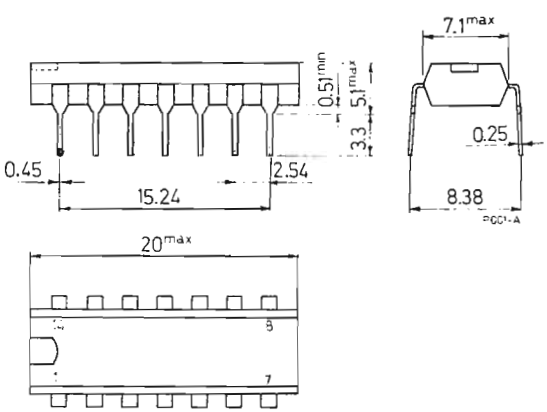
HBC 4030 AD	for dual in-line ceramic package
HBC 4030AF	for dual in-line ceramic package, frit seal (extended temperature range)
HBC 4030AK	for ceramic flat package
HBF 4030AE	for dual in-line plastic package
HBF 4030AF	for dual in-line ceramic package, frit seal (standard temperature range)

MECHANICAL DATA (dimensions in mm)

Dual in-line ceramic package
for HBC 4030 AD and
HBC/HBF 4030 AF

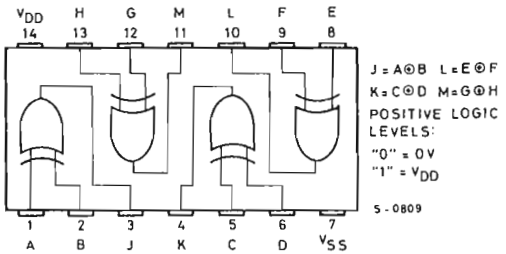


Dual in-line plastic package
for HBF 4030 AE

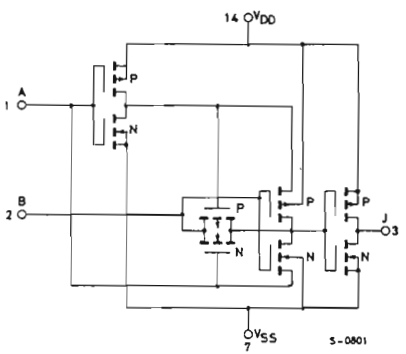


Ceramic flat package for HBC 4030 AK

CONNECTION DIAGRAM



SCHEMATIC DIAGRAM and TRUTH TABLE



ALL P-CHANNEL SUBSTRATES ARE INTERNALLY CONNECTED TO V_{DD}
ALL N-CHANNEL SUBSTRATES ARE INTERNALLY CONNECTED TO V_{SS}

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

Where "1" = High level
"0" = Low level

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage	3 to 15 V
V_I*	Input voltage	V_{DD} to V_{SS}
T_{op}	Operating temperature: for **HBC** types	-55 to 125 °C
	for **HBF** types	-40 to 85 °C

* This is measured with respect to the V_{SS} pin voltage

STATIC ELECTRICAL CHARACTERISTICS

Parameter		Test conditions	Min.	Typ.	Max.	Unit
HBC types (extended temperature range)						
I_L	Quiescent current	V_{DD} = 5V				
		at T_{amb}=-55°C			0.5	μA
		at T_{amb}= 25°C		0.005	0.5	μA
		at T_{amb}=125°C			30	μA
		V_{DD} = 10V				
		at T_{amb}=-55°C			1	μA
		at T_{amb}= 25°C		0.01	1	μA
		at T_{amb}=125°C			60	μA
V_{OH}	Output high voltage	I_o = 0				
		V_{DD} = 5V				
		at T_{amb}=-55°C	4.99			V
		at T_{amb}= 25°C	4.99	5		V
		at T_{amb}=125°C	4.95			V
		V_{DD}= 10V				
		at T_{amb}=-55°C	9.99			V
		at T_{amb}= 25°C	9.99	10		V
		at T_{amb}=125°C	9.95			V
V_{OL}	Output low voltage	I_o = 0				
		V_{DD} = 5V or 10V				
		at T_{amb}=-55°C			0.01	V
		at T_{amb}= 25°C		0	0.01	V
		at T_{amb}=125°C			0.05	V
V_{NH}	Noise immunity	V_{DD} = 5V				
		at T_{amb}=-55°C	1.4			V
		at T_{amb}= 25°C	1.5	2.25		V
		at T_{amb}=125°C	1.5			V
		V_{DD} = 10V				
		at T_{amb}=-55°C	2.9			V
		at T_{amb}= 25°C	3	4.5		V
		at T_{amb}=125°C	3			V

STATIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{NL}	Noise immunity	V_{DD} = 5V				
		at T_{amb}=-55°C	1.5			V
		at T_{amb}= 25°C	1.5	2.25		V
		at T_{amb}=125°C	1.4			V
		V_{DD} = 10V				
		at T_{amb}=-55°C	3			V
		at T_{amb}= 25°C	3		4.5	V
		at T_{amb}=125°C	2.9			V
I_DN	Output drive current N-channel	V_{DD} = 5V				
		at T_{amb}=-55°C	0.75			mA
		at T_{amb}= 25°C	0.6		1.2	mA
		at T_{amb}=125°C	0.45			mA
		V_{DD} = 10V				
		at T_{amb}=-55°C	1.5			mA
		at T_{amb}= 25°C	1.2		2.4	mA
		at T_{amb}=125°C	0.9			mA
I_DP	Output drive current P-channel	V_{DD} = 5V				
		at T_{amb}=-55°C	-0.45			mA
		at T_{amb}= 25°C	-0.3		-0.6	mA
		at T_{amb}=125°C	-0.21			mA
		V_{DD} = 10V				
		at T_{amb}=-55°C	-0.95			mA
		at T_{amb}= 25°C	-0.65		-1.3	mA
		at T_{amb}=125°C	-0.45			mA
I_I	Input current	V_I = 0V or V_i = V_{DD} T_{amb}= 25°C		10		pA

HBF types (standard temperature range)

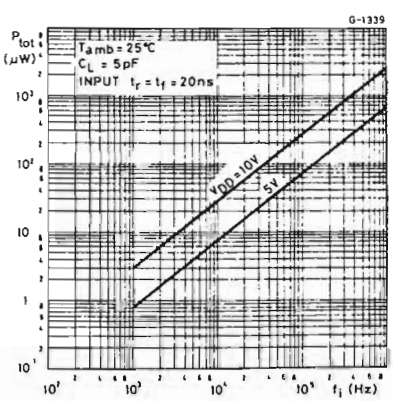
I_L	Quiescent current	V_{DD} = 5V				
		at T_{amb}=-40°C			5	μA
		at T_{amb}= 25°C		0.05	5	μA
		at T_{amb}= 85°C			70	μA

STATIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_L	Quiescent current	V_{DD} = 10V				
		at T_{amb}=-40°C			10	μA
		at T_{amb}= 25°C		0.1	10	μA
		at T_{amb}= 85°C			140	μA
V_{OH}	Output high voltage	I_o = 0				
		V_{DD} = 5V				
		at T_{amb}=-40°C	4.99			V
		at T_{amb}= 25°C	4.99	5		V
		at T_{amb}= 85°C	4.95			V
		V_{DD} = 10V				
		at T_{amb}=-40°C	9.99			V
		at T_{amb}= 25°C	9.99	10		V
		at T_{amb}= 85°C	9.95			V
V_{OL}	Output low voltage	I_o = 0				
		V_{DD}= 5V or 10V				
		at T_{amb}=-40°C			0.01	V
		at T_{amb}= 25°C		0	0.01	V
		at T_{amb}= 85°C			0.05	V
V_{NH}	Noise immunity	V_{DD} = 5V				
		at T_{amb}=-40°C	1.4			V
		at T_{amb}= 25°C	1.5	2.25		V
		at T_{amb}= 85°C	1.5			V
		V_{DD} = 10V				
		at T_{amb}=-40°C	2.9			V
		at T_{amb}= 25°C	3	4.5		V
		at T_{amb}= 85°C	3			V
V_{NL}	Noise immunity	V_{DD} = 5V				
		at T_{amb}=-40°C	1.5			V
		at T_{amb}= 25°C	1.5	2.25		V
		at T_{amb}= 85°C	1.4			V

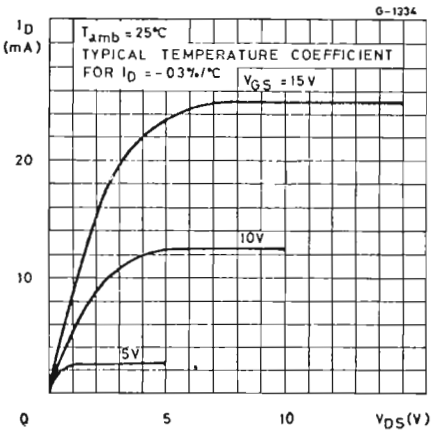
STATIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{NL}	Noise immunity	V_{DD} = 10V				
		at T_{amb}=-40°C	3			V
		at T_{amb}= 25°C	3		4.5	V
		at T_{amb}= 85°C	2.9			V
I_DN	Output drive current N-channel	V_{DD} = 5V				
		at T_{amb}=-40°C	0.35			mA
		at T_{amb}= 25°C	0.3		1.2	mA
		at T_{amb}= 85°C	0.25			mA
		V_{DD} = 10V				
		at T_{amb}=-40°C	0.7			mA
		at T_{amb}= 25°C	0.6		2.4	mA
		at T_{amb}= 85°C	0.5			mA
I_DP	Output drive current P-channel	V_{DD} = 5V				
		at T_{amb}=-40°C	-0.21			mA
		at T_{amb}= 25°C	-0.15		-0.6	mA
		at T_{amb}= 85°C	-0.12			mA
		V_{DD} = 10V				
		at T_{amb}=-40°C	-0.45			mA
		at T_{amb}= 25°C	-0.32		-1.3	mA
		at T_{amb}= 85°C	-0.25			mA
I_i	Input current	V_i = 0V or V_i = V_{DD}				
		T_{amb} = 25°C		10		pA

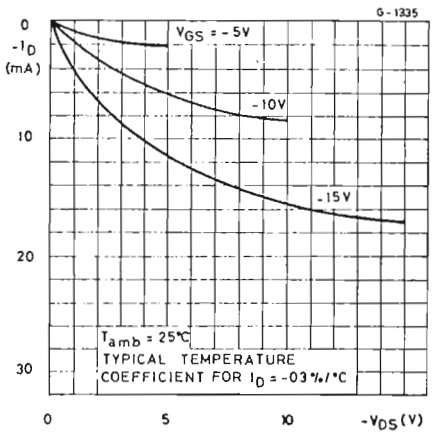


Typical power dissipation characteristics (per gate)

Typical N-channel drain characteristics

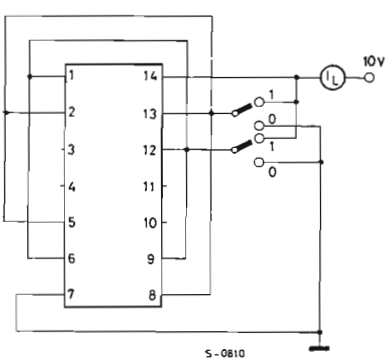


Typical P-channel drain characteristics

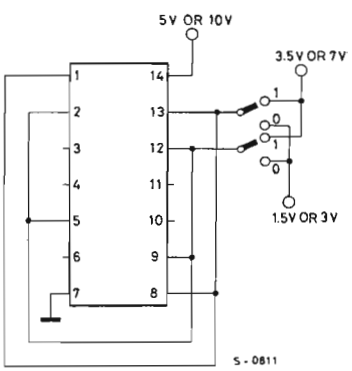


TEST CIRCUITS

Quiescent device current

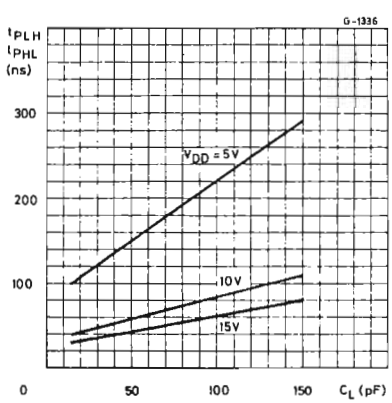


Noise immunity



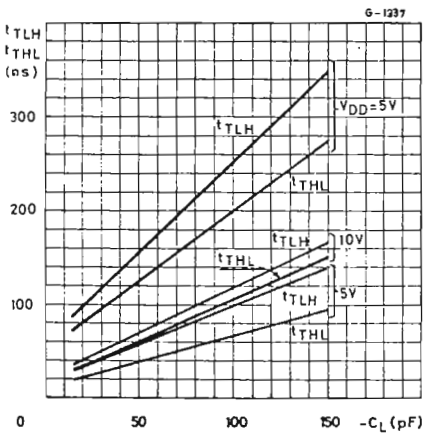
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 15 pF, typical temperature coefficient for all V_{DD} = 0.3%/°C values, all input rise and fall time = 20 ns)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
t_{PLH}, t_{PHL}	Propagation delay time	V_{DD} = 5V				
		for **HBC** types		100	200	ns
		for **HBF** types		100	300	ns
		V_{DD} = 10V				
		for **HBC** types		40	100	ns
		for **HBF** types		40	150	ns
t_{TLH}	Transition time	V_{DD} = 5V				
		for **HBC** types		80	150	ns
		for **HBF** types		80	300	ns
		V_{DD} = 10V				
		for **HBC** types		30	75	ns
		for **HBF** types		30	150	ns
t_{THL}	Transition time	V_{DD} = 5V				
		for **HBC** types		70	150	ns
		for **HBF** types		70	300	ns
		V_{DD} = 10V				
		for **HBC** types		25	75	ns
		for **HBF** types		25	150	ns
C_i	Input capacitance	V_i = 0V or V_i = V_{DD} for **HBC** and **HBF** types		5		pF

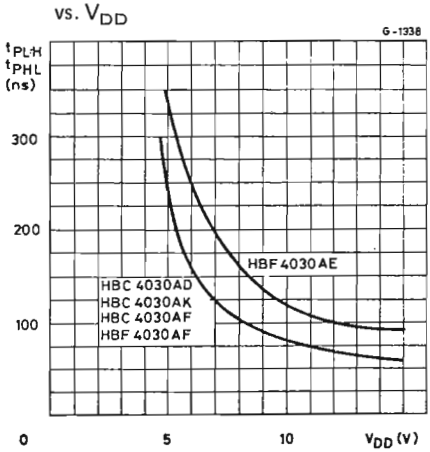


Typical propagation delay time vs. C_L

Typical transition time vs. C_L

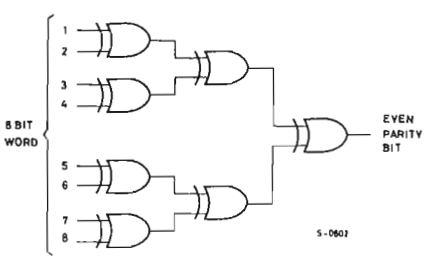


Maximum propagation delay time vs. V_{DD}

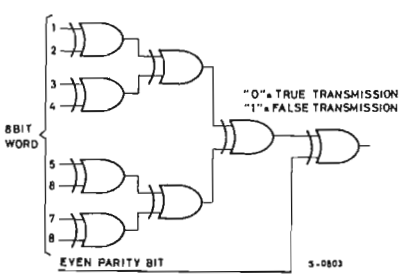


TYPICAL APPLICATIONS

Even-parity-bit generator
(1-3/4 x **HBC/HBF 4030A**)

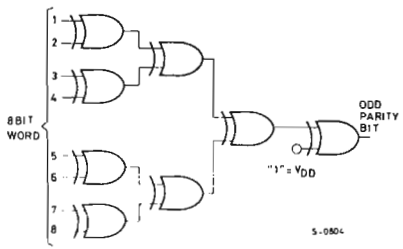


Even-parity checker
(2 x **HBC/HBF 4030A**)

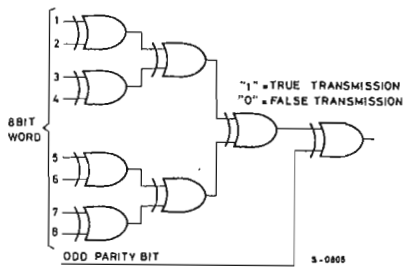


TYPICAL APPLICATIONS (continued)

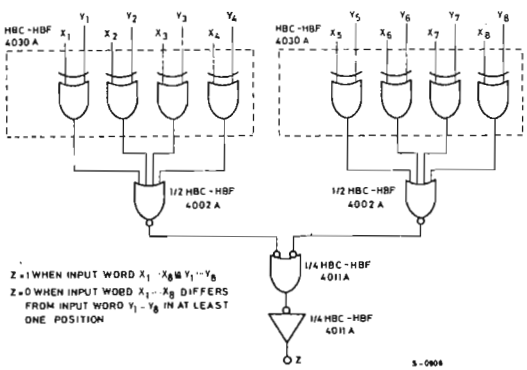
Odd-parity-bit generator
(2 x **HBC/HBF 4030A**)



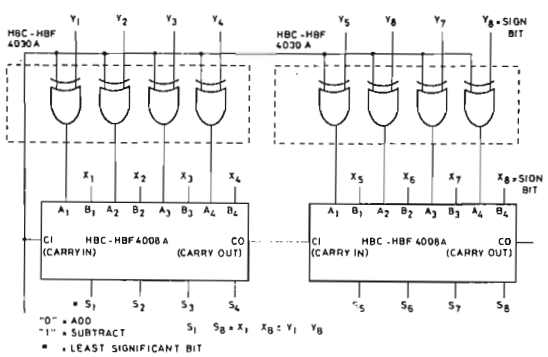
Odd-parity checker
(2 x **HBC/HBF 4030A**)



8-bit comparator



8-bit two's complement
adder-substractor



TYPICAL APPLICATIONS (continued)

TABLE 1

Two's complement numbers and their equivalent decimal values

X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1			X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1		
0	0	0	0	0	0	0	0	=	0	1	1	1	1	1	1	1	1	=	-1
0	0	0	0	0	0	0	1	=	1	1	1	1	1	1	1	1	0	=	-2
0	0	0	0	0	0	1	0	=	2	1	1	1	1	1	1	0	1	=	-3
0	0	0	0	0	0	1	1	=	3	1	1	1	1	1	1	0	0	=	-4
										1	1	1	1	1	0	1	1	=	-5
0	1	1	1	1	1	1	0	=	126	1	0	0	0	0	0	0	1	=	-127
0	1	1	1	1	1	1	1	=	127	1	0	0	0	0	0	0	0	=	-128

The two's complement adder-substractor can add or substract any two of the numbers in TABLE 1. For example

a)

		SIGN BIT									
2		X	0	0	0	0	0	1	0	2	+
+	=										
-5		Y	1	1	1	1	1	0	1	-5	+
		CI							0	+	+
		S 0	1	1	1	1	1	1	0	1	= -3
		CO									

b)

		SIGN BIT									
-2		X	1	1	1	1	1	1	1	0	-2 +
-	=										
-5		Y	1	1	1	1	1	0	1	1	-5
		$\overline{Y}$	0	0	0	0	0	1	0	0	+
		CI								1	+
		S 1	0	0	0	0	0	0	1	1	= 3
		CO									

COS/MOS INTEGRATED CIRCUIT

4 - STAGE PARALLEL IN/PARALLEL OUT SHIFT REGISTER

- LOW QUIESCENT POWER DISSIPATION
- WIDE SUPPLY VOLTAGE RANGE : 3 to 15V
- HIGH NOISE IMMUNITY : 45% of V_{DD} (TYP.)
- HIGH SPEED OPERATION : up to 5 MHz
- INPUTS FULLY PROTECTED
- SYNCHRONOUS PARALLEL ENTRY on ALL 4 STAGES
- HIGH FANOUT
- STATIC FLIP-FLOP OPERATION; MASTER-SLAVE CONFIGURATION
- RESET CONTROL
- BUFFERED OUTPUTS

The **HBC4035A** (extended temperature range) and **HBF 4035A** (standard temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package. Four stage clocked serial registers with provision for synchronous parallel inputs to each stage and serial inputs to the first stage via J-$\overline{K}$ logic, are integrated. With J-$\overline{K}$ inputs connected together, the first stage becomes a "D" type flip-flop.

ABSOLUTE MAXIMUM RATINGS

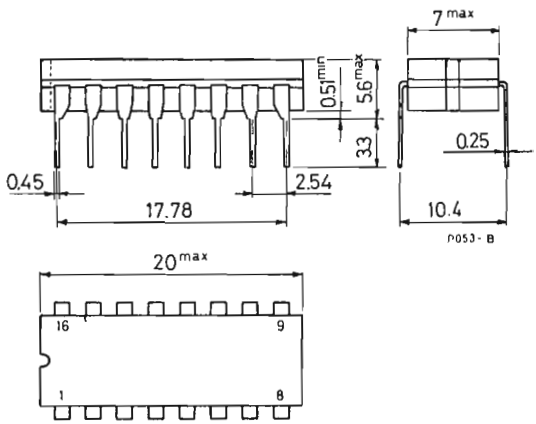
V_{DD}-V_{SS}	Supply voltage	-0.5 to 15	V
V_i	Input voltage (at any pin)	$V_{SS} \leqslant V_i \leqslant V_{DD}$	
P_{tot}	Total power dissipation (per package)	200	mW
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature: for **HBC** types	-55 to 125	°C
	for **HBF** types	-40 to 85	°C

ORDERING NUMBERS :

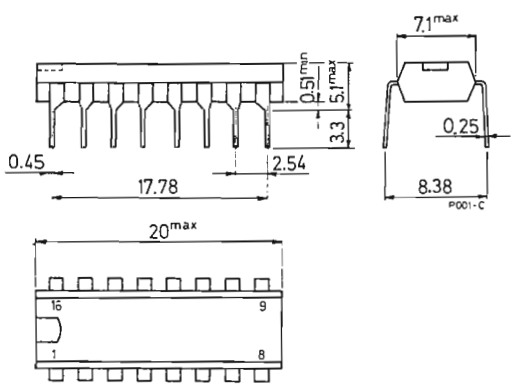
HBC 4035 **AD** for dual in-line ceramic package
HBC 4035 **AF** for dual in-line ceramic package frit seal (extended temperature range)
HBC 4035 **AK** for ceramic flat package
HBF 4035 **AE** for dual in-line plastic package
HBF 4035 **AF** for dual in-line ceramic package frit seal (standard temperature range)

MECHANICAL DATA (dimensions in mm)

Dual in-line ceramic package
for HBC 4035 AD and
HBC/HBF 4035 AF



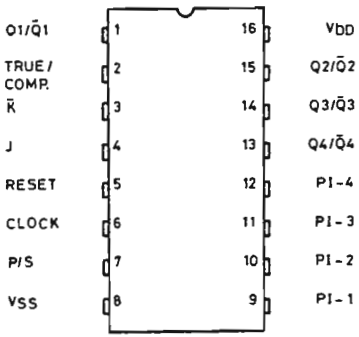
Dual in-line plastic package
for HBF 4035 AE



Ceramic flat package for HBC 4035 AK

CONNECTION DIAGRAM and OPERATING MODE TRUTH TABLE

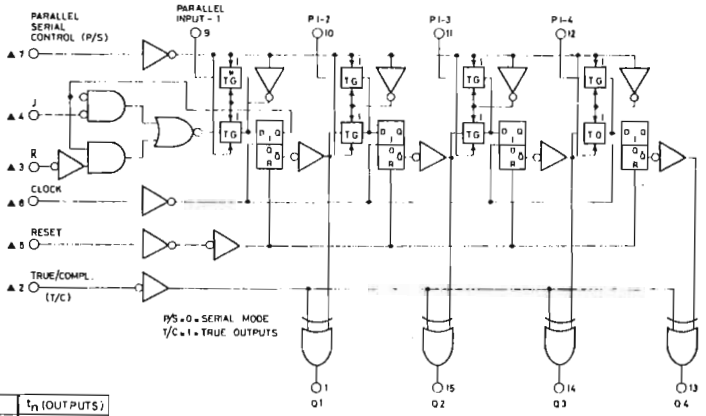
(top view)



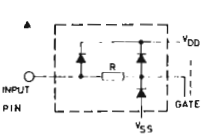
5-0535

CONTROL INPUTS	LOGIC LEVEL	DEVICE PLACEMENT
PARALLEL/SERIAL (P/S)	1	PARALLEL MODE
	0	SERIAL MODE
TRUE/COMPLEMENT (T/C)	1	TRUE OUTPUTS
	0	COMPLEMENT OUTPUTS
RESET	1	OUTPUT LOW
CLOCK (ϕ)	⎍	INFORMATION REMOVAL

LOGIC BLOCK DIAGRAM and FIRST STAGE TRUTH TABLE



CLOCK (ϕ)	t_{n-1} (INPUTS) J	K̄	R	Q_{n-1}	t_n (OUTPUTS) Q_n
⎍	0	X	0	0	0
⎍	1	X	0	0	1
⎍	X	0	0	1	0
⎍	1	Q	0	Q_{n-1}	$\overline{Q_{n-1}}$ TOGGLE MODE
⎍	X	1	0	1	1
⎎	X	X	0	Q_{n-1}	Q_{n-1}
X	X	X	1	X	0



5-0540/3 INPUT PROTECTION CIRCUIT

PIN 16 = V_{DD}
PIN 8 = GND

* TG = TRANSMISSION GATE

INPUT TO OUTPUT IS

a) A BIDIRECTIONAL LOW IMPEDANCE WHEN CONTROL INPUT 1 IS "LOW" AND CONTROL INPUT 2 IS "HIGH"

b) AN OPEN CIRCUIT WHEN CONTROL INPUT 1 IS "HIGH" AND CONTROL INPUT 2 IS "LOW"

RECOMMENDED OPERATING CONDITIONS

V_{DD} *	Supply voltage	3 to 15	V
V_i *	Input voltage	V_{DD} to V_{SS}	
T_{op}	Operating temperature : for **HBC** types	-55 to 125	°C
	for **HBF** types	-40 to 85	°C

* This is measured with respect to the V_{SS} pin voltage

STATIC ELECTRICAL CHARACTERISTICS

Parameter	Test conditions	Min.	Typ.	Max.	Unit
HBC types (extended temperature range)					
I_L Quiescent current	V_{DD} = 5V				
	at T_{amb} = -55°C			5	μA
	at T_{amb} = 25°C		0.3	5	μA
	at T_{amb} = 125°C			300	μA
	V_{DD} = 10V				
	at T_{amb} = -55°C			10	μA
	at T_{amb} = 25°C		0.5	10	μA
	at T_{amb} = 125°C			600	μA
V_{OH} Output high voltage	I_o = 0				
	V_{DD} = 5V				
	at T_{amb} = -55°C	4.99			V
	at T_{amb} = 25°C	4.99	5		V
	at T_{amb} = 125°C	4.95			V
	V_{DD} = 10V				
	at T_{amb} = -55°C	9.99			V
	at T_{amb} = 25°C	9.99	10		V
	at T_{amb} = 125°C	9.95			V
V_{OL} Output low voltage	I_o = 0				
	V_{DD} = 5V or 10V				
	at T_{amb} = -55°C			0.01	V
	at T_{amb} = 25°C		0	0.01	V
	at T_{amb} = 125°C			0.05	V

STATIC ELECTRICAL CHARACTERISTICS (continued)

	Parameter		Test conditions	Min.	Typ.	Max.	Unit
→	V_{NH}	Noise immunity	V_{DD} = 5V V_o = 4.2V				
			at T_{amb} = -55°C	1.4			V
			at T_{amb} = 25°C	1.5	2.25		V
			at T_{amb} = 125°C	1.5			V
			V_{DD} = 10V V_o = 9V				
			at T_{amb} = -55°C	2.9			V
			at T_{amb} = 25°C	3	4.5		V
			at T_{amb} = 125°C	3			V
→	V_{NL}	Noise immunity	V_{DD} = 5V V_o = 0.8V				
			at T_{amb} = -55°C	1.5			V
			at T_{amb} = 25°C	1.5	2.25		V
			at T_{amb} = 125°C	1.4			V
			V_{DD} = 10V V_o = 1V				
			at T_{amb} = -55°C	3			V
			at T_{amb} = 25°C	3	4.5		V
			at T_{amb} = 125°C	2.9			V
	I_DN	Output drive current N-channel	V_{DD} = 5V V_o = 0.5V				
			at T_{amb} = -55°C	0.62			mA
			at T_{amb} = 25°C	0.50	1		mA
			at T_{amb} = 125°C	0.35			mA
			V_{DD} = 10V V_o = 0.5V				
			at T_{amb} = -55°C	1.55			mA
			at T_{amb} = 25°C	1.25	2.5		mA
			at T_{amb} = 125°C	0.87			mA
	I_DP	Output drive current P-channel	V_{DD} = 5V V_o = 4.5V				
			at T_{amb} = -55°C	-0.31			mA
			at T_{amb} = 25°C	-0.25	-0.5		mA
			at T_{amb} = 125°C	-0.17			mA
			V_{DD} = 10V V_o = 9.5V				
			at T_{amb} = -55°C	-0.81			mA
			at T_{amb} = 25°C	-0.65	-1.3		mA
			at T_{amb} = 125°C	-0.45			mA

STATIC ELECTRICAL CHARACTERISTICS (continued)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_i	Input current	$T_{amb} = 25°C$		10		pA

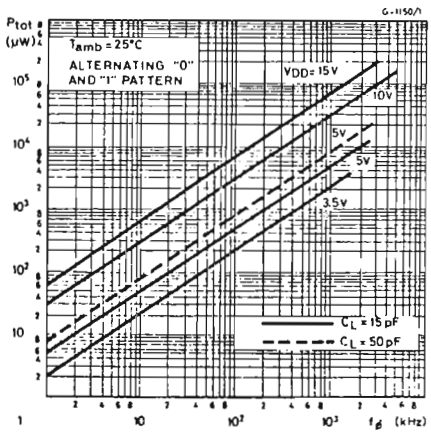
HBF types (standard temperature range)

I_L	Quiescent current	$V_{DD} = 5V$				
		at $T_{amb} = -40°C$			50	μA
		at $T_{amb} = 25°C$		0.5	50	μA
		at $T_{amb} = 85°C$			700	μA
		$V_{DD} = 10V$				
		at $T_{amb} = -40°C$			100	μA
		at $T_{amb} = 25°C$		1	100	μA
		at $T_{amb} = 85°C$			1400	μA
V_{OH}	Output high voltage	$I_o = 0$				
		$V_{DD} = 5V$				
		at $T_{amb} = -40°C$	4.99			V
		at $T_{amb} = 25°C$	4.99	5		V
		at $T_{amb} = 85°C$	4.95			V
		$V_{DD} = 10V$				
		at $T_{amb} = -40°C$	9.99			V
		at $T_{amb} = 25°C$	9.99	10		V
		at $T_{amb} = 85°C$	9.95			V
V_{OL}	Output low voltage	$I_o = 0$				
		$V_{DD} = 5V$ or $10V$				
		at $T_{amb} = -40°C$			0.01	V
		at $T_{amb} = 25°C$		0	0.01	V
		at $T_{amb} = 85°C$			0.05	V
→ V_{NH}	Noise immunity	$V_{DD} = 5V$ $V_o = 4.2V$				
		at $T_{amb} = -40°C$	1.4			V
		at $T_{amb} = 25°C$	1.5	2.25		V
		at $T_{amb} = 85°C$	1.5			V
		$V_{DD} = 10V$ $V_o = 9V$				
		at $T_{amb} = -40°C$	2.9			V
		at $T_{amb} = 25°C$	3	4.5		V
		at $T_{amb} = 85°C$	3			V
→ V_{NL}	Noise immunity	$V_{DD} = 5V$ $V_o = 0.6V$				
		at $T_{amb} = -40°C$	1.5			V
		at $T_{amb} = 25°C$	1.5	2.25		V
		at $T_{amb} = 85°C$	1.4			V

STATIC ELECTRICAL CHARACTERISTICS (continued)

	Parameter		Test conditions	Min.	Typ.	Max.	Unit
→	V_{NL}	Noise immunity	V_{DD} = 10V V_o = 1V				
			at T_{amb} = -40°C	3			V
			at T_{amb} = 25°C	3		4.5	V
			at T_{amb} = 85°C	2.9			V
	I_DN	Output drive current N-channel	V_{DD} = 5V V_o = 0.5V				
			at T_{amb} = -40°C	0.43			mA
			at T_{amb} = 25°C	0.35		1	mA
			at T_{amb} = 85°C	0.24			mA
			V_{DD} = 10V V_o = 0.5V				
			at T_{amb} = -40°C	1.05			mA
			at T_{amb} = 25°C	0.85		2.5	mA
			at T_{amb} = 85°C	0.59			mA
	I_DP	Output drive current P-channel	V_{DD} = 5V V_o = 4.5V				
			at T_{amb} = -40°C	-0.2			mA
			at T_{amb} = 25°C	-0.18		-0.5	mA
			at T_{amb} = 85°C	-0.12			mA
			V_{DD} =10V V_o = 9.5V				
			at T_{amb} = -40°C	-0.56			mA
			at T_{amb} = 25°C	-0.45		-0.31	mA
			at T_{amb} = 85°C	-0.31			mA
	I_i	Input current	T_{amb} = 25°C		10		pA

Typical power dissipation characteristics



DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 15pF, typical temperature coefficient for all V_{DD} = 0.3%/°C values)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
CLOCKED OPERATION					
t_{PLH}, t_{PHL} Propagation delay time	V_{DD} = 5V				
	for **HBC** types		250	500	ns
	for **HBF** types		250	700	ns
	V_{DD} = 10V				
	for **HBC** types		100	200	ns
	for **HBF** types		100	300	ns
t_{TLH}, t_{THL} Transition time	V_{DD} = 5V				
	for **HBC** types		100	200	ns
	for **HBF** types		100	300	ns
	V_{DD} = 10V				
	for **HBC** types		50	100	ns
	for **HBF** types		50	150	ns
t_{pwH}, t_{pwL} Minimum clock pulse width	V_{DD} = 5V				
	for **HBC** types		200	335	ns
	for **HBF** types		200	500	ns
	V_{DD} = 10V				
	for **HBC** types		100	165	ns
	for **HBF** types		100	250	ns
$t_{\phi r}$, $t_{\phi f}$ Clock rise and fall time	V_{DD} = 5V				
	for **HBC** types			15	μs
	for **HBF** types			15	μs
	V_{DD} = 10V				
	for **HBC** types			5	μs
	for **HBF** types			5	μs
t_s Set - up time (J/$\overline{K}$ lines)	V_{DD} = 5V				
	for **HBC** types		250	500	ns
	for **HBF** types		250	750	ns
	V_{DD} = 10V				
	for **HBC** types		100	200	ns
	for **HBF** types		100	250	ns

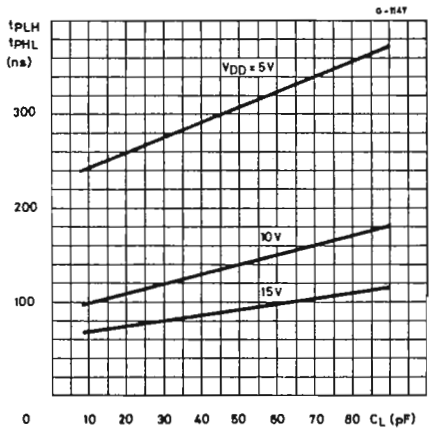
DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
t_s	Set-up time (parallel -in-lines)	V_{DD} = 5V				
		for **HBC** types		100	350	ns
		for **HBF** types		100	500	ns
		V_{DD} = 10V				
		for **HBC** types		50	80	ns
		for **HBF** types		50	100	ns
f_{max}	Maximum clock frequency	V_{DD} = 5V				
		for **HBC** types	1.5	2.5		MHz
		for **HBF** types	1	2.5		MHz
		V_{DD} = 10V				
		for **HBC** types	3	5		MHz
		for **HBF** types	2	5		MHz
C_I	Input capacitance	Any input for **HBC** and **HBF** types		5		pF

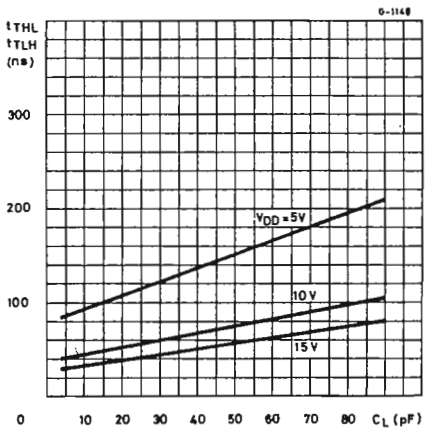
RESET OPERATION

t_{PLH}, t_{PHL}	Propagation delay time	V_{DD} = 5V				
		for **HBC** types		250	500	ns
		for **HBF** types		250	700	ns
		V_{DD} = 10V				
		for **HBC** types		100	200	ns
		for **HBF** types		100	300	ns
t_{pwH}, t_{pwL}	Minimum reset pulse width	V_{DD} = 5V				
		for **HBC** types		200	400	ns
		for **HBF** types		200	500	ns
		V_{DD} = 10V				
		for **HBC** types		100	175	ns
		for **HBF** types		100	200	ns

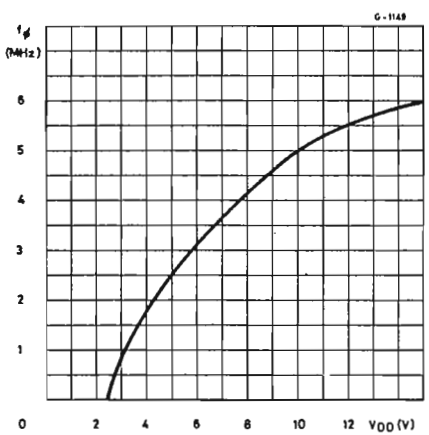
Typical propagation delay time vs. C_L



Typical transition time vs. C_L

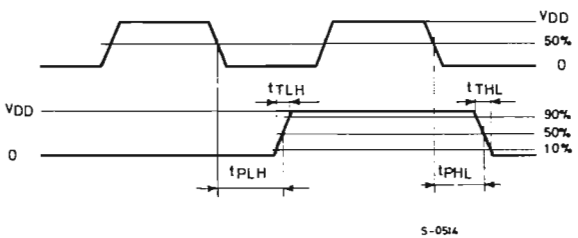


Typical clock input frequency vs. V_{DD}



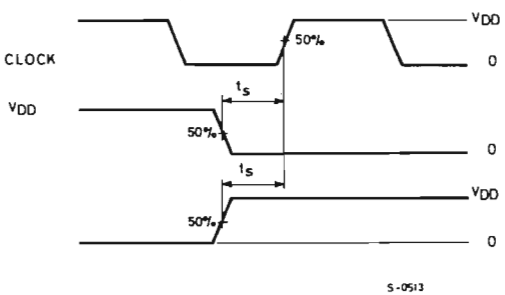
WAVEFORMS

Transition times and propagation delay times



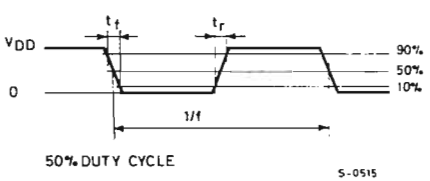
S-0514

Set-up times



S-0513

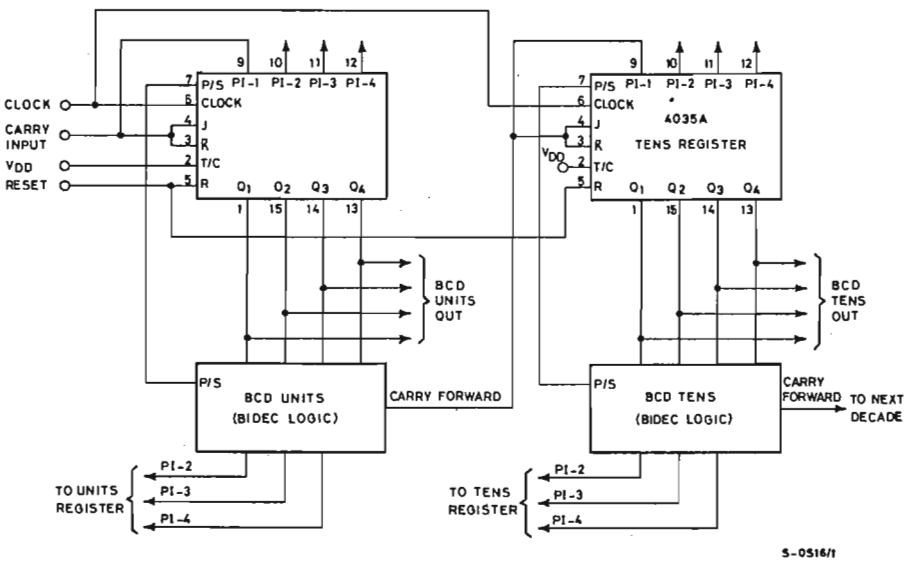
Clock pulse rise and fall times



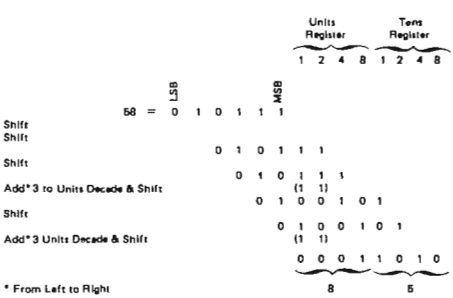
S-0515

TYPICAL APPLICATIONS

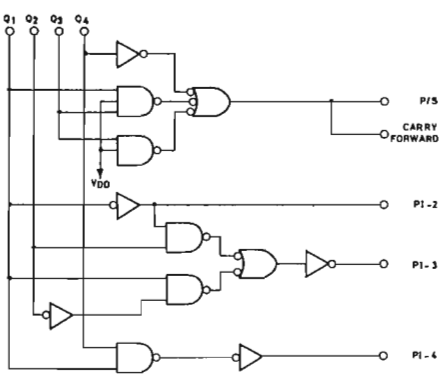
Binary-to-BCD converter



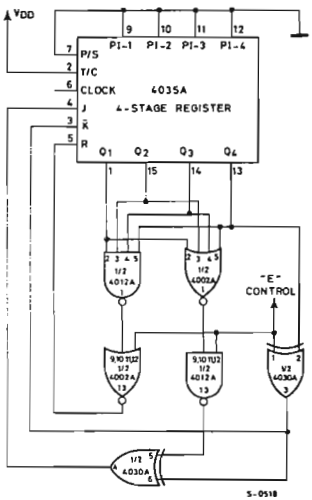
Example of binary-to-BCD conversion



BIDEC logic



Double sequence generator

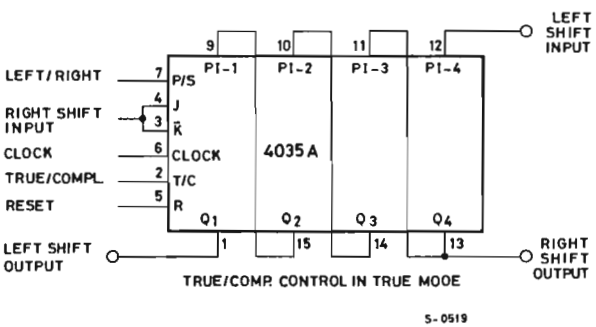


State sequences

Using a control line (E) two different state sequences can be generated. For example, suppose the following two sequences are desired on command (control line E)

Control = E =	0					1				
	Q_1 A	Q_2 B	Q_3 C	Q_4 D			Q_1 A	Q_2 B	Q_3 C	Q_4 D
0	0	0	0	0		15	1	1	1	1
1	1	0	0	0		14	0	1	1	1
2	0	1	0	0		13	1	0	1	1
5	1	0	1	0		10	0	1	0	1
10	0	1	0	1		5	1	0	1	0
4	0	0	1	0		11	1	1	0	1
9	1	0	0	1		6	0	1	1	0
3	1	1	0	0		12	0	0	1	1
6	0	1	1	0		9	1	0	0	1
13	1	0	1	1		2	0	1	0	0
11	1	1	0	1		4	0	0	1	0
7	1	1	1	0		8	0	0	0	1
14	0	1	1	1		1	1	0	0	0
12	0	0	1	1		3	1	1	0	0
8	0	0	0	1		7	1	1	1	0

Shift left/shift right register



COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

21 - STAGE COUNTER

- LOW QUIESCENT POWER DISSIPATION
- WIDE SUPPLY VOLTAGE RANGE: 3 to 15V
- HIGH NOISE IMMUNITY: 45% of V_{DD} (TYP.)
- HIGH SPEED OPERATION: 10 MHz (TYP.) at $V_{DD} = 10V$
- INPUTS FULLY PROTECTED
- OUTPUT DRIVERS with SINK or SOURCE CAPABILITY:
  7 mA (TYP.) at $V_o = 0.5V$, $V_{DD} = 5V$ (SINK)
  5 mA (TYP.) at $V_o = 4.5V$, $V_{DD} = 5V$ (SOURCE)
- OUTPUT WAVEFORMS SHAPED for a 3.125% DUTY CYCLE
- 16.5V ZENER DIODE TRANSIENT PROTECTION on CHIP for AUTOMOTIVE USE

The **HBC 4045A** (extended temperature range) and **HBF 4045A** (standard temperature range) are 21 - stage binary counters constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic chip. The device is a timing circuit consisting of 23 flip-flops, two inverter output drivers, three zener diodes providing transient protection at 16.5V, and input inverters for use in a crystal oscillator. The **HBC/HBF 4045A** configuration has 21 flip-flop counting stages and two flip-flops used to shape the output waveform. Push-pull operation is provided by the inverter output drivers. A crystal oscillator circuit can be made less sensitive to voltage supply variations by the use of source resistors. In this device, the sources of the P and N transistors have been brought out to package terminals. If external resistors are not required, the sources must be shorted to their respective substrates (S_P to V_{DD}, S_N to V_{SS} - see logic diagram). The device is available in 16-lead dual in-line plastic or ceramic package and ceramic flat package.

ABSOLUTE MAXIMUM RATINGS

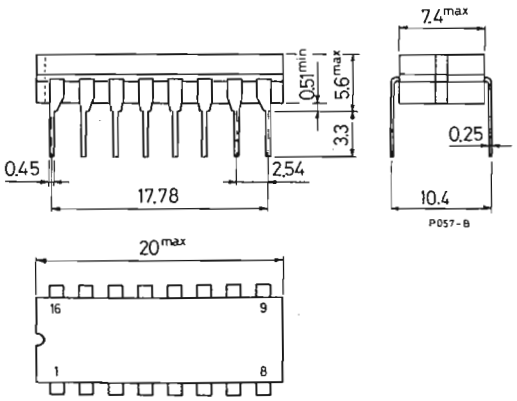
V_{DD}-V_{SS}	Supply voltage	-0.5 to 15	V
V_i	Input voltage (at any pin)	$V_{SS} \leqslant V_i \leqslant V_{DD}$	
P_{tot}	Total power dissipation (per package, including zener diodes)	200	mW
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature: for **HBC** types	-55 to 125	°C
	for **HBF** types	-40 to 85	°C

ORDERING NUMBERS :

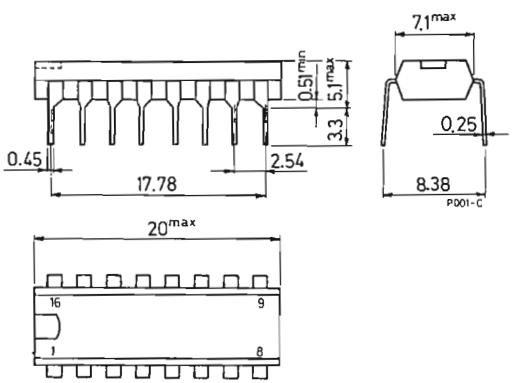
HBC 4045 AD	for dual in-line ceramic package
HBC 4045 AF	for dual in-line ceramic package frit seal, (extended temperature range)
HBC 4045 AK	for ceramic flat package
HBF 4045 AE	for dual in-line plastic package
HBF 4045 AF	for dual in-line ceramic package frit seal, (standard temperature range)

MECHANICAL DATA (dimensions in mm)

Dual in-line ceramic package
for HBC 4045 AD and
HBC/HBF 4045 AF

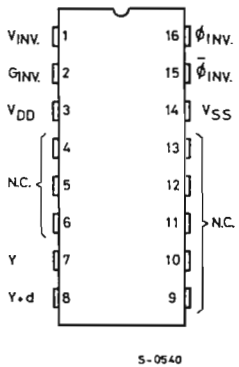


Dual in-line plastic package
for HBF 4045 AE

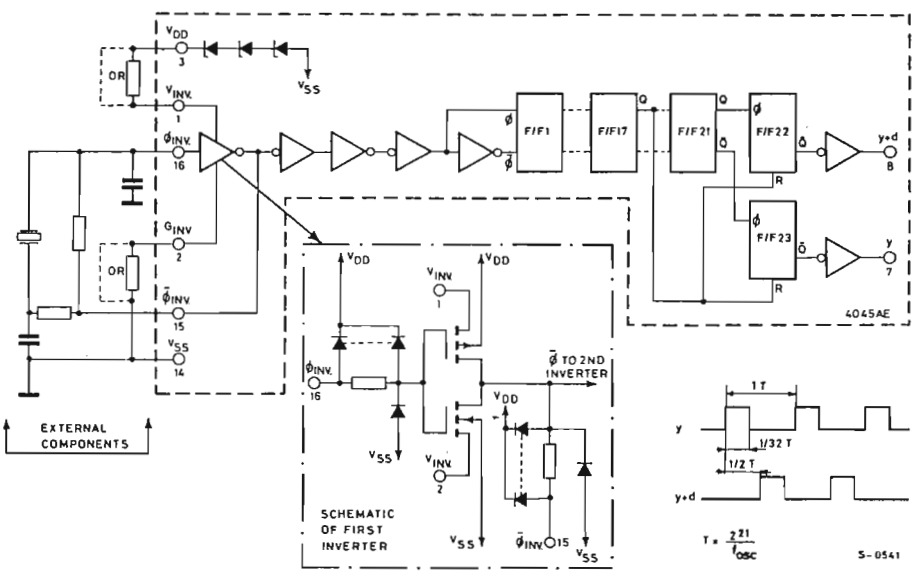


Ceramic flat package for HBC 4045 AK

CONNECTION DIAGRAM (top view)



LOGIC BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage	3 to 15	V
V_i*	Input voltage	V_{DD} to V_{SS}	
T_{op}	Operating temperature: for **HBC** types	-55 to 125	°C
	for **HBF** types	-40 to 85	°C

* This is measured with respect to the V_{SS} pin voltage

STATIC ELECTRICAL CHARACTERISTICS

Parameter	Test conditions	Min.	Typ.	Max.	Unit
HBC types (extended temperature range)					
I_L Quiescent current	V_{DD} = 5V				
	at T_{amb} = -55°C			15	μA
	at T_{amb} = 25°C		0.5	15	μA
	at T_{amb} = 125°C			900	μA
	V_{DD} = 10V				
	at T_{amb} = -55°C			25	μA
	at T_{amb} = 25°C		1	25	μA
	at T_{amb} = 125°C			1500	μA
V_{OH} Output high voltage	I_o = 0				
	V_{DD} = 5V				
	at T_{amb} = -55°C	4.99			V
	at T_{amb} = 25°C	4.99	5		V
	at T_{amb} = 125°C	4.95			V
	V_{DD} = 10V				
	at T_{amb} = -55°C	9.99			V
	at T_{amb} = 25°C	9.99	10		V
	at T_{amb} = 125°C	9.95			V
V_{OL} Output low voltage	I_o = 0				
	V_{DD} = 5V or 10V				
	at T_{amb} = -55°C			0.01	V
	at T_{amb} = 25°C		0	0.01	V
	at T_{amb} = 125°C			0.05	V

STATIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{NH}	Noise immunity	V_{DD} = 5V				
		at T_{amb} = -55°C	1.4			V
		at T_{amb} = 25°C	1.5	2.25		V
		at T_{amb} = 125°C	1.5			V
		V_{DD} = 10V				
		at T_{amb} = -55°C	2.9			V
		at T_{amb} = 25°C	3	4.5		V
		at T_{amb} = 125°C	3			V
V_{NL}	Noise immunity	V_{DD} = 5V				
		at T_{amb} = -55°C	1.5			V
		at T_{amb} = 25°C	1.5	2.25		V
		at T_{amb} = 125°C	1.4			V
		V_{DD} = 10V				
		at T_{amb} = -55°C	3			V
		at T_{amb} = 25°C	3	4.5		V
		at T_{amb} = 125°C	2.9			V
$I_D N$	Output drive current N-channel	V_{DD} = 5V V_o = 0.5V				
		at T_{amb} = -55°C	4.4			mA
		at T_{amb} = 25°C	3.5	7		mA
		at T_{amb} = 125°C	2.5			mA
		V_{DD} = 10V V_o = 0.5V				
		at T_{amb} = -55°C	6.9			mA
		at T_{amb} = 25°C	5.5	11		mA
		at T_{amb} = 125°C	3.9			mA
$I_D P$	Output drive current P-channel	V_{DD} = 5V V_o = 4.5V				
		at T_{amb} = -55°C	-3.1			mA
		at T_{amb} = 25°C	-2.5	-5		mA
		at T_{amb} = 125°C	-1.8			mA
		V_{DD} = 10V V_o = 9.5V				
		at T_{amb} = -55°C	-5.6			mA
		at T_{amb} = 25°C	-4.5	-9		mA
		at T_{amb} = 125°C	-3.2			mA
I_i	Input current	T_{amb} = 25°C		10		pA

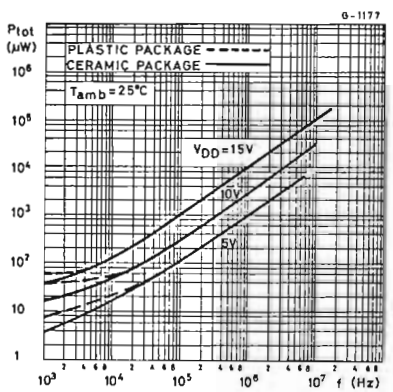
STATIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
HBF types (standard temperature range)						
I_L	Quiescent current	V_{DD} = 5V				
		at T_{amb} = -40°C			50	μA
		at T_{amb} = 25°C		1	50	μA
		at T_{amb} = 85°C			700	μA
		V_{DD} = 10V				
		at T_{amb} = -40°C			100	μA
		at T_{amb} = 25°C		2	100	μA
		at T_{amb} = 85°C			1400	μA
V_{OH}	Output high voltage	I_o = 0				
		V_{DD} = 5V				
		at T_{amb} = -40°C	4.99			V
		at T_{amb} = 25°C	4.99	5		V
		at T_{amb} = 85°C	4.95			V
		V_{DD} = 10V				
		at T_{amb} = -40°C	9.99			V
		at T_{amb} = 25°C	9.99	10		V
		at T_{amb} = 85°C	9.95			V
V_{OL}	Output low voltage	I_o = 0				
		V_{DD} = 5V or 10V				
		at T_{amb} = -40°C			0.01	V
		at T_{amb} = 25°C		0	0.01	V
		at T_{amb} = 85°C			0.05	V
V_{NH}	Noise immunity	V_{DD} = 5V				
		at T_{amb} = -40°C	1.4			V
		at T_{amb} = 25°C	1.5	2.25		V
		at T_{amb} = 85°C	1.5			V
		V_{DD} = 10V				
		at T_{amb} = -40°C	2.9			V
		at T_{amb} = 25°C	3	4.5		V
		at T_{amb} 85°C	3			V
V_{NL}	Noise immunity	V_{DD} = 5V				
		at T_{amb} = -40°C	1.5			V
		at T_{amb} = 25°C	1.5	2.25		V
		at T_{amb} = 85°C	1.4			V

STATIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{NL}	Noise immunity	V_{DD} = 10V				
		at T_{amb} = -40°C	3			V
		at T_{amb} = 25°C	3		4.5	V
		at T_{amb} = 85°C	2.9			V
I_DN	Output drive current N-channel	V_{DD} = 5V V_o = 0.5V				
		at T_{amb} = -40°C	2.2			mA
		at T_{amb} = 25°C	1.8		7	mA
		at T_{amb} = 85°C	1.3			mA
		V_{DD} = 10V V_o = 0.5V				
		at T_{amb} = -40°C	3.5			mA
		at T_{amb} = 25°C	2.8		11	mA
		at T_{amb} = 85°C	2			mA
I_DP	Output drive current P-channel	V_{DD} = 5V V_o = 4.5V				
		at T_{amb} = -40°C	-1.6			mA
		at T_{amb} = 25°C	-1.3		-5	mA
		at T_{amb} = 85°C	-0.9			mA
		V_{DD} = 10V V_o = 9.5V				
		at T_{amb} = -40°C	-2.8			mA
		at T_{amb} = 25°C	-2.3		-9	mA
		at T_{amb} = 85°C	-1.6			mA
I_I	Input current	T_{amb} = 25°C		10		pA

Typical power dissipation characteristics



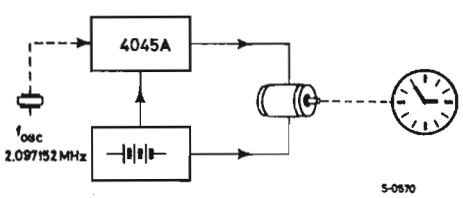
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 15 pF, typical coefficient temperature for all values of V_{DD} = 0.3%/°C, input t_r and t_f = 20 ns except $t_{\phi r}$ and $t_{\phi f}$)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
$t_{\phi r}$, $t_{\phi f}$	Clock rise and fall time	V_{DD} = 10V for **HBC** and **HBF** types			15	μs
f_{max}	Maximum clock frequency	V_{DD} = 5V for **HBC** and **HBF** types	DC		5	MHz
		V_{DD} = 10V for **HBC** and **HBF** types	DC		10	MHz
C_I	Input capacitance	Any input for **HBC** and **HBF** types			5	pF

TYPICAL APPLICATIONS

Digital equipment in which ultra-low dissipation and/or operation using a battery source are primary design requirements.
Accurate timing from a crystal oscillator for timing applications such as wall clocks, table clocks, automobile clocks, and digital timing references in any circuit requiring accurately timed outputs at various intervals in the counting sequence.
Driving miniature synchronous motors, stepping motors, or external bipolar transistors in push-pull fashion.

Electronic watch application circuit



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ALPHA-NUMERICAL INDEX

LINEAR INTEGRATED CIRCUITS

MOS INTEGRATED CIRCUITS

COS/MOS INTEGRATED CIRCUITS